

A Comprehensive Survey on Packet and Circuit Switched NoC Routers

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Abstract : This study has been undertaken to present a comprehensive survey to have an insight in network-on-chip design. The article provides a detailed comparison of various performance parameters adopted in the design process of Network on chip router microarchitecture. The article focuses mainly on two broad classes of router viz packet switched and circuit switched routers and reports their respective parameters that may further aid a designer in adopting a better choice while carrying a topological level design process.

IndexTerms – Network-on-chip, Virtual channels.

I. INTRODUCTION

Traditionally the design space exploration for Network on chip has focused on the computational aspects of the problem at hand. However, as the number of components on a single chip and their performance continue to increase the design of the communication architecture plays a major role in defining area, performance, and energy consumption of overall system. Further more, with technology scaling, the global interconnects cause severe on-chip synchronization errors, unpredictable delays, and high power consumption [1] [2]. To mitigate these effects, the network-on-chip (NoC) approach emerged recently as a promising alternative to classical bus-based and point to point (P2P) communication architectures[3]. The NoC paradigm provides a scalable solution to the tough integration challenge of modern SoCs, by applying at the silicon chip level well established networking principles, after suitably adapting them to the silicon chip characteristics and to application demands [4] The general block diagram of a NoC based system is illustrated in figure 3.1. With the application of seminal idea of networking technology to address the chip-level interconnect problem has been shown to be adequate for current systems, the complexity of future computing platforms demands new architectures that go beyond physical-related requirements and equally participate in delivering high-performance, quality of service, dynamic adaptivity at the minimum energy and area overhead[5]. The Network-on-Chip communication paradigm architectures have evolved significantly in key areas starting from topology and routing algorithms [6],[7], [8], [9], and covering router and network interface microarchitecture, over the last decade. The topologies and routing algorithms are usually defined in a generic manner, so as true for a router microarchitecture. The general router design involves assembling hardware blocks from a component library of varying granularity and complexity. Although such an approach has provided so far efficient architectures, its efficiency is limited by the efficiency of the independent blocks; the designer's potential for delivering efficient compositions, and the depth of the design space exploration. There is a high need of a unified customizable model that will cover in a unified manner all micro-architectural alternatives such as control and data path pipelines [10] [8], speculation [11], buffering architecture [12], [13], [14] and allocation policies. The derivation of such a model would allow for rapid, safe architectural changes in order to find the globally optimum architectures bridging the gap between architecture exploration, microarchitecture fine tuning and physical implementation.

II. NETWORK-ON-CHIP ROUTER

The heart of an on-chip network is the router, which undertakes the crucial task of steering and coordinating the data flow. The architecture employed by conventional NoC routers [1] is illustrated in Figure 1(a). The router operation revolves around two fundamental regimes: (a) the datapath, and (b) the associated control logic. The datapath consists of a number of input and output channels to facilitate packet switching and traversal. In general, the router has Q input and Q output channels (or ports). In most implementations, Q=5; four inputs from the four cardinal directions (North, East, South and West) and one from the local Processing Element (PE), which is attached to the NoC router. To minimize router complexity and traffic congestion, NoC routers are usually assumed to connect to a single PE. The input/output channels may consist of unidirectional links, bidirectional, or even serial links. Buffering within a network router is necessary due to congestion, output link contention, and intra-router processing

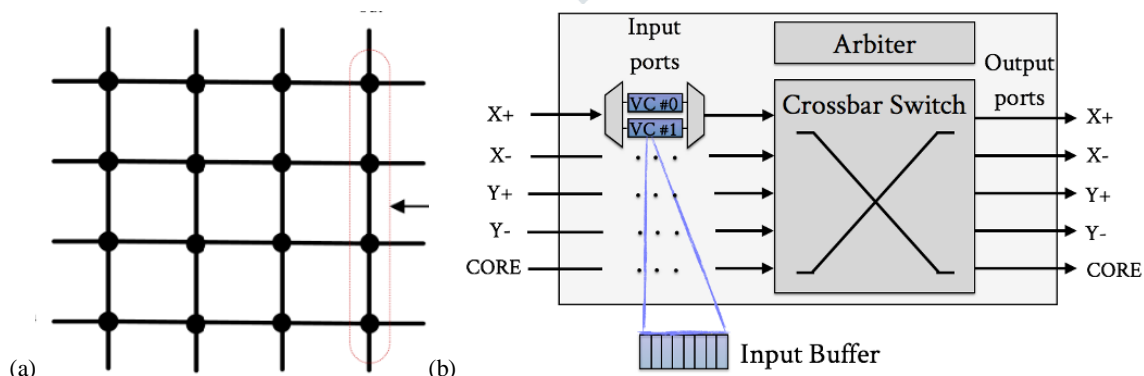


Figure1: Block level architecture of Network-on-chip router node.

III. NOC ROUTER BLOCKS

The section illustrates various blocks of a network on chip router. The network on chip router microarchitecture is composed broadly of two types of circuit's blocks. These blocks are classified as control path block network and data path block network. The control path consists of blocks such as routing and computation blocks, allocations units. While as data path blocks comprises blocks such as buffering and storage units, channel pipeline blocks, crossbar unit and virtual channel units. Figure 2 shows the architecture of a generic virtual channel router. The router has five input ports and five output ports, supporting two virtual channels (VCs) per port. The control logic comprises of the routing computation (RC) unit, the virtual channel allocation (VA) unit, the switch allocation (SA) unit and the crossbar (XB) which connects the input and output ports of the router.

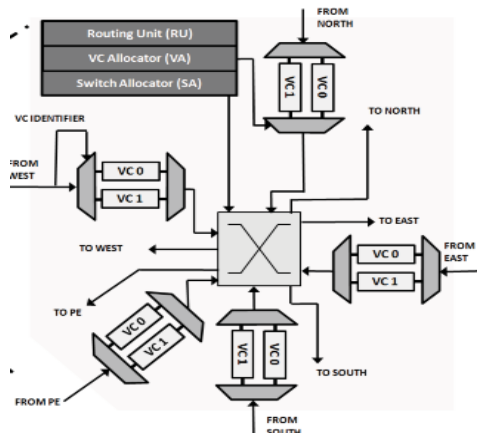


Figure 2: Illustration of Router Microarchitecture.

The detailed discussion of each block is presented as follows:

- **Input Buffering unit:** In a general NoC router, buffers are organized as multiple fixed-length queues (as shown in Figure 2). Each of these queues is termed as a virtual channel. All virtual channels share a physical channel. Each new incoming flit is stored in the VC buffer designated by its VC identifier.
- **Routing path Computation Logic:** The routing path computation logic is used to compute the output port based on the destination information in the head flit using routing algorithms. In a generic NoC router, we use the routing computation logic to compute the output port of the downstream router. Particularly, each input port has its own routing computation unit. The fundamental logic blocks required for implementing a routing logic unit is comparators.
- **Virtual Channel Allocation Unit:** The virtual channel allocation unit allocates an unused VC to a new packet. It only operates on the head flit. Figure 2 shows the block diagram of the virtual channel allocation unit in a generic 2-stage router. In the first stage of this separable virtual channel allocator, every input VC with a head flit arbitrates for an empty VC in the downstream router. In the second stage, head flits that have been allocated to the same VC at the downstream router compete with each other.
- **Switch Allocation Unit:** The switch allocation unit determines which input VC from an input port can transmit a flit through the crossbar in the next cycle. Figure 5 shows the micro-architecture of the switch allocation unit in a generic 2-stage router. It can be seen that two switch allocators are implemented. One handles speculative requests (from packets that are also requesting a VC) and the other one handles non-speculative requests. Non speculative requests have higher priorities over speculative requests. The red rectangular box shows the diagram of a separable switch allocator. The first stage is used to select an input VC from each input port. The second stage is used to arbitrate for an output port.
- **Crossbar:** The crossbar connects the input and output ports. Figure 6 shows the block diagram of the crossbar in a generic NoC router, where Q is the number of port. Each output port has an associated multiplexer. The control signal comes from the result of SA.

IV. SWITCHING CLASSIFICATION IN NOC ROUTERS.

Messages are data that have to be sent from a sender to a receiver through a network. Messages can be transformed into packets, by encapsulating all or part of each message with network control information. Alternatively, messages can be sent after a connection establishment between the sender and the receiver. This defines the two basic modes for message transmission in networks, packet switching and circuit switching, respectively. Wormhole packet switching is the switching mode most commonly employed in NoCs [15]. Packet-switched networks often allow for high aggregate system bandwidth, as each packet can be distributed across a subset of network nodes at any given instant [16]. However, such networks generally require congestion control and packet processing, which include the need for buffers to queue packets awaiting the availability of routing resources. Correct buffer sizing is a fundamental parameter to optimize NoC performance. Small buffers increase network congestion and large buffers increase area and latency overhead. This switching mode supports well best-effort (BE) services [17], being efficient for traffic with short and frequent packets. HERMES [18], Xpipes [19], MANGO [20] and SoCIN [21] are examples of NoCs employing wormhole packet switching. Another switching mode employed in NoCs is circuit switching. It can provide guaranteed throughput and latency bounds for individual packets, since an exclusive path is allocated to data transfers between requirement is typically a single register instead of a FIFO buffer, since when the circuit is established the NoC acts like a pipeline where each router acts as a stage. The disadvantages of circuit switching are the channel bandwidth underutilization when data is transmitted at lower rates and the setup latency to establish a circuit, which depends on the traffic in the path during circuit establishment. This switching mode is more efficient for traffics with long packets transmitted at high rates, with requirements for throughput and latency guarantees. Representative circuit-switching NoCs are Aetheral [22], SoCBUS [23] and Octagon [24]. Aetheral employs circuit switching only for traffic with QoS requirements, while BE traffic uses wormhole packet switching. Table I summarizes the main advantages and inconvenient features of circuit switching and wormhole packet switching.

Table I. Advantages and disadvantages of NoC switching modes.

Features	Features	Features
→Switching Mode	Advantageous	Inconvenient
Circuit Switching	Guaranteed throughput and latency - Single register instead of FIFO buffers	- Static path, reservation and possibly wasted bandwidth
Wormhole Switching	Shared NoC resources, enabling to distributes multiple flows simultaneously along routers	- Under heavy traffic, flits may block an important number of routers - Wasted bandwidth when the traffic initiator rate is slower than the channel rate

V. RESULTS AND DISCUSSION

There are many different ways to measure and present the performance of a particular NoC based system, however the standard metric to measure the performance of a NoC are throughput, latency, and area. While these names sound generic, their exact definition depends strongly on how we measure them or, more specifically, the measurement setup. Power analysis determines the amount of on-chip power dissipated during operation. For high throughput NoC systems it is more appropriate to quantify the power efficiency through energy analysis. To compare and contrast different NoC architectures, a standard set of performance metrics can be used. Another parameter of interest is throughput. Throughput is the rate at which packets are delivered by the network for a particular traffic pattern. It is measured by counting the packets that arrive at destinations over a time interval for each flow (source-destination pair) in the traffic pattern and computing from these flow rates the fraction of the traffic pattern delivered. Throughput, or accepted traffic, is to be contrasted with demand, or offered traffic, which is the rate at which packets are generated by the packet source. Area on the other hand may be defined as the amount of logic resources needed to implement a NoC architecture. Table 2 gives a detailed comparison of various parameters of interest reported by various authors while designing a packet switch based router microarchitecture. Table 3 gives a detailed comparison of various performance parameters reported by various authors while designing a circuit switch based NoC router microarchitecture.

Table 2: Comparison of performance parameters in various packet switched NoC routers

Authors	Channel type	Topological connections	Routing algorithm	Throughput	Timing delay (ns)	Power (mW)
David. A et-al [25]	PS	4x4	custom	NA	1.33/cycle	1.08
Mehdi et-al[26]	PS	6x6	encoding scheme algo	32bit/0.3ns	0.3	254 for DSB
Rohit et-al[27]	PS	8x8	WXY routing	1 Gbps	1	NA
Mohammad et-al[28]	PS	4x3	RACO-CAR Routing	1.879 Gbs/node	2	51
En-jui chang et-al[29]	PS	16x16	RoShQ5	0.362 f/cycle	1	58.26
Anh. T. Tran et-al[30]	PS	2D mesh	PAA routing	0.02Gps	0.015	108.2
JIANG et-al[31]	PS	4x4	custom	NA	1.33/cycle	1.08

*PS= Packet switching, CS= Circuit switching, NA Not Available.

Table 3: Comparison of performance parameters in various packet switched NoC routers

Authors	Channel type	Target device	Resources used	Throughput	Frequency(MHz)
Matheus et al [32]	CS	V5	0.35 % total LUT	NA	NA
lu wang [33]	CS	Asic	80000Um2	.4 F/c/node	NA
Bouraoui Chemli[34]	CS	v6	7847	NA	NA
yahia salah[35]	CS	S3	713 slices	0.7	134
yahia slah[36]	CS	V2	291 Slices	0.35	164
jawad latief[37]	CS	NA	NA	1.14	NA

*PS= Packet switching, CS= Circuit switching, NA Not Available.

VI. CONCLUSION

The paper provides a comprehensive introduction about Network on chip routers. The comprehensive survey provided in this article will help NoC designers to adopt a proper microarchitecture for the design of a NoC based topology.

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