

Design of High Gain DC-DC Boost Converter for PV Application and its Simulation in PSIM

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Abstract—With increasing power consumption and demand for power, PV applications are coming up as ideal solution. The objective of this paper is to achieve high gain, high efficiency DC-DC converter for the PV application. This converter uses three switches to boost the output voltage up to 6 times the input voltage with duty cycle in the range 16%-25%. Thus reducing the conduction losses as compared to conventional boost converter. The converter uses transformer less topology as efficiency of the transformer less topology is better than the transformer topology. The converter is designed for an input of 25-50V and output of 300 to drive load of 450W. The results are validated using PSIM software.

Keywords— PV (Photo Voltaic) , Boost converter , Transformer less topology

I. INTRODUCTION

With increasing power consumption and demand for power, PV applications are coming up as ideal solution. As the fossil fuels are depleting, one such renewable resource i.e. Solar is being widely used for the power generation for domestic utilization as it is more economical, efficient and also available easily. The PV cells are connected in series and/ or parallel to form a PV array. The PV array can have an output voltage in the range 12-48V [2]. In order to utilize this energy for the domestic utilization, an inverter which converts the DC voltage

to AC is required as shown in Fig1. After this stage, the energy can be utilized for the domestic applications. Also the system can be connected to grid for energy management. Step up converters with high gain are used to get the required voltages. In conventional boost converters, to achieve the high gain, the duty ratio has to be increased beyond 0.9 and requires pulse width modulation[1].

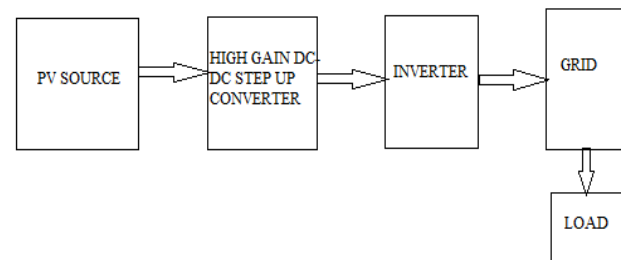


Fig 1: Block diagram of Power conversion with High gain boost converter

With high duty ratio these converters produce high voltage gain but practically it is limited by the switch commutation time in the circuit[4]. These times play significant role in high frequency operation. As duty ratio increases, the diode conduction period reduces[3]. If the frequency increases, diode conduction time will be taken by the commutation time. Thus the range of duty ratio should be smaller to overcome these problems.

To overcome this problem, this paper presents a step up converter that can operate at low duty ratios to provide higher voltage gain. The circuit uses 3 switches, capacitors, inductor and diode.

The important features of the converter are: simple in structure, high voltage gain, smaller duty cycle for reducing the conduction losses of power switches, also less voltage stress on the power devices.

II. PROPOSED CONVERTER

Fig 2 shows the proposed converter. The Circuit of the converter consists of four capacitors (C0-C3), one inductor (L), three power switches (Sw1, Sw2 and Sw3), five diodes (D0-D4) and a resistive load (R). The circuit operates in two modes. All the three switches operate simultaneously. The circuit operates in two modes. Mode1 when all the switches are turned on and Mode2 when all the switches are turned off. The assumption made during the analysis are

- (1) The devices used are ideal and lossless
- (2) The output capacitor capacitance is very large to maintain the constant output voltage
- (3) Current in the inductor increases or decreases linearly

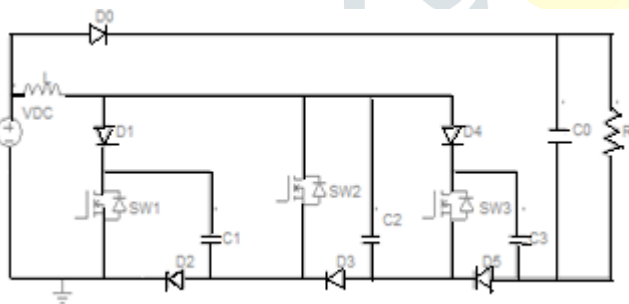


Fig 2: Block diagram of high gain DC-DC converter

To reduce the ripple in the output voltage and current, LC filter is used. This circuit is designed to drive a load of about 450W. Resistive load (RL) corresponding to this wattage is shown for demonstration purpose. The key waveforms of inductor current and voltage are shown in fig3. The design of circuit parameter is shown in section III and the result validation in PSIM is shown in section IV.

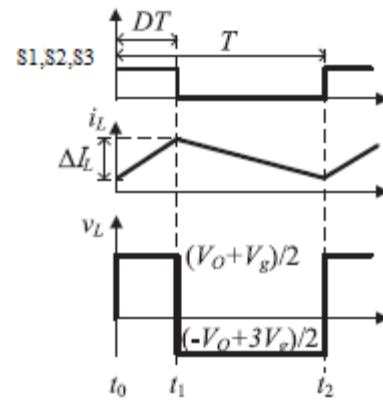


Fig 3: Key waveforms of the Circuit

A. Circuit analysis when the switches are on

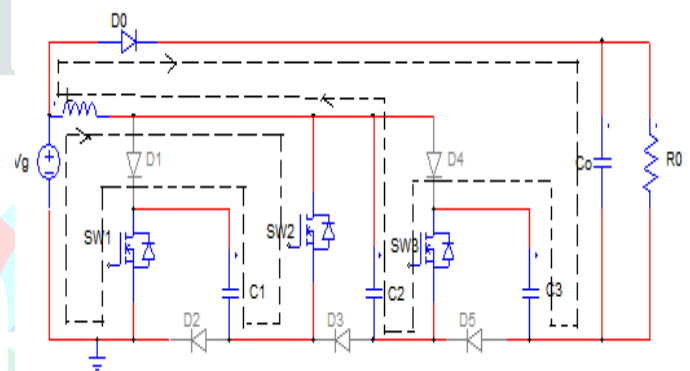


Fig 4: Circuit operation when all the switches are on

When all the switches are turned on, the inductor current increases linearly. Diode D0 is forward biased and the diodes D1-D5 are reverse biased. The capacitors C1-C3 that are previously charged are discharged now. The time interval in this mode is DT. The current follows the path as shown in fig 4.

B. Circuit analysis when the switches are off

When all the switches are turned off, inductor current decreases linearly. Diode D0 is reverse biased and the diodes D1-D5 are forward biased. The capacitors C1-C3 are charged. The time interval in this mode is (1-D)T. The current follows the path as shown in fig 5.

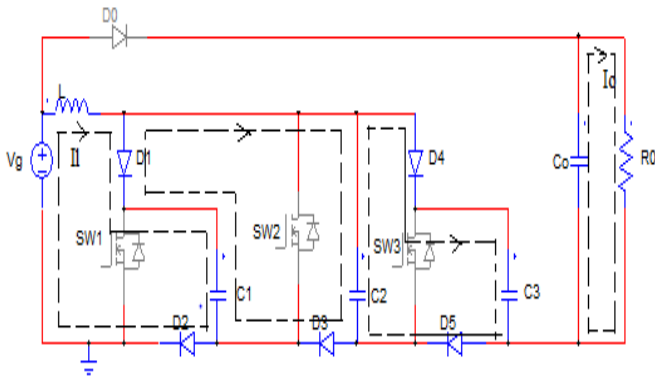


Fig 5: Circuit operation when all the switches are off

III. PROPOSED CONVERTER DESIGN

The role of main components of the proposed boost converter are discussed and their values are calculated to meet the requirement.

In the specification the input voltage 50v generates an approximate output voltage of 300 Volts.

Table1: Specifications of the converter

Sl. no	Parameters	Values
1	Power Rating	450W
2	Input voltage	50V
3	Output voltage	300V
4	Duty Cycle	16%
5	Output Current	1.5A
6	Resistance	200 Ω
7	Voltage gain	$(4-2D)/(1-2D)=6$
8	Switching frequency	50KHz
9	Inductance (L)	0.93mH
10	Capacitance (C1-C3)	22 μF

When the switches are closed

$$L \frac{di}{dt} = Vg + Vc1 \dots \dots \dots (1)$$

Applying KVL ,

$$Vo = Vc2 + Vc3 + V1 \dots \dots \dots (2)$$

Substituting (1) in (2),

$$Vo = Vg + Vc1 + Vc2 + Vc3 \dots \dots \dots (3)$$

We can observe that the output voltage is the sum of supply voltage and capacitor voltages.

$$\Delta Ii(\text{closed}) = \frac{Vg + Vc1}{L} DT \dots \dots \dots (4)$$

When the switches are open

$$L \frac{di}{dt} = Vg - Vc1 \dots \dots \dots (5)$$

Applying KVL,

$$Vc1 = Vc2 - Vc3 \dots \dots \dots (6)$$

$$\Delta Ii(\text{open}) = \frac{Vg - Vc1}{L} (1 - D)T \dots \dots \dots (7)$$

Using volt-sec balance equation,

$$Vc1 = \frac{Vg}{1 - 2D} \dots \dots \dots (8)$$

We know that,

$$Vo = Vg + Vc1 + Vc2 + Vc3 \dots \dots \dots (9)$$

Substituting (8) in (9)

$$Vo = Vg + 3 \left(\frac{Vg}{1 - 2D} \right) \dots \dots \dots (10)$$

Rearranging equation (10), we get

$$\frac{Vo}{Vg} = \frac{4 - 2D}{1 - 2D} \dots \dots \dots (11)$$

Inductor value used in the circuit is given by the equation (12). Considering 1% ripple current

$$L = \frac{D(1-D)(4-2D)T Vg^2}{ri\%(1-2D)Po} \dots \dots \dots (12)$$

Capacitors C1, C2, C3

$$C1, C2, C3 = \frac{(1-2D)T Po}{rv\%(3-2D)Vg^2} \dots \dots \dots (13)$$

Capacitor Co

Output capacitor value is given by the equation 14.

$$Co = \frac{(1-D)(1-2D)^2 T Po}{rv\%(3-2D)Vg^2} \dots \dots \dots (14)$$

IV. SIMULATIONS IN PSIM AND ITS RESULT

The simulation of the high gain step up converter is carried out in PSIM to validate the results and the output waveforms are as shown.

Fig 8 shows the simulation circuit of the proposed converter in PSIM.

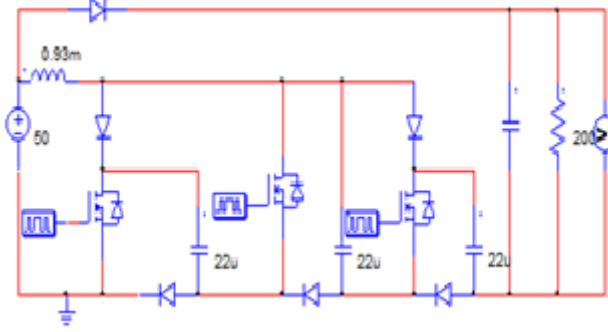


Fig 6 : Simulation Circuit in PSIM

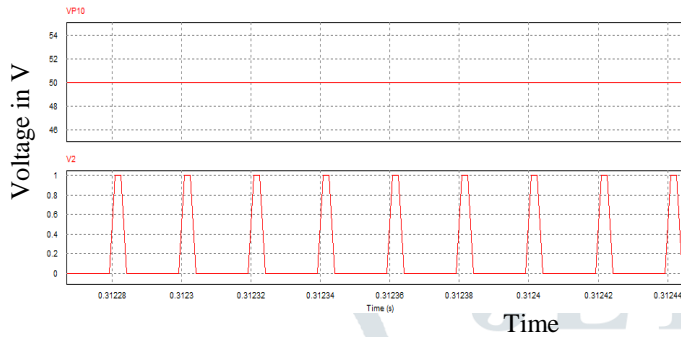


Fig 7: Input voltage and Gate pulse

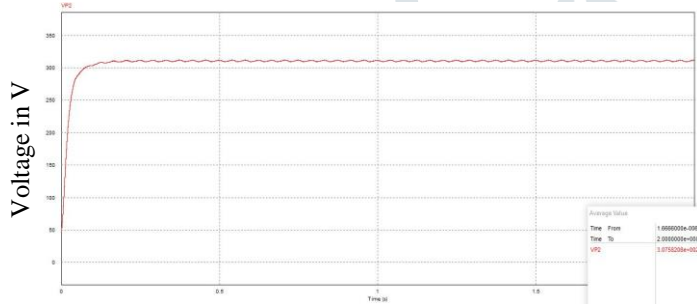


Fig 8: Ouput voltage=300V Time

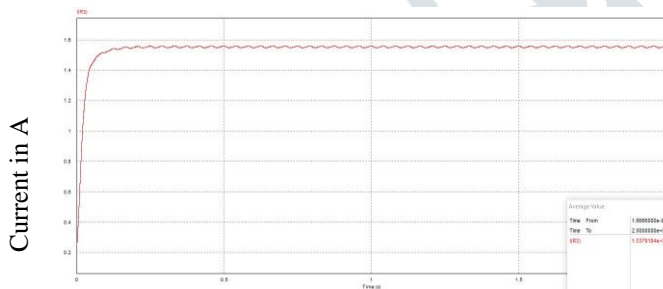


Fig 9: Ouput current=1.5A Time

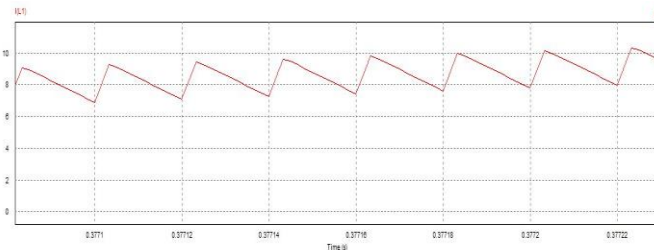


Fig 10: Inductor Current= 9A Time

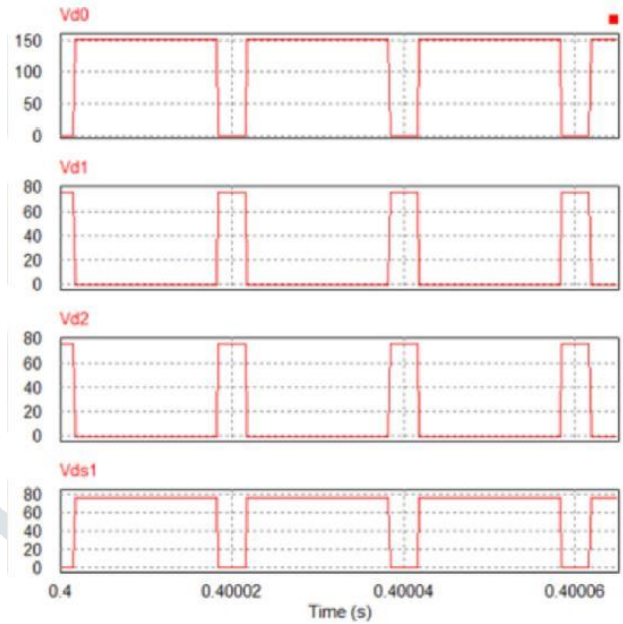


Fig 11 : Diode Voltages

V. RESULTS

The dc-dc boost converter with high gain and less stress on switching devices and diodes is analyzed. This converter is efficient to operate at the frequency of 50KHz. The converter attains a constant 300V output at full load i.e. 200Ω for an input voltage of 50V. Furthermore, the boost converter attained the high voltage gain as expected with duty cycle of 0.16.

VI. CONCLUSION

A High gain dc-dc boost converter is designed . The main attributes of the proposed dc-dc converter are high voltage gain , simple in structure, smaller duty cycle that reduces conduction losses of the switches. Also lesser voltage stress experienced by the power switches.

The principle of operation, design and the simulation results are presented to validate the theoretical analysis.

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