# REVIEW ON ENERGY EFFICIENT SRAM DESIGN

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**Abstract**- With the increment of mobile, biomedical and space applications, digital systems with low-power consumption and high speed are required. As a main part in digital systems, low-power and high speed memories are especially desired. Reducing the power supply voltages to sub-threshold region is one of the effective approaches for low-power applications. However, the reduced Static Noise Margin (SNM) of Static Random Access Memory (SRAM) imposes great challenges to the sub-threshold SRAM design. The conventional 6- transistor SRAM cell does not function properly at sub-threshold supply voltage range because it has no enough noise margin for reliable operation. In order to achieve low-power at sub-threshold operation, previous research work has demonstrated that the read and write decoupled scheme is a good solution to the reduced SNM problem. A Dual Interlocked Storage Cell (DICE) based SRAM cell was proposed to eliminate the drawback of conventional DICE cell during read operation. This cell can mitigate the single-event effects and also improve the stability. Also switching activity can be improved for low power and high speed design of SRAMs.

## I. INTRODUCTION

### *A. BASIC SRAM CELL*

SRAM stands for Static Random Access Memory .Static memory cells basically consists of two back to back inverters as seen in Fig. 1. The output of the second inverter (Vo2) is connected to the input of the first inverter (Vi1). If we consider the voltage transfer characteristics of the first inverter (Vo1 vs.Vi1) and that of the second consideringVo2vsVi2 as shown in Fig. 2, there are three possible operating points (A, B and C) obtained by intersection as shown in Fig. 2. It may be seen that operation points A, B are stable as loop gain is less than 1. Point A shows that the out-put of inverter1 is high and the output of the inverter2 is low. Point B shows that the output of inverter1 is low and the output of inverter 2 is high. This shows that the outputs of two inverters are complementary in any stable condition. This property is made use of to realize static random access memory SRAM.

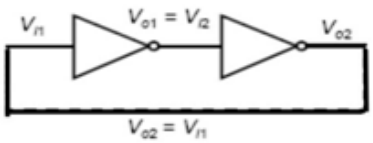


Figure 1.: Inverters connected back to back

Point C is a meta stable operating point as the loop gain at point C is much larger than 1. When a small perturbation is applied to the input of the first inverter when the operating point is C, it gets amplified by the gain of the first inverter and is applied to the input of the second inverter and again amplified by the gain of the second inverter. The values of Vo1 and Vo2 (Vi2) increases and the bias point moves away from C until it reaches either A or B. Fig. 2 shows transfer characteristics of a Meta stable system . The curve in Fig.2 is also known as Butter fly curve.

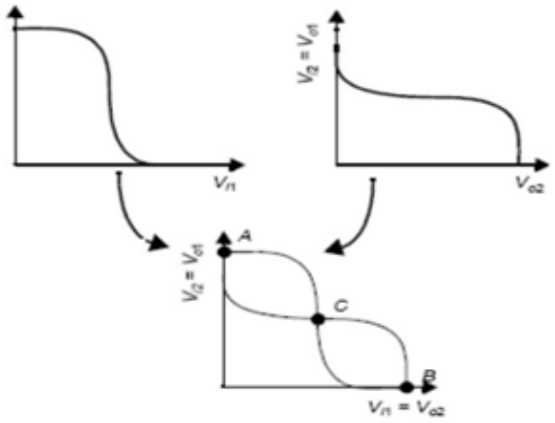


Figure 2 : Transfer characteristics of an inverter with meta stable state at C

**Conventional SRAM cell and Static Noise Margin**

The most popular and widely implemented structure in commercial SRAMs is the conventional 6-Transistor (6T) structure, shown in Fig 3

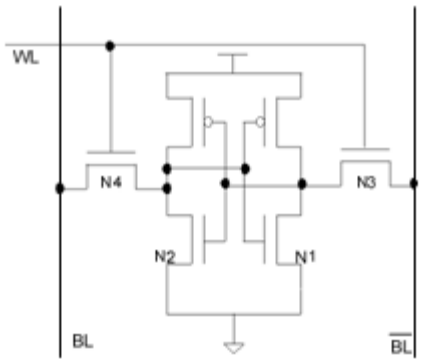


Fig 3: Conventional 6T SRAM cell

Cross-coupled inverter pair in the 6T cell is the main part of of the static storage elements, including register files, SRAMs, latches and flip-flops. There are two important aspects in SRAM design, one is cell area and the other is the stability. The former can be reduced by technology scaling down, but the stability is always a prominent issue. To analyze the stability, power and speed of SRAM cells, a number of researches have proposed different ways to define energy efficient SRAM.Static Noise Margin (SNM) and its analytic criteria which is widely used to evaluate the stability of SRAM cells. Enhancing the switching activity is also analyzed to decrease power consumption.

## II. LITERATURE REVIEW

This section describes various attempts made by investigators to reduce the power dissipation in SRAM or to develop low power and energy efficient SRAM. These investigations cover SRAMs operated at low voltages reducing power dissipation, SRAMs using techniques like power gating in which the circuits are switched off when they are not needed , SRAMs (drowsy) where the power supply voltage is reduced to a lower value during standby mode and SRAMs based on adiabatic techniques. Lowering the power supply voltage reduces the dynamic power quadratic ally and leakage power exponentially. But power supply voltage scaling also limits signal swing and thus reduces noise margin.

Evert Seevinck et al.[1987] investigated the stability of both R load and full CMOS SRAM cells analytically as well as by simulation .The expressions for Static Noise Margin as a function of device parameters and supply voltages have been derived. By analytical method they have concluded that SNM for both Rload and 6T CMOS cell depends on threshold voltage vdd, beta ratio ,cell ratio .SNM for Rload and 6t CMOS increases with increase in cell ratio and Vt .SNM 6T is independent of VDD

variation but SNM® always decreases with decrease in vdd. Also by simulation method they have shown that full CMOS cells have better SNM values than R load cells at low power supply voltage and to maintain reasonable SNM values at reduced power supply the area required by the R-load cell will be close or equal to that of full CMOS cells[1].

Martin Margala [1999] proposed different techniques for power reduction in both active and standby modes. The most efficient techniques which are used in power reduction are

1. Capacitance reduction of word lines and number of cells connected to them, data lines input/output lines and decoders .
2. DC current reduction by using new pulse operation technique for word line, periphery circuits and sense amplifiers .
3. AC current reduction by using new decoding techniques( Multistage static CMOS decoding)
4. Operating voltage reduction
5. Leakage current reduction by utilizing multiple threshold voltage or variable threshold voltage technologies.

All above techniques were studied and it was found that there is drastic reduction of power consumption by capacitance reduction, DC and AC current reduction and suppression of leakage current[2].

Michael Powell et.al [2000] has explored an integrated architectural and circuit approach to reduce leakage energy dissipation in instruction cache. They proposed a gated Vdd , a circuit level technique to gate the supply voltage and reduced leakage in unused SRAMS cells. Gated Vdd enables a DRI i-cache to turn off the supply voltage and eliminate virtually all leakage energy dissipation in the caches unused sections. They used the extra transistor in the supply voltage or in the Ground path of the caches SRAM cells. The extra transistor is turned on in used sections and turned off in unused sections . The results indicate that a 64k DRI i-cache reduces the energy delay at best by 87% and on average by 62% with less than 4% on execution time. The results indicated that a wide NMOS dual –Vt-gated Vdd with a charge pump reduces leakage most with minimal impact on cell speed and area.

Azeez J.Bhavanagarwala et.al [2001] investigated about the effect of intrinsic threshold voltage fluctuations on static noise margin. They have used compact physical and stochastic models for investigation of reduction in static noise margin of SRAM cell. These enable accurately assessing the impact of stochastic variation in device threshold voltage due to random placement of dopant atoms on cell stability. Stochastic distribution of cell SNM across the 1997 NTRS technology nodes calculated using models demonstrates substantial reduction in cell SNM for sub 100nm technology generation[3].

Krisztian Flaunter et.al [2002]talked about the caches which are the main candidates of leakage reduction since they contain a significant fraction of processors transistor .Various techniques has been discussed for dealing with leakage power problem. These techniques either completely turn off circuits by creating a high impedance path to ground or trade off increased execution time for reduced static power consumption .In this paper they used Dynamic Voltage Scaling to reduce leakage power of cache cells. By scaling the voltage of cells to approx. 1.5 times Vt , the state of the memory cell can be maintained. So according to the paper ,in 70nm CMOS process, drowsy caches will be able to reduce total energy( Static or Dynamic) consumed in caches by 50% -75%.[4]

Kevin Zhang et.al [2005]has designed and fabricated 70 MB SRAM in 65nm CMOS technology . The cell has area of 0.57 um^2 (0.464*1.2 um). The device sizes are optimized to achieve 150 mV Static Noise Margin down to 0.7V operation .A dynamically controlled sleep transistor technique is implemented in fully synchronized sub array for leakage reduction .It has also a built in programmable defect “screen” circuit for high volume manufacturing. The measurements have shown that the SRAM leakage at 1.1V is reduced by 3-5 times in data retention mode.[5]

Lawrence T. Clark et al.[2005] has discussed the problems occur in SRAM with the scaling of voltage .Scaling increases leakage current components to the point where stand by power is frequently a limiting design factor . So in this paper , circuit to implement the low power state, which addresses the increasing leakage components that face sub 130nm technologies is presented . This is accomplished by placing the IC State in latches fabricated using thick gate , high Vt transistor and cutting off the supply to non state logic circuitry. This decouples the performance of IC in active operation from the standby operation . This approach is applicable to various static and dynamic circuits.[6]

Jinhui Chen et al. [2006] has proposed 512 *13 bit ultra low power sub threshold memory which is fabricated on a 130nm process technology .The memory is fully functional at 190mV with 28KHz clock frequency . However such low voltage creates so much difficulties in memory design since the ratio of I on /I off is greatly reduce in high fan in /out circuits. So that’s why researcher

proposed a number of circuit techniques to overcome I on /I off ratio and poor drive strength of the transistor operating in sub threshold .These techniques are gated feedback memory cell and decode circuits.[7]

Koichi Takeda et al.[2006]has proposed seven transistor SRAM circuit , in which several transistor are low Vth nMOS transistor used to achieve both low Vdd and high speed operations .In this, a single transistor for loop cutting is added to a 6T cell. This makes it possible to reduce area overhead from 30 to 13% compared to 8T cell and also overcome the SNM problem encountered with 6T SRAM cell . They have fabricated a 64kb SRAM Macro using 90nm CMOS technology and have obtained with 0.5 V supply , a minimum Vdd of 440 mV and 20nm access time .[8]

Srikanth Sundram et.al [2006] presented the sense amplifier which senses the current from SRAM with high speed. They proposed the sense amplifier which uses WTA technique (winners take all ) approach for nano scale SRAMs and can tolerate 10 percent threshold variation. They compared the energy consumption and sensing delay of the proposed technique with normal sense amplifier in 70nm technology and found that the WTA sense amplifier provides 70-80% improvement in sensing speed and consumes 28-70% less energy than traditional voltage and current mode sense amplifier.[9]

Ramy E.Aly et al.[2007] tried to optimized the power by controlling the switching activity of bit lines because charging and discharging of bit line capacitance represents a large portion of power consumption during write operation . They proposed 7T SRAM cell with reduced switching activity of bit line pair to perform write operation .This has been observed that cache area increases by 12.25%.The researcher has also used sleep transistor technique to reduce leakage power and also by carefully sizing of transistor read delay and Static Noise Margins are also maintained.[10]

Benton High Smith et al.[2008]has explored the limit of low voltage operation for traditional (6T SRAM. Due to low voltage operation SRAM suffers from two major problems Soft error rate and degraded SNM for read and write operation .So the researcher has proposed an alternative bit cell that functions to much lower voltages . Measurements shown that the 65nm 10T bulk CMOS solves the read SNM problem, overcomes the write problem and relaxes the integration limitation to allow sub threshold operation. At 400 mV it consumes 32.8 uW and works up to clock frequency 475 KHz.[11]

E.I Vatajelu et al.[2008]investigated the effect of lowering the supply voltage on robustness of 6T SRAM cell both in saturation and sub threshold regions .The Static Noise Margin is evaluated analytically and compared with Hspice simulations for 130nm,90nm,65nm BPTM. It was found that Static Noise Margin decreases non linearly with the supply voltage but the relative noise margin increases up to a maximum value and after that decreases .The proposed analytical model also predicts that minimum value of supply voltage that preserves the data stored in SRAM.[12]

Kuande Wang et al.[2014] discussed the effect of scaling in SRAM circuits . Due to voltage scaling various errors occur in SRAM .Theses include soft errors, Single Event Upsets and degraded noise margin etc. To mitigate single event effect , improve the stability and also to maintain low power characteristic of sub threshold SRAM, a dual interlocked storage cell based SRAM cell in 90nm CMOS technology was proposed to eliminate the drawback of conventional DICE cell. The replica technique used in sense control makes this proposed 14T transistor SRAM cell be able to work under variable power supply voltages and due to this it has achieved optimal speed whereas standby leakage current is somewhat more than Conventional DICE cells.[13]

Mohammed Shafique and Ruchi Sharma[2016] presented the comparative Study of different type of sense amplifier.They analysed voltage mode sense amplifier and charge transfer sense amplifier in which they compared different parameters like sensing delay , power and speed .For this ,they used the TANNER EDA software for simulation . At last they presented the result in which they showed that the CTSA (Charge Transfer Sense Amplifier) has higher speed with small delay with low power dissipation than Voltage Mode sense amplifier .

K.khare et al.[2017] has proposed various techniques for reducing leakage power because with the shrinkage in technology ,the leakage current is increasing very fast. These techniques include sleep transistor approach and stack transistor approach. The two techniques have been compared and various models 6T,8T,10T with sleep transistor has been proposed. The SRAM with sleep transistor shows better leakage reduction than stack approach .It has also shown in the paper that 10T SRAM type II with sleep model is best technique and reduce more than 98 % leakage power. However the area has been increased compare to conventional SRAM.[14]

## III. CONCLUSION

After going through various research papers and study related to this topic it can be concluded that high speed , low power SRAMs are very important for digital systems. However designing of high speed, low power SRAMs are very challenging because with large scale integration, the performance of embedded memory and peripheral circuits can adversely affect the speed and power of overall system. Also large memories use long bit lines which present a large capacitive load to the memory cell ,thus cause extra signal delay .To eliminate this , high speed sense amplifiers are presented in various papers. Many researchers focused on reducing the switching activity on bit lines which helps in reducing the power consumption. Various other techniques are also presented like reducing the bit line capacitance, sleep transistor approach, stack transistor approach, multi threshold transistor approach for reducing AC, DC and leakage currents through memories which further reduces power consumption. So by implementing the above used techniques we can design low power , high speed energy efficient SRAMs.

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