CASCADED H-BRIDGE FIVE LEVEL INVERTER WITH REDUCED SWITCH COUNT USING SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUE

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Abstract: Multilevel inverters are designed to produce desired output voltages from different DC sources. This includes high quality output voltage, reduction of voltage stress on the switches, low common mode voltages, better harmonic content and reduction in total harmonic distortion. As there will be reduction in THD the size of the filter will also get minimized which decreases complexity of the system. Multilevel inverter employs sinusoidal pulse width modulation technique to get undistorted output voltage by eliminating lower order harmonics. By varying the modulation index ratio output voltage levels can be varied. Cascaded H-bridge multilevel inverters are most preferable because of its modularity, reliability, less usage of clamping diodes and ease of control of circuitry and it also reduces the switching and conduction losses of the system. By connecting several modules of multilevel inverter in series configuration desired output level can be achieved. These multilevel inverters are widely used in industrial as well as domestic appliances and the demand has been growing day by day for the continuous supply of power.

I. INTRODUCTION

Multilevel inverters are come out as the new breed for high power applications. Multilevel inverters are playing a major role in most electrical systems such as large motors, flexible AC transmission systems, power quality improvement devices and renewable energy converter. Multilevel inverter approach enhances the usage of high - power and high voltage electric motor drive systems. Switching scheme of multilevel inverters are categorized into high switching frequency methods such as SPWM strategy and low switching frequency techniques often equal to fundamental switching frequency of the components which create stepwise output voltage waveform. Second category includes three major switching strategies so- called optimized harmonic stepped waveform, selective harmonic mitigation PWM and optimal minimization of the THD. Selective harmonic elimination is as effective method to mitigate the low – order harmonic components. Cascaded H-bridge with reduced switch count multilevel inverter is proposed in the paper which compromises of several low frequency transformers. Due to the reduction in number of switching components the size and the cost of realization also reduces and sinusoidal pulse width modulation technique is employed to get a high-quality output voltage.

II.RELATED WORK

A New Cascaded H-Bridge Multilevel Inverter with Reduced Switch Count [1]The publishers explained about the cascaded H-bridge multilevel inverter using less number of switches. As the number of switches is reduced, the output level also increases due to which minimized conduction losses and switching losses are obtained. The proposed multilevel inverter includes series connected modules which can generate only unidirectional positive voltage. In order to get the bidirectional voltage an H-bridge is connected. The proposed block diagram employs sinusoidal pulse width modulation technique (SPWM). Generally, SPWM requires (L-1) carriers but in the proposed block diagram only (L+1/2) carriers are much sufficient for the operation of block. Due to the use of less number of carriers controlling of the circuit becomes less complex, size and installation cost also reduces.

Cascaded seven level inverters with reduced number of switches using level shifting PWM technique [2].The paper explains about multilevel inverter and its advantages. The paper proposes two new topologies of 7- level cascaded multilevel inverter with reduced number of switches than that of conventional type which has 12 switches. The topologies consist of circuits with 9 switches and 7 switches for the same 7-level output. Therefore, with a less number of switches, there will be a reduction in gate drive circuitry and also very few switches will be conducting for specific intervals of time. The SPWM technique is implemented using multicarrier wave signals. Level shifted triangular waves are used in comparison with sinusoidal reference to generate sine PWM switching sequence. The number of levels shifted triangular waves depends on the number of levels in the output i.e. for n levels, (n-1) number of carrier waves.

Performance of Three Phase 11-level Inverter with reduced number of switches using different PWM Techniques [3], The paper implemented the new three phase configuration to produce the 11-level output with low total harmonic distortion (THD). In phase disposition, alternate phase disposition, carrier overlap and variable frequency techniques are used to produce switching pulses. The waveform obtained after implementing the series LC filter at the inverter output is analyzed in the paper. The proposed inverter configuration has 8 switches and 3 DC sources per phase. The series combination among the three DC sources V_{DC}, 2 V_{DC} and -2 V_{DC} can be used to produce eleven DC levels at the inverter output in a single cycle.

III. PROPOSED SYSTEM

To overcome existing system, newly designed five level cascaded H-bridge is implemented. The design includes single switching element and four diodes are added in H-Bridge inverter which connects to DC power supply. The switching control should be proper so that it can generate half of the input Dc supply voltage. The obtained corresponding five voltage outputs are V, V/2, 0, -V/2, -V. The switches S_1 and S_2 are turned on to get voltage output V. Likewise, the switches S4 and S5 are turned on to get voltage output V/2. The switches S_3 and S_4 or S_1 and S_2 are turned on to get voltage output 0. The switches S_2 and S_5 are turned on to get voltage output –V/2.

IV. DESIGN METHODOLOGY

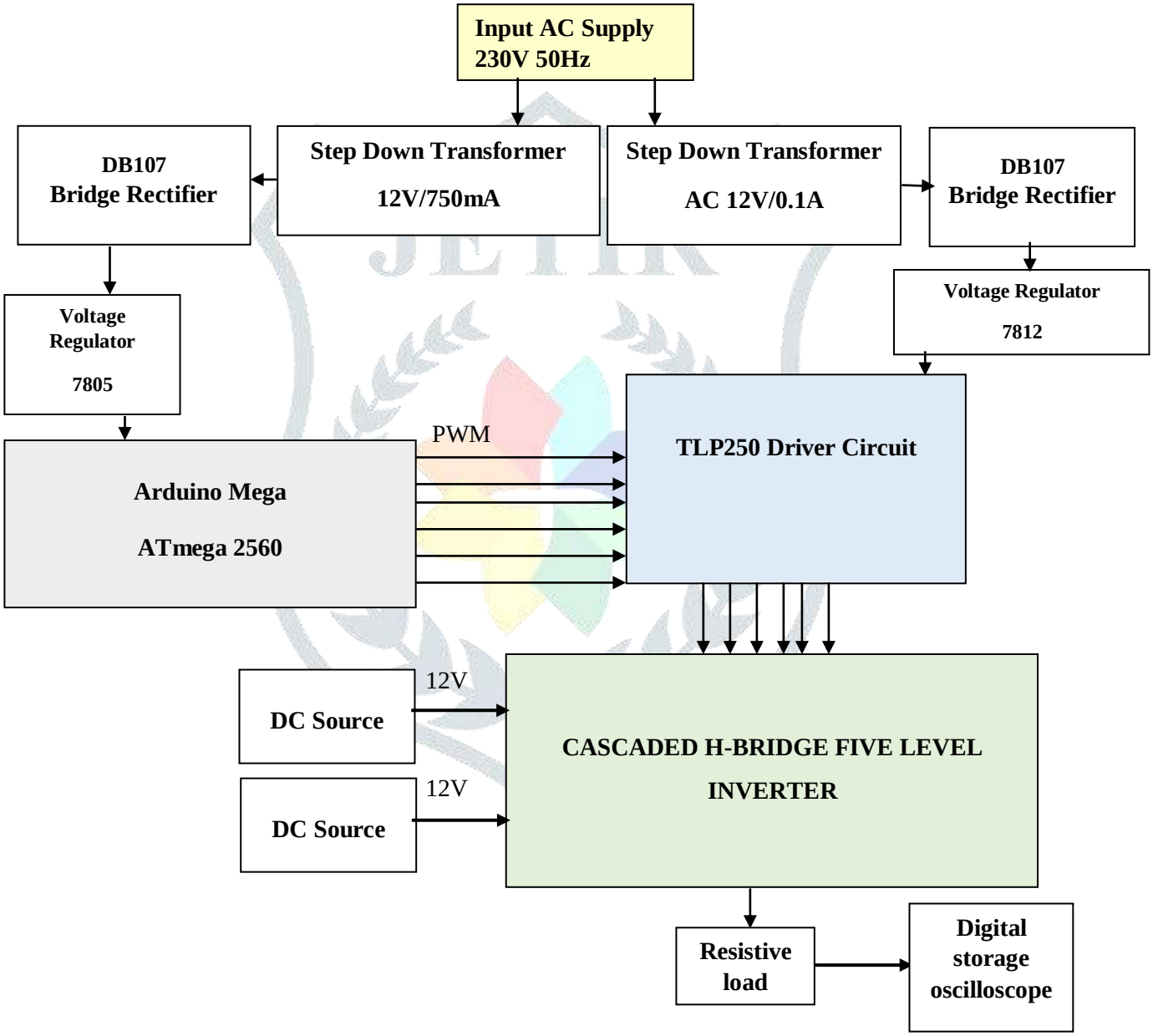


Figure 1. Block Diagram of Proposed Hardware System

Fig.1 shows the complete block diagram cascaded H-bridge five level inverter using SPWM technique which consists of transformer, rectifier, filter, voltage regulator 7805 and 7812 IC, cascaded H-Bridge five level inverter, microcontroller Arduino mega 2560 and resistive load and digital storage oscilloscope. The brief explanation of each block is explained in the following.

STEP DOWN TRANSFORMER (12-0-12V): It is static device which transfers power from one circuit to the other circuit with constant frequency. It works on the principle of electromagnetic induction. Transformer does not have any rotating parts so the efficiency of the transformer is high compare to the all electrical equipment's.

BRIDGE RECTIFIER (DB107): It is a device which converts the ac signal into dc signal. The output voltage of a rectifier circuit contains unwanted ac components (components of supply frequency f and its harmonics) along with dc component. In order to reduce ac components from the rectifier output voltage a filter circuit is required.

Filter (C=1000µF): It is a device which passes dc component to the load and blocks ac components of the rectifier output. Filter is typically constructed from reactive circuit elements such as capacitors and/or inductors and resistors. The magnitude of output dc voltage may vary with the variation of either the input ac voltage or the magnitude of load current. So at the output of a rectifier filter combination a voltage regulator is required, to provide an almost constant dc voltage at the output of the regulator. The voltage regulator may be constructed from a Zener diode, and or discrete transistors, and/or integrated circuits (ICs). Its main function is to maintain a constant dc output voltage. However, it also rejects any ac ripple voltage that is not removed by the filter. The regulator may also include protective devices such as short-circuit protection, current limiting, thermal shutdown, or over-voltage protection.

TLP 250 DRIVER CIRCUIT: The main function of driver circuit is to amplify the signals. TLP driver circuit also provides isolation between the power circuits as well as the control circuit.TLP250 is more suitable for MOSFET and IGBT. The main difference between TLP250 and other MOSFET drivers is that TLP250 MOSFET driver is optically isolated. It means that input and output of TLP250 MOSFET driver is isolated from each other.

MICROCONTROLLER (ARDUINO MEGA2560): Arduino can sense the environment by receiving input from a variety of sensors and can affect its surroundings by controlling lights, motors, and other actuators. The microcontroller on the board is programmed using the Arduino programming language (based on Wiring) and the Arduino development environment (based on Processing). Arduino projects can be stand-alone or they can communicate with software running on a computer (e.g. Flash, Processing and Max MSP). The boards can be built by hand or purchased pre-assembled; the software can be downloaded for free. The hardware reference designs (CAD files) are available under an open-source license; you are free to adapt them to your needs. The Arduino Mega 2560 is a microcontroller board based on the ATmega2560. It has 54 digital input/output pins (of which 15 can be used as PWM outputs), 16 analog inputs, 4 UARTs (hardware serial ports), a 16 MHz crystal Oscillator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with a AC-to-DC adapter or battery to get started. The Mega 2560 is an update to the Arduino Mega, which it replaces. The Mega2560 differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the ATmega16U2 (ATmega8U2 in the revision 1 and revision 2 boards) programmed as a USB-to-serial converter.

N-CHANNEL MOSFET (IRF 840): It is the third generation power MOSFET with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. It is preferred for industrial applications where power dissipation levels is approximately 50 W. The low thermal resistance and low package cost contribute to its wide acceptance throughout the industry.

VOLTAGE REGULATOR (LM7805 and LM7812): Voltage regulators are commonly used in electronic circuits and provide constant DC output voltage for the variable input voltage. Voltage regulator 7805 IC is used in the design as the microcontroller operates on the regulated DC supply of 5V and 7812 regulator to the TLP250 driver circuit which works on 12V supply.

Sinusoidal pulse width modulatio: A sinusoidal pulse width modulation method is also known as triangulations, sub oscillation, sub harmonic method is very popular in industrial applications. In this technique a high frequency triangular wave is compared with the sinusoidal reference wave determining the switching instant. The modulating signal is a sinusoidal of amplitude Am, and the amplitude of triangular carrier wave is Ac, then the ratio m=$Am \div Ac$ is well known as modulation index. It is noted that by controlling the modulation index one can control the magnitude of applied output voltage and frequency of inverter. The block of sinusoidal pulse width modulation is given below Fig.

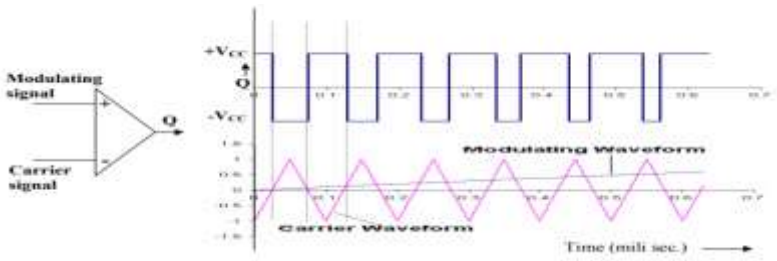


Figure 2 Schematic circuit for comparison of modulating and carrier signals.

Switching logic will be :
Vo = +Vdc ifVr>Vc
Vo = -Vdc if Vr<Vc

Where, Vr is the modulating sinusoidal signal, Vc is the carrier triangular signal, Vo is the rms output voltage of the inverter, Vdc is the DC link voltage, Modulating frequency = 50Hz and Carrier frequency = 10 KHz

V SIMULATION RESULT ANALYSIS

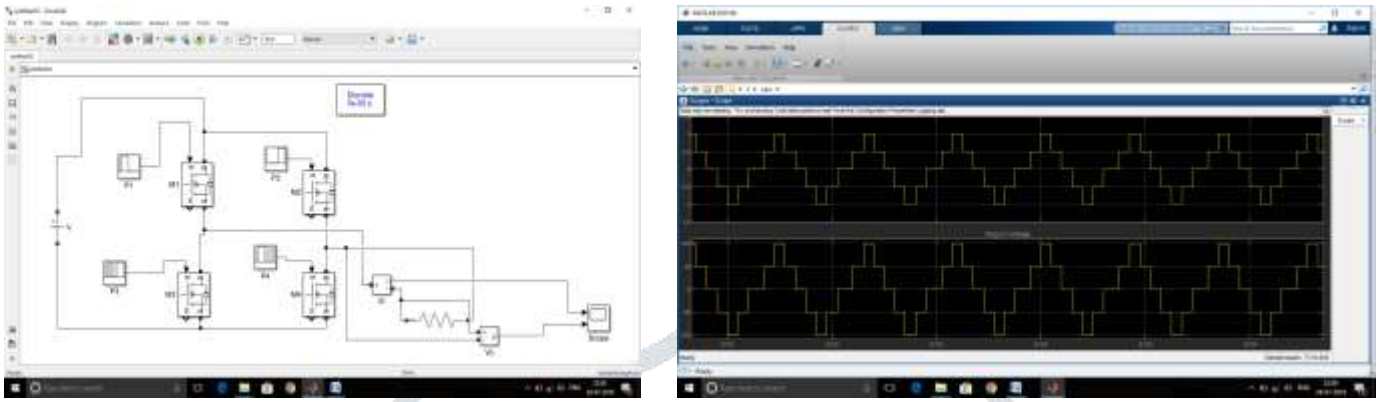


Fig. 3 Simulink model, output current and voltage waveforms of single phase full bridge inverter

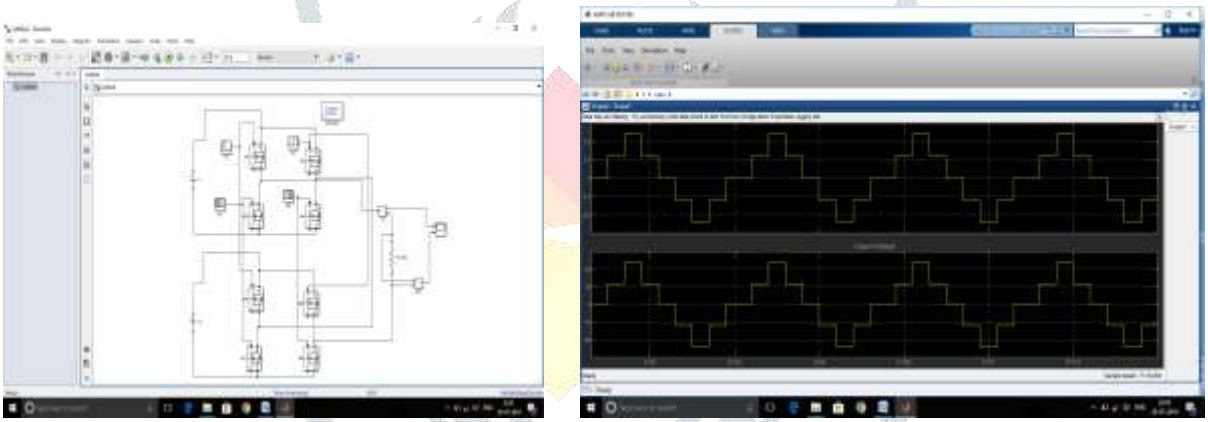


Fig. 4 Simulink model, output current and voltage waveforms of five level inverter using single phase PWM method with V=12V and V_1=12V

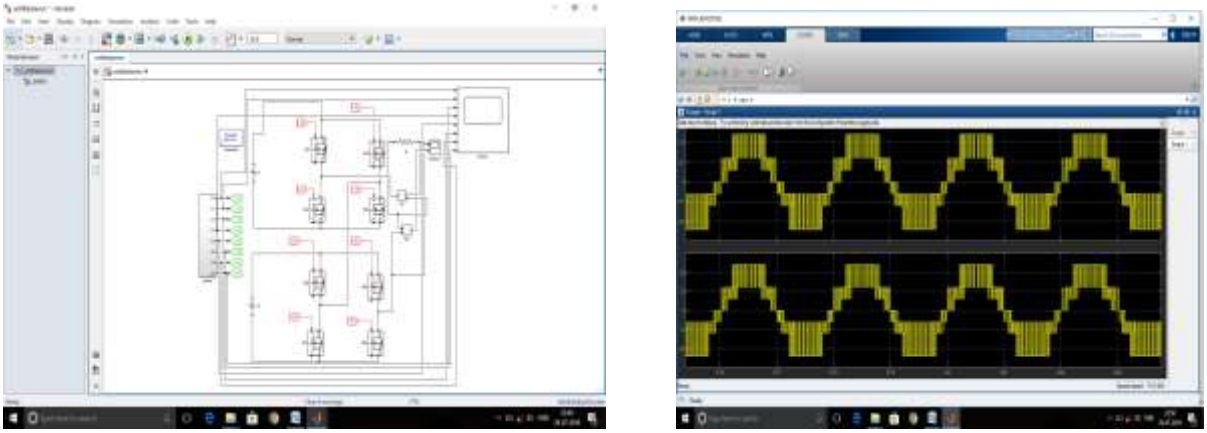


Fig. 5 Simulink model, output current and voltage waveforms of five level inverter using sinusoidal PWM method with V=100V and V_1=50V

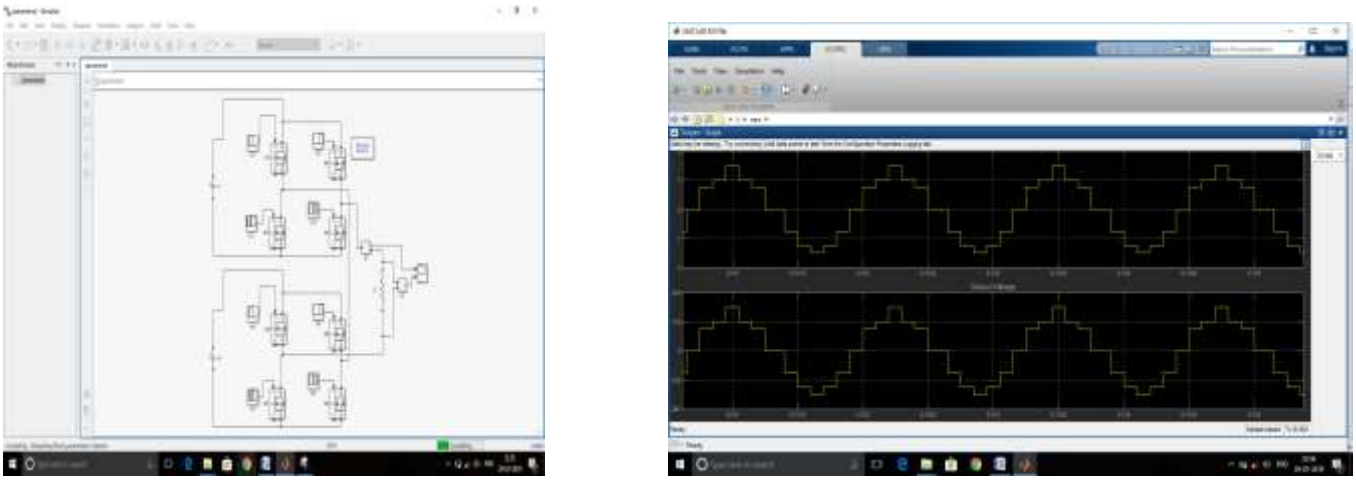


Fig. 6 Simulink model, voltage and current waveforms of seven level inverter using single phase PWM method with V=100V and V_1=50V

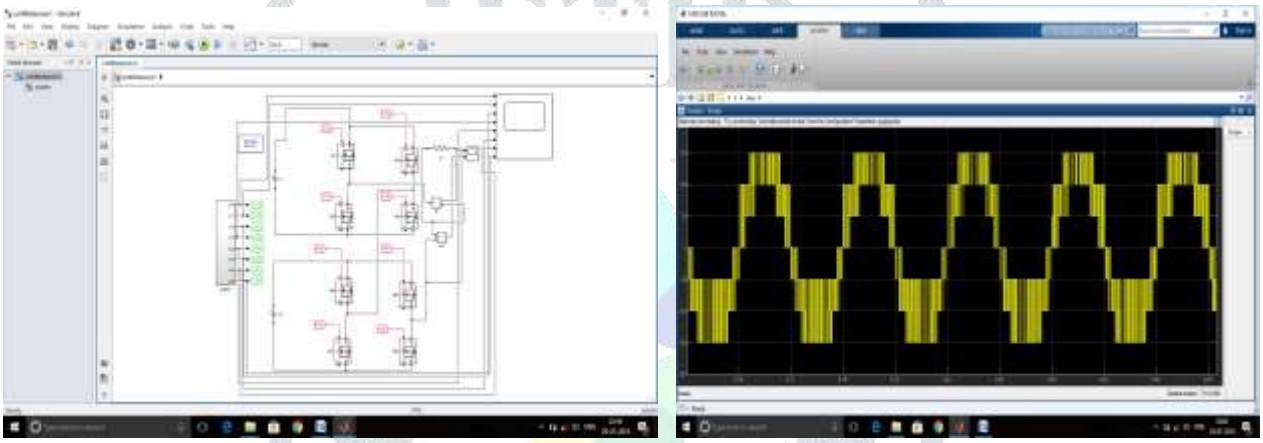


Fig. 7 Simulink model and voltage waveforms of seven level inverter using sinusoidal PWM method with V=100V and V_1=50V

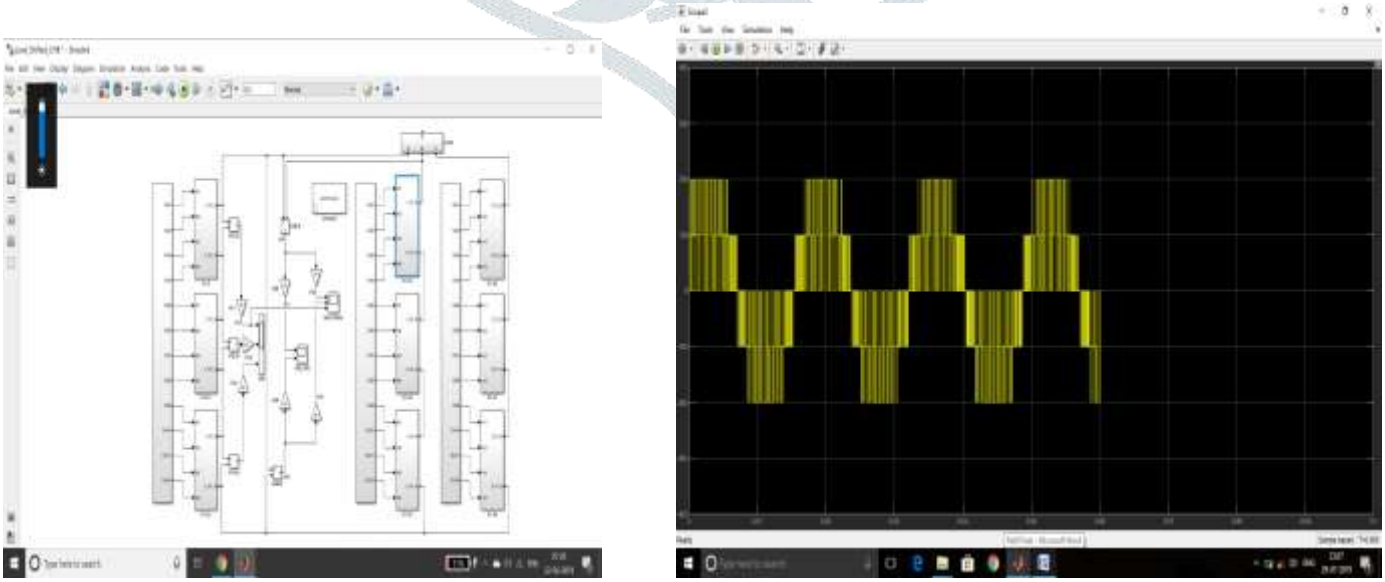


Fig. 8 Simulink model and output voltage waveform of five level inverter using level shifting PWM method

VI. MODES OF OPERATION FOR CASCADED H-BRIDGE FIVE LEVEL INVERTER:

Modes of operation:

According to the switching states of the MOSFET's used in the designed hardware for cascaded H-bridge five level inverter and they operate in different modes which are as follows.

Table 1 Switching table for cascaded H- bridge five level inverter

SL. NO	No of levels	Switching states / Output voltage	S1	S2	S3	S4	S5	S6	S7	S8
1	1 Level	V_{DC} =24V	1	0	0	1	1	0	0	1
2	2 Level	$V_{DC}/2$=12V	1	0	1	1	1	0	1	1
3	3 Level	0	0	0	0	0	0	0	0	0
4	4 Level	$-V_{DC}/2$= -12V	0	1	1	1	0	1	1	1
5	5 Level	$-V_{DC}$ = -24V	0	1	1	0	0	1	1	0

❖ **Complete circuit diagram of cascaded H-bridge five level inverter :**

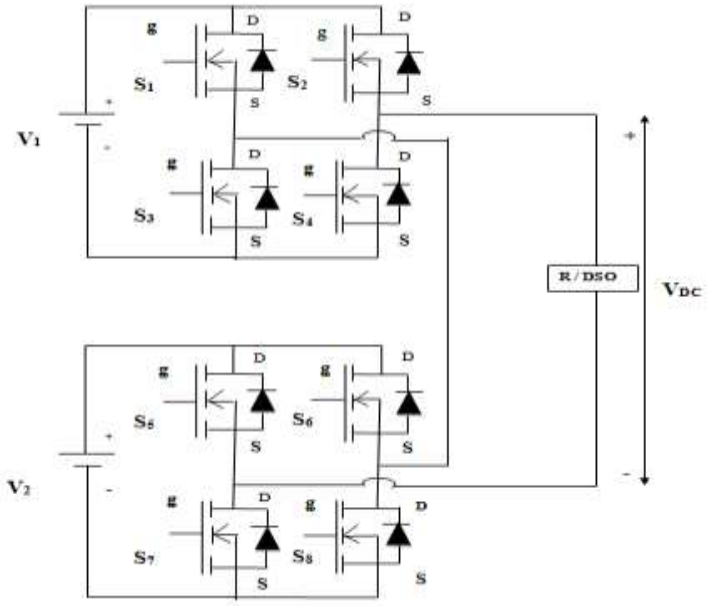


Fig. 9 Complete circuit diagram of cascaded H-bridge five level inverter

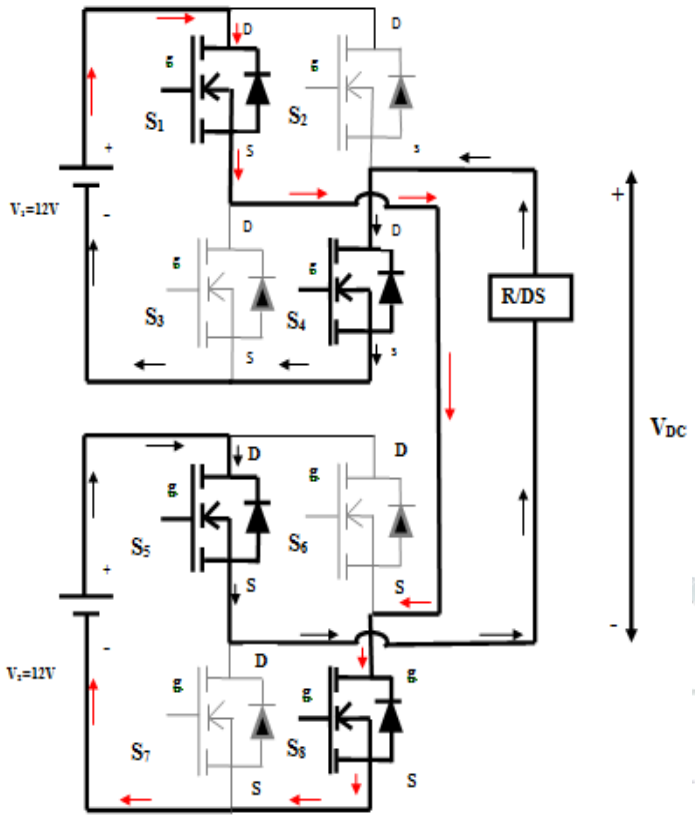


Fig. 10 Mode 1

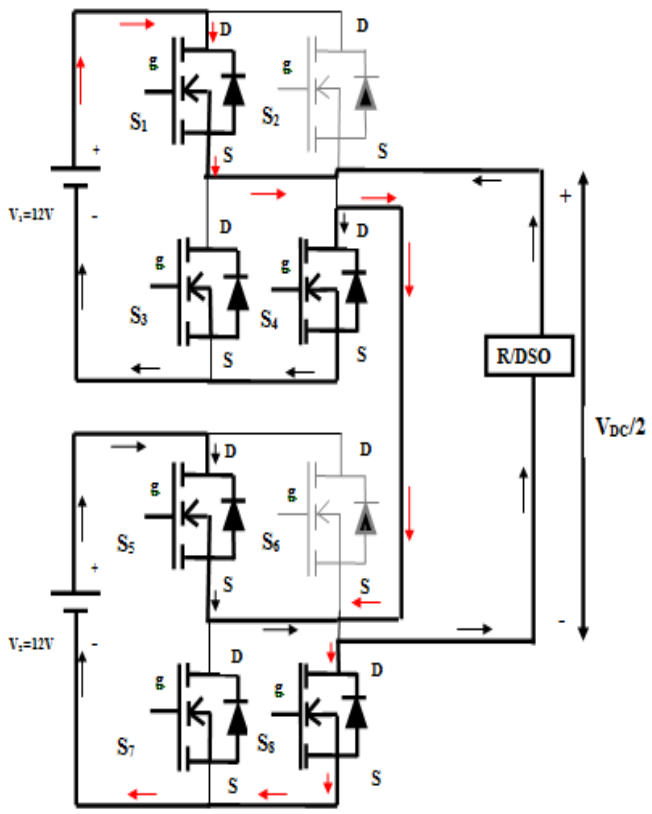


Fig. 11 Mode 2

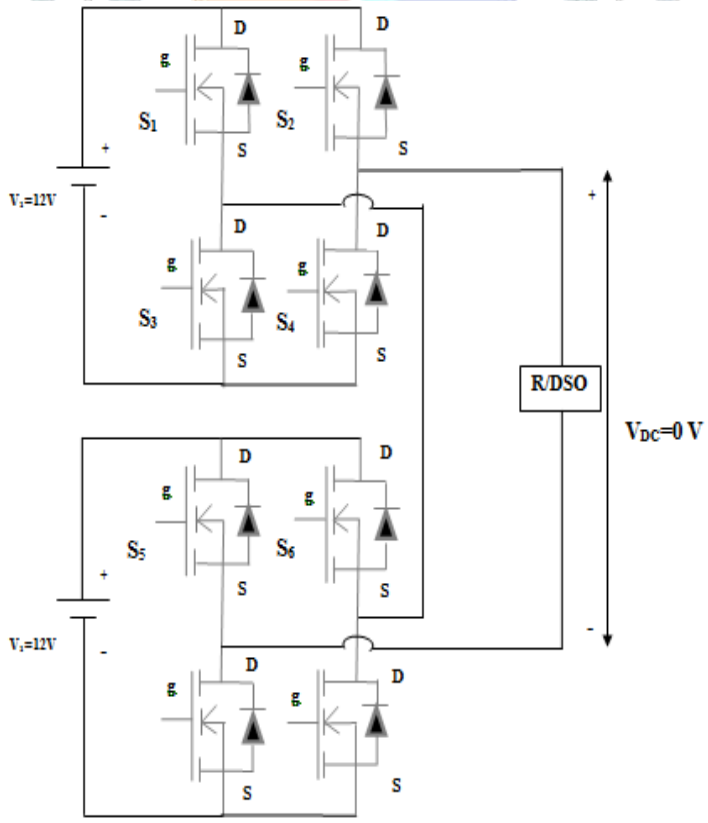


Fig. 12 Mode 3

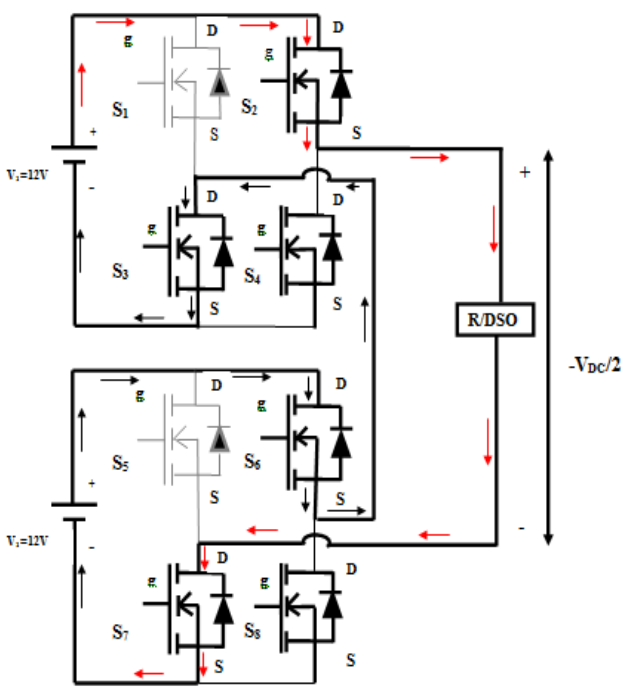


Fig. 13 Mode 4

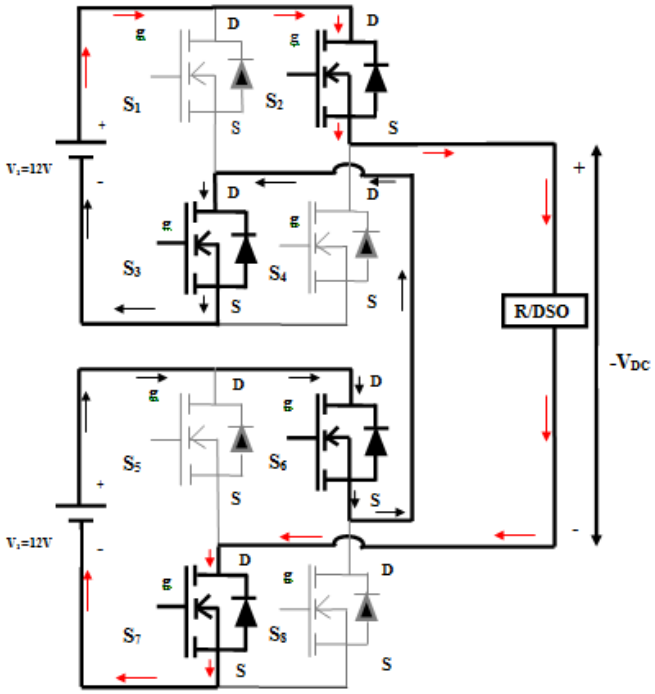


Fig. 14 Mode 5

VII. EXPERIMENTAL SETUP AND ITS RESULTS:

The hardware on cascaded H-bridge inverter is designed to obtain five different voltage levels with two separate DC sources employing sinusoidal pulse width modulation scheme resulted in to staircase waveform which is nearly sinusoidal in nature. Sinusoidal PWM technique is a modulation scheme where triangular waves are compared with reference sine wave to generate PWM switching pulses.

❖ EXPERIMENTAL SETUP

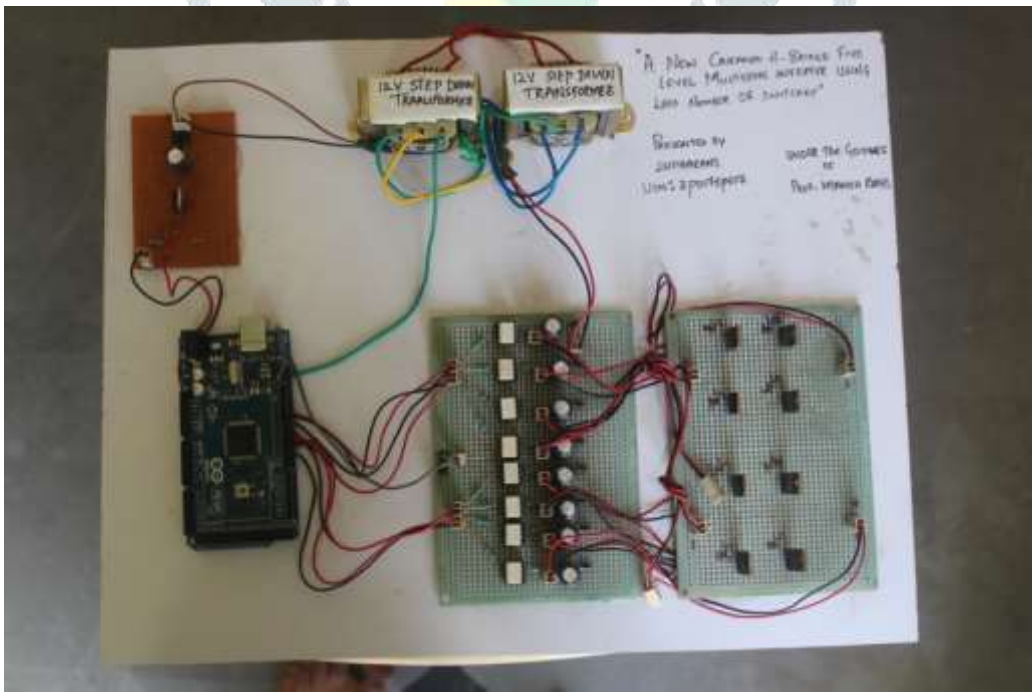


Fig. 15 Experimental setup of cascaded H -bridge five level inverter

❖ GENERATION OF PWM SIGNALS FROM ARDUINO MEGA 2560

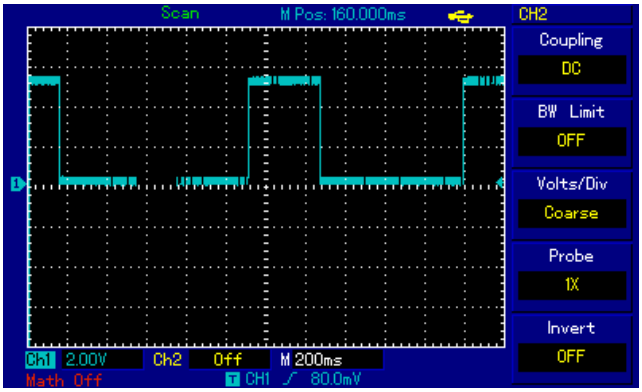


Fig.16 Generation of PWM signals for S_1 and S_5

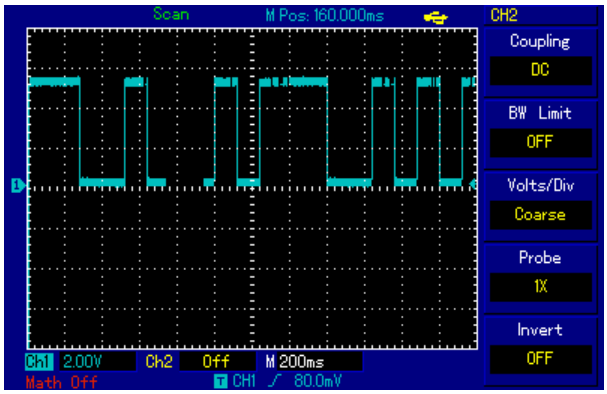


Fig.17 Generation of PWM signals for S_2 and S_6

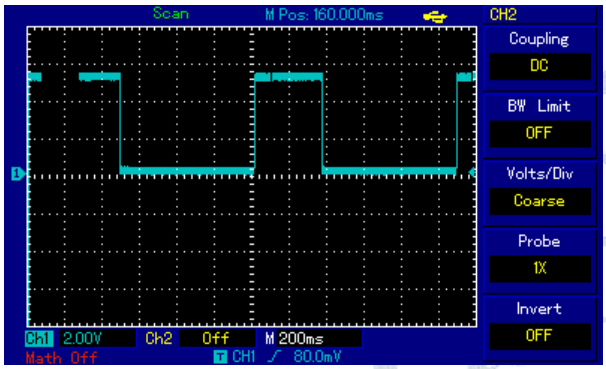


Fig.18 Generation of PWM signals for S_3 and S_7

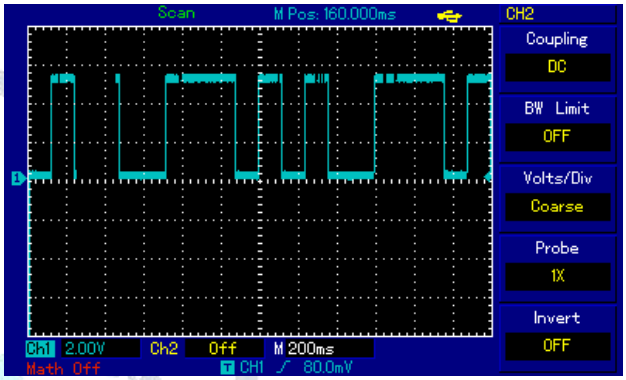
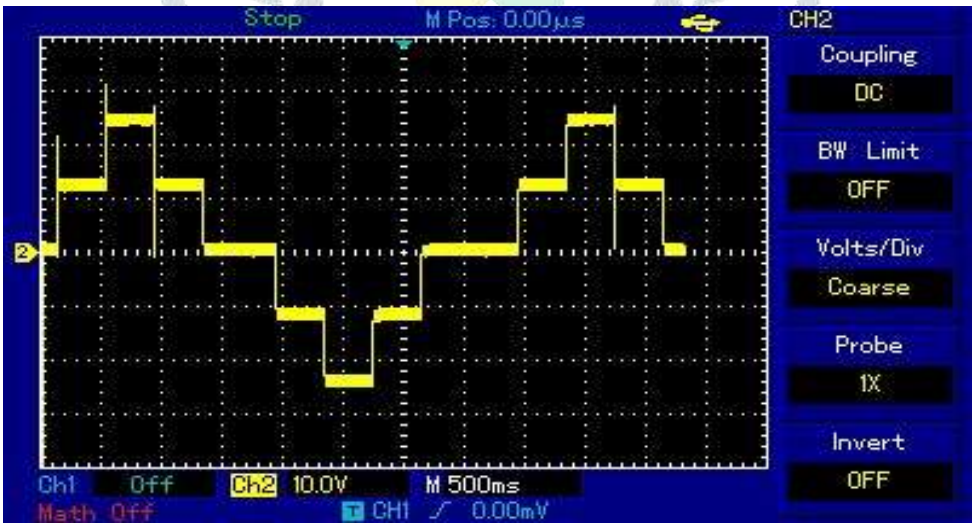


Fig.19 Generation of PWM signals for S_4 and S_8

❖ OUTPUT VOLTAGE WAVEFORM FOR CASCADED H-BRIDGE FIVE LEVEL INVERTER:



VIII. CONCLUSION

The developed hardware on cascaded H-bridge five level inverter using SPWM method has high quality output waveform compared to conventional direct current to alternative current inverter. The main advantage of the cascaded H-bridge inverter is less cost and weight compared with other type inverters. Moreover, the THD level is very less. Practically, with high THD value the output voltage is not possible. But the design of the five level inverter has better performance than 9 level inverters. Due to the increase in levels, the cost and weight is greatly increased. This method is well suited for industries drives. By having a filter circuit in a network, we can reduce the THD value. This circuit implementation decreases the usage of switches. The developed hardware is able to operate in both symmetrical and asymmetrical modes.

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