Design of 6LoWPAN module for IoT communication

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***Abstract*—IPV6 over low power personal area network is abbreviated as 6LoWPAN basically designed for high bandwidth infrastructure with mesh topology. The 6LoWPAN standard RFC 4944 was deployed by organization called Internet Engineering Task Force (IETF) which carries IP packets over IEEE 802.15.4 networks. This module is deliberated for low data rate communication (250kbps) of devices with short range distance (10m to 100m) having the highest degree of reliability. It can be operating in a point-to-point or point-to-multipoint network and also supports virtually illimitable number of nodes in a network. The 6LoWPAN module powered up by 3.3 V with Texas Instrument CC1310 microcontroller with frequency range sub-1 GHz. In 6LoWPAN module provides different low power modes to save energy in battery operated devices. This paper mainly focuses on power calculation for different mode like active mode, sleep mode, run mode, idle mode of 6LoWPAN module and Functional test for different peripheral interfaces on designed module. Schematic of each component in the 6LoWPAN is designed using software Cadence Redon 16.3 with tool PCB Allegro design entry. By using the design, we estimated the total input and output power required for each compound. Finally, total Power losses is calculated during the active mode of each component for 70% of efficiency.**

***Index Terms*—6LoWPAN, Sub-1GHz MCU, PCB, Functional test, Power loss, functional test.**

I. INTRODUCTION

Internet Protocol(IP) is a set of rules which is used for communication between two modules. This IP deals mainly with sensor networks. IPv4 and IPv6 helps in bringing up data delivery for local area networks and wide-area networks such as the Internet. 6LoWPAN defines IP version 6 (IPv6) over low data rate, low power radio networks (6LoWPAN) as typified by the IEEE 802.15.4 radio. 6LoWPAN is deliberated for low data rate communication (250kbps) of devices with very limited availability of resources. It defines the header compression mechanisms and encapsulation that allow IPv6 packets to be sent and received over IEEE 802.15.4 based networks The main advantages of IPv6 over IPv4 is large bit address, which provides 2 power 128 unique bit addresses. This large address space can be allotted to unique IP address for every wireless sensor device that could be connected to the Internet.

A typical 6LoWPAN network configuration setup is shown in Fig 1. Using various 6LoWPAN modules the Personal Area Network(PAN) is designed with mesh topology .Routing of IP packets in this topology is handled by the software stack apparent for the user. The network is communicate through via a border router to the local area network (LAN) and from LAN to a wide area network (WAN) such as the cloud. In this configuration setup, each module can be accessed from anywhere in the world with just its unique IPv6 address. These

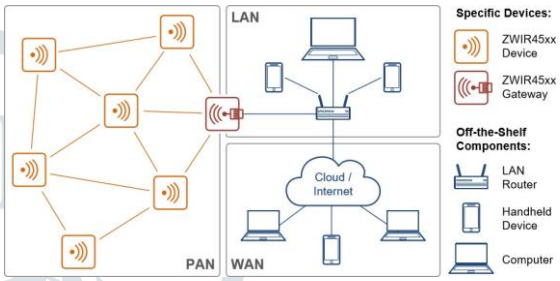

Fig. 1. Typical 6LoWPAN configuration Setup

type of networks can be easily unified into subsisting IT in- frastructure. standard agreeable usage of the Internet Protocol Security (IPSec) convention gives verified correspondence and the Internet Key Exchange Protocol adaptation 2 (IKEv2), which empower profoundly secure hub to hub correspondence inside the scope of 10m to 100m. The module provides perfect proprietary RF solution in the frequency of sub1 GHz or 2.4Ghz for wireless sensor network applications such as smart grid, smart home and health monitoring etcand it transmit the serial data over small distances with the highest degree of reliability.

The 6LoWPAN module powered up by 3.3 V with TIs CC1310 is a sub-1 GHz microcontroller and It gives a rich arrangement of GPIO and peripheral interfaces. It consists of up to 128kB of internal flash, 8kB of cache SRAM and 20KB general purpose SRAM are available for applications. Whip antenna is compatible with 6LOWPAN module with receiver sensitivity -110dBm. Balanced and unbalanced modu- lator(BLUN) used to convert unbalanced signals into balanced signals, and balanced signal is feed into RF core in MCU with 50-ohm impedance. In 6LOWPAN module diverse low power modes are given to spare vitality in battery-worked gadgets. This module provides higher level radio properties without need of complex external RF design. In this paper we are going discuss on design of 6LOWPAN module (PCB board) using cadence redone 16.3 and generated Netlist file, Bill of Material and ERC file. Power calculation is done for different modes of operation for 6LOWPAN module and Functional test is done for different peripheral interfaces in the proposed module.

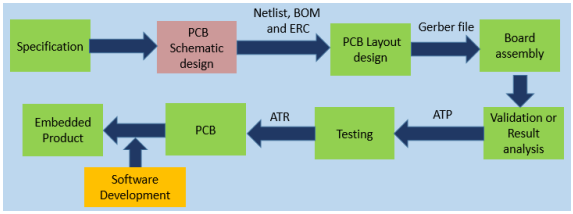

Fig. 2. Embedded hardware design flow

II. RELATED WORK

Jorge E. Higuera and Jose Polo proposes the 6LoWPAN using IEEE 1451 standard in IEEE 802.15.4 wireless sensor network. Using the data type they designed the 6LoWPAN physical-layer transducer electronic data sheet (PHY-TEDS) and redefine the header compression. Their analysis shows that there is a reduction in memory size by 48% in the PHY-TEDS and 25% in the meta-TEDS.Design of 6LoWPAN is implemented for automatic environmental monitoring system for real time application[1].

A lightweight 6LoWPAN gateway designed based on Contiki operating system for both hardware and software. A complex experiment work done on 6LoWPAN , in which their verified gateway's capability of accessing the Internet. they analyzed performance like average network delay and jitter. The experimental results shown on proposed gateway designed and observed the communication between 6LoWPAN networks and Internet, also they discussed about network adaptability and stability.

The proposed CETIC-6LBR is open source, Contiki OS based, and good support by popular repositories. The main goal of design and im plementation of 6LoWPAN border router with an embedded Web server on Beagle Bone Black (BBB) module and implemented connectivity between 6LoWPAN devices to the internet using IPV6 and IPV4 protocal.

According to the previous survey, it is understood that there is a need for power analysis of low power devices and functional test for different peripheral interfaces in order to maintain adaptability and provide new features that interface between device with cloud. hence a new 6LoWPAN module is proposed here for IoT low data communication using TIs CC1310 MCU.

III. METHODOLOGY

Embedded system is integration of hardware and software parts. In fig 2 is shown the hardware design flow for 6LoWPAN module. Specification and component selection is done as per the requirement. Schematic diagram conveys the electrical connectivity between different active and passive electrical components like resistors, capacitors, Integrated circuits IC. Schematics are readable and understandable format about the functionality and connectivity between different components. Schematic Design is done as per the selected hardware components using Cadence radon 16.3 allegro design entry tool. Output of the schematic is netlist file, it consists I/O information and connectivity of each node in the design. ERC file shows the violation of the design and BOM consists of detailed information regarding PCB design such as components used, quantity and manufactures of each component used in the 6LoWPAN. PCB layout design is mechanically supports and electrically connects electronic components or electrical components using conductive tracks, pads and other features etched from one or more sheet layers of copper laminated onto and/or between sheet layers of a non-conductive substrate. Components are generally soldered onto the PCB to both electrically connect and mechanically fasten them to it. Output of the layout design is Gerber file; it consists of detailed information of electrical connectivity and mechanical support for PCB and it feed for assembly. Finally assembled board tested and flashed using smartrf programmer tool and output is displayed using CRO and PuTTY emulator.

IV. IMPLIMENTATION

A. *Architecture of 6LoWPAN RF module*

Fig 3 shows the block diagram of 6LoWPAN RF module, it mainly deliberated to transmit and receive the signal from the wipe antenna. This RF module consists of following components:

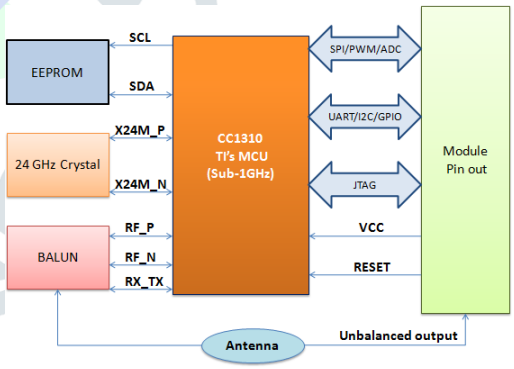

Fig. 3. Block diagram of 6LoWPAN RF module

- *CC1310*: It is a power full Arm Cortex M3 microcontroller unit it works up to 48MHz recurrence and it comprises of 32KB, 64KB, and 128KB of In-System Programmable Flash and 8KB of SRAM for broadly useful Cache memory.it supports OTA(over the time) for software upgradation and JTAG for debugging. CC1310 consists of rich rest of 30 pin GPIOs with 7mm 7mm

RGZ VQFN4 package. Supported peripherals such as 12 Bit ADC, PWM, four 32 bit timers, real time clock, integrated temperature sensor, programmable current source and serial interfaces such as I2C, I2S, SPI, UART etc. This MCU powered up by 1.8V to 3.8 V, while communication RX and TX current consumption 5.4mA and 13.4mA respectively with -110dBm receiver sensitivity. Power analysis shown in the results section[4].

- *EEPROM*: It mainly deliberated to store the MAC address in order to maintain uniqueness between each module in the wireless network. It is powered up by 1.7 V to 3.6 V and it consists of 128-byte organization. EEPROM compatible with I2C interface with 400KHz fast mode operation. In I2C SDA and SCL is pulled up by 10K ohm resistors using below formula [3].

$$RPUP(max) = tR(max)/0.8473 \times CL \quad (1)$$

$$RPUP(min) = VCC - VOL(max)/IOL \quad (2)$$

Where tR(max) is the rise time (100ns), CL is load capacitance(100pF), VOL is 0.4V and IOL is 2.1mA recommended.For these values RPUP(max) and RPUP(min) is calculated, when VCC is 3.3V.

- *BALUN*: It mainly deliberated to balance the unbalanced signal received from the wipe antenna.it operates in the range of 860 MHz to 928MHz with 50 ohm unbalanced impedance. Typical insertion loss 1.8dB(max), return loss 9.5dB(min), phase difference 180±15 °C, amplitude difference 20dB (max) and power capacity 2 W(max).
- *Crystal oscillator*: Nominal frequency range 8MHz to 58MHz with load capacitance 20pf and its Operating temperature -40 °Cto 80 °C(proposed module 24MHz). Using above components the (designed) 6LoWPAN RF module has been designed using cadence radon 16.3 allegro design entry tool .

B. *Architecture of 6LoWPAN EVK module*

6LoWPAN evaluation kit (EVK) consists of peripherals and Connectors. EVK designed to test the functionality of different peripheral interfaces and devices. 6LoWPAN EVK is powered up by 3.3 V using USB through Buck regulators. Connectors for USB, sensors and antenna, switches for reed and reset, jumpers and LED are mounted on PCB using schematic design.

In the fig 4 shows block diagram of 6LoWPAN EVK module. The board is powered up by using USB connection and CC1310 MCU, debugger MCU and sensors are powered up by output of the buck regulators as shown. First flashing is done for debugger MCU using USB and later CC1310 is Flashed through JTAG using Smartrf programmer tool. Whatever data coming from the sensor, is processed and transmit and receive the date using wipe antenna. Each peripheral interface is tested and shown in the result section.

V. RESULTS

In this section we show power calculation and functional test for different peripheral interfaces.

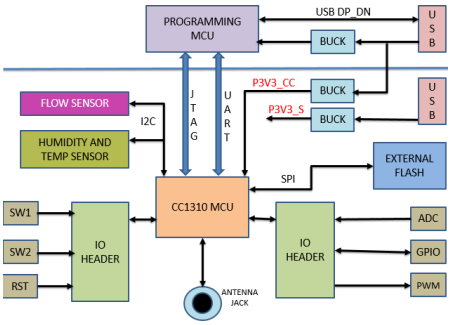

Fig. 4. Block diagram of 6LoWPAN EVK module

A. *Power calculation for 6LoWPAN module*

6LoWPAN module operates different modes such as active mode, idle mode, shutdown mode and sleep mode for power saving purpose. In this paper we estimated total input and output power for different modes of the operation for each component and finally total power loss is calculated for 6LoWPAN module, when it is in active mode using below equations.

$$Outputpower = Vin(3.3V) \times current(I) \quad (3)$$

$$Efficiency(70\%) = Outputpower/Inputpower \quad (4)$$

TABLE I
CC1310 AND INTERNAL EEPROM IN ACTIVE MODE

	P3V3	Unit
CPU	32.318	mA
EEPROM	1.5	mA
Total Current	33.818	mA
Output Power	111.5994	mW
Input Power	159.427714	mW

TABLE II
CC1310 AND INTERNAL EEPROM IN IDLE MODE

	P3V3	Unit
CPU	0.57	mA
EEPROM	0	mA
Total Current	0.57	mA
Output Power	1.881	mW
Input Power	2.6871	mW

TABLE III
CC1310 AND INTERNAL EEPROM IN SHUT DOWN MODE

	P3V3	Unit
CPU	0.000185	mA
EEPROM	0	mA
Total Current	0.000185	mA
Output Power	0.0006105	mW
Input Power	0.00087214	mW

TABLE IV
CC1310 AND INTERNAL EEPROM IN STAND-BY MODE

	P3V3	Unit
CPU	0.0015	mA
EEPROM	0.0008	mA
Total Current	0.0023	mA
Output Power	0.00759	mW
Input Power	0.010842	mW

TABLE V
DEBUGGING/PROGRAMMING IC IN ACTIVE MODE

	P3V3	Unit
SRAM loop	45	mA
Flash loop	39.1	mA
USB	4	mA
Total current	88.1	mA
Output Power	290.73	mW
Input Power	415.3286	mW

TABLE VI
DEBUGGING/PROGRAMMING IC IN SLEEP MODE

	P3V3	Unit
Total current	29.8	mA
Output Power	98.34	mW
Input Power	140.48	mW

TABLE VII
DEBUGGING PROGRAMMING IC IN DEEP SLEEP MODE

	P3V3	Unit
Total current	24.1	mA
Output Power	79.53	mW
Input Power	113.6143	mW

TABLE VIII
EXTERNAL EEPROM IN ACTIVE MODE

	P3V3	Unit
Write	6	mA
Read	4	mA
Total current	10	mA
Output Power	33	mW
Input Power	47.14	mW

TABLE IX
EXTERNAL EEPROM IN STAND-BY MODE

	P3V3	Unit
Total current	8	μA
Output Power	0.0264	mW
Input Power	0.037714	mW

TABLE X
EXTERNAL EEPROM IN DEEP POWER DOWN MODE

	P3V3	Unit
Total current	0.2	μA
Output Power	0.0006	mW
Input Power	0.000942	mW

TABLE XI
TOTAL POWER CALCULATION FOR 6LOWPAN MODULE IN ACTIVE MODE

	Current *mA*	Output Power *mW*	Input Power *mW*	Power Loss *mW*
CC1310 and *Internal EEP ROM*	33.818	109.49	156.41	46.923
Debugging IC	88.1	290.73	415.32	124.596
External *EEP ROM*	10	33	47.14	14.142
Total	131.91	433.22	618.87	185.661

Above tables 1 ,2 3 & 4 show the power calculation for CC1310 and internal EEPROM, table 5,6 & 7 shows the programming/ debugging IC power calculation, table 8,9 & 10 shows the power calculation for external EEPROM and table 11 shows the total power calculation for each component present in the 6LoWPAN module during active mode. Here we assumed 70% of efficiency to calculate total power loss for proposed module using below formula.

$$Eff = 1 - powerloss/inputpower \quad (5)$$

B. Functional test for Peripheral interfaces

Functional test for different peripheral interfaces is done in order to maintain the adaptability for wireless sensor environment. Fig 5 shows the PWM output for 10% duty cycle, where T_{ON} is 100μs and T_{OFF} 900μs. In Fig 6 and Fig 7 the I2C read and write operations are displayed. Here the waveform gives information on layered I2C protocol. The sensor reads the data from the environment and it communicates with CC1310 MCU using I2C as shown in fig 8. Fig 9 shows the GPIO Toggling with 3.3V input voltage. Fig 10, Fig 11 and 12 show the UART, SPI and ADC interface respectively, using PuTTY emulator.

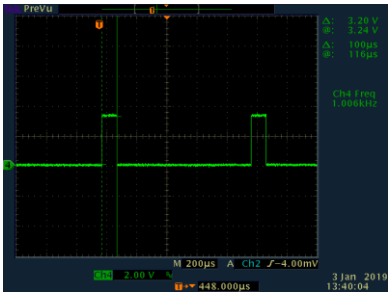

Fig. 5. PWM output for 10% duty cycle

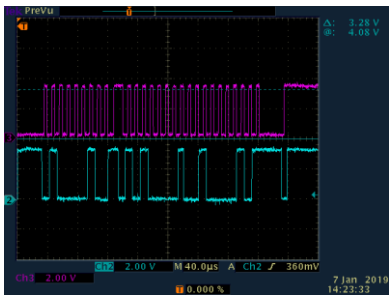

Fig. 6. EEPROM I2C read operation

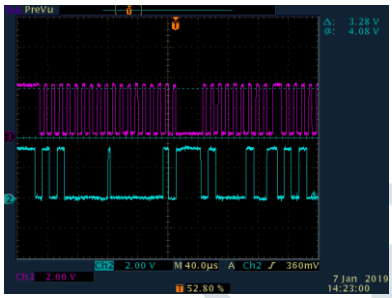

Fig. 7. EEPROM I2C write operation

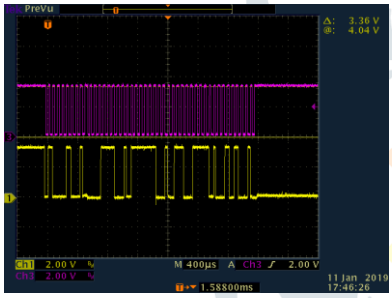

Fig. 8. Sensor I2C read operation

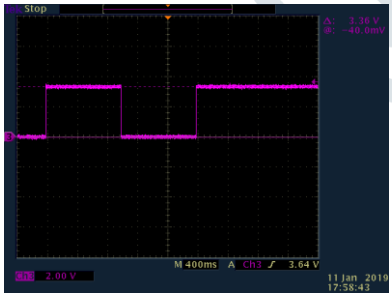

Fig. 9. GPIO Toggling

Fig. 10. UART test using PuTTY

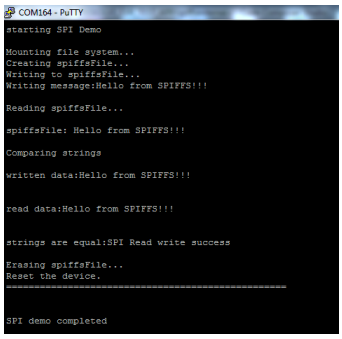

Fig. 11. SPI test using PuTTY

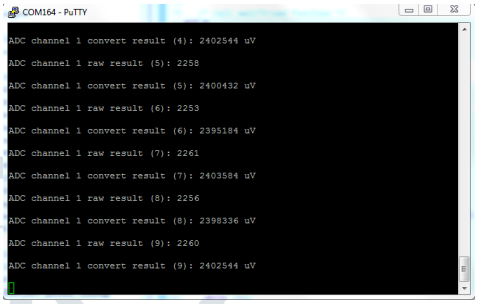

Fig. 12. ADC test using PuTTY

CONCLUSION

6loWPAN mainly deliberated to Low power, Low data rate and short range of communication. In this paper we focused on power calculation and functional test for proposed module. Power calculation is done for different mode of the operation, here input/output power and power loss for proposed 6LoWPAN is estimated. Functional test is done for different interfaces used in the schematic diagram and output is displayed using CRO and PuTTY emulator after the flashing by smartrf programming tool.

REFERENCES

[1] Jorge E. Higuera, Student Member, IEEE, and Jose Polo,"IEEE 1451 Standard in 6LoWPAN Sensor Networks Using a Compact Physical-Layer Transducer Electronic Datasheet",IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 60, NO. 8, AU-GUST 2011.
[2] Zhao Honggang, Shi Chen and Zhai Leyu, Design and Implementation of Lightweight 6lowpan Gateway Based on Contiki, IEEE trans,2018
[3] Praveen Kumar Kamma, Chennakeshava Reddy Palla, Usha Rani Nelakuditi and Ravi Sekhar Yarrabothu, "Design of 6LoWPAN Border Router and implementation", IEEE IOT journal, December 2016..
[4] Internal contents from Tessolve Semiconductor PVT LTD.
[5] Internal contents from Taxes Instruments.
[6] Jorge Higuera, Jose Polo, Understanding the IEEE 1451 standard in 6loWPAN Sensor Networks IEEE Trans,2009.
[7] Yannis Mazzer and Bernard Tourancheau "Comparisons data packets and Implementations of 6LoWPAN on Wireless Sensor Networks", Third International Conference on Sensor Technologies and Applications, July 2009.
[8] Dae In Choi, Jong tak Park, Su Yeon Kim and Hyun K Kahng "IPv6 global connectivity Improvement for 6LoWPAN", 13th International Conference on Advanced Communication Technology,2011.
[9] Shen guo, Wenpeng luan , Xueyuan su, The Design of a Remote Meter Acquisition Module Based on 6LoWPAN,China International Conference on Electricity Distribution, 10-13 Aug, 2016.