LOW POWER AND HIGH SPEED 12T SRAM USING HALF-VDD PRECHARGE

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Abstract: In this paper a new 12T static random access memory cell having single ended decoupled read-bit line (RBL) for low power operation and delay reduction is proposed. The RBL is precharged with the 50% of cell's supply voltage and it can be charge and discharge based on the data stored in the SRAM cell. An inverter, driven by the complementary data node (QB), connects the RBL to the virtual power rails through a transmission gate during the read operation. The RBL charges towards the supply voltage for read '1' operation and it discharges toward the ground for the read '0' operation. During the cell write operation virtual power rails have the same value of the RBL precharging level and are connected to true supply levels only during the read operation. Due to the dynamic control of virtual rails significantly reduces the RBL leakage. The proposed 12T cell in a commercial 90 nm technology is 1.37× the delay of 10T and reduces the read power dissipation by 20% than that of 10T SRAM cell.

Index Terms **- read bit line, low power, SRAM cell, read static noise margin**

I. INTRODUCTION

The power consumption is a major concern in VLSI chip design of a battery operated system [1]. SRAM plays a critical role and consumes a significant amount of power in almost every SoC. With ever increasing scaling of integration, the transistor and metal interconnection geometry is supplemented by increasing random threshold (Vt) variation and increased wire routing resistance and capacitance variation in advanced technologies. Such variation degrades SRAM performance and its minimum operating voltage. As a key tactic toward power saving, near-threshold SRAM design has been widely used in SoC design. Lowering the supply voltage is the quadratic effect on the dynamic energy power consumption. The most important factors to consider in the design of SRAM in modern nanometer technologies are the [4]: 1) read stability; 2) write stability; 3) cell supply reduction; 4) power dissipation; 5) leakage currents;

Reduction of the supply voltage is the most straightforward technique to reduce the active power dissipation. However, 6T SRAM power supply cannot be reduced aggressively due to its read static noise margin (RSNM) degradation. Many SRAM cell have been proposed that improve RSNM, including single ended (SE) 8T [6], [8] and 10T [12], [13]. Also, numerous SRAM assist techniques have been described in the literature as a cost-effective method to increase the write margin, and lower the leakage power dissipation compared to bitcell transistor upsizing or operating the memory array at a higher supply voltage [5]. A 10T cell in [12] uses virtual ground rail for read port to achieve lower BL leakage and differential.

II. EXISTING SRAM CELLS

The conventional 6T SRAM cell structure is shown in the Fig.1. It is composed of two cross-coupled inverters (M1-M4) with two access transistors (M5, M6) connected to complementary bit-lines (BL, BLB). Both access transistors are connected to word line (WL) to perform the access write and read operations through the bit lines. There are three operating modes in SRAM [2]: standby/Hold, read and write. Each mode can define its own operating margin. When the cell is in the standby, its word line (WL) is connected to ground. In order to hold its data properly, the cross-coupled two inverters in the cell must sustain bi-stable operating points.

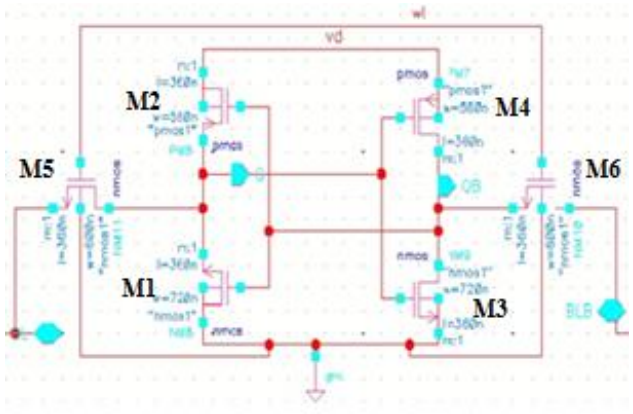

Fig. 1. Conventional 6T SRAM Cell

In write mode, bit-lines are driven to complementary voltage levels through a write driver. Then, with WL held high the data on bit-line written to the internal storage node of the bit cell. In read mode the bit-lines are initially precharged to VDD. Then with word-line is selected (VDD) bit-line discharges via M6 and M3 (node Q=0), so that differential voltage develops across the bit-lines [3]. This differential voltage should be large enough for a sense amplifier to detect the state of the cell. To avoid the read disturb, cell ratio, i.e., ratio of strength of the pull-down transistor (M1/M3) to that of the access transistor (M5/M6), should be sufficiently large.

Cell ratio= M1/M5 (large)

Pull up ratio, i.e., ratio of strength of the access transistor (M5/M6) to that of the pull-up transistor (M2/M4) should be sufficiently large to ensure a proper write operation.

Pull up ratio=M5/M2 (large).

In essence, 6T SRAM has conflicting read and write requirements [5] and transistor sizing cannot be done independently. Also, 6T has inherit read static noise margin problem as the read current passes through the cell internal node [7] and it further degrades with VDD scaling [8]. Also, being considered as baseline design, 6T has overall a higher power dissipation, and higher BL leakages, as the low power techniques employ a certain mechanism to lower the dynamic power dissipation. Many alternative bit cells and techniques have been proposed in the literature to improve SRAM cell stability, reduce the leakage currents and achieve low power operation and high speed compared with the conventional 6T SRAM cell design.

An 8T SRAM cell adds a separate 2T read port, shown in Fig. 2, and it essentially resolves the problem of read stability. Internal nodes are isolated from the read path and thus a high read static noise margin is achieved. Also, sizing of 8T read port can be done individually without disturbing the cell write operation.

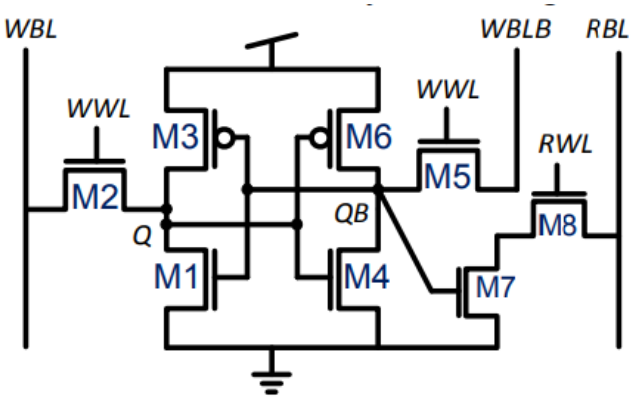

Fig. 2. Conventional 8T SRAM Cell

Thus, the 8T SRAM cell still has the same dynamic power dissipation as of 6T SRAM due to the higher differential voltage requirement [9]. Also, the differential voltage needs to be developed in the same time, to provide similar performance. Thus, the read port of 8T is sized wider to provide higher Iread, which exhibits higher RBL leakages.

SE 9T SRAM [11] uses a 3T read port and it effectively stacks the M2 between M1 and M3 to reduce the RBL leakage. Write performance and dynamic power dissipation of this cell is the same as 8T, however, speed is degraded compared with 6T and 8T cell due to 3T read path.

Another state-of-the-art 9T SRAM cell [10] uses a 3T read port [10]. It provides the leakage current to the replica bitline through M9, to compensate the BL leakage when the replica bitline is stay at a VDD level but reduces due to the current leakage in the SRAM cell. The 10T SRAM cell improves the sensing time and delivers better performance due to adding of two transistors (M9-M10) in the cell read path. But, its dynamic power is the same as 6T and overall static power dissipation is increased.

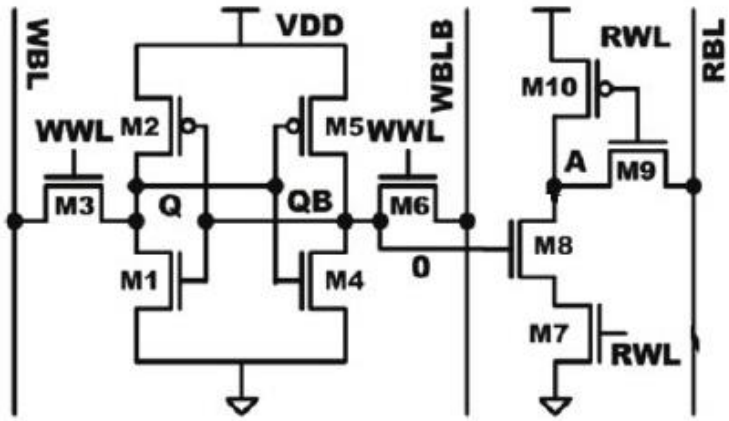

Fig.3. 10T SRAM cell

The Fig.3. shows the existing 10T SRAM cell, due to the single-ended read operation, it needs add another line that refer to this line as RBL. It is precharged to supply voltage levels (VDD) before beginning of the read operation. In the read operation, the wordline voltage (WL) is set to zero and the read wordline (RWL) is set to VDD. One main advantage of separating the read and write wordlines and bitlines is that the memory using this structure can have distinct read and write ports [1]. Using M7-M10 makes it possible to perform the read operation while the bitlines are isolated from the storage nodes improving the read static noise margin. It should be noted that M10 has been added to reduce the leakage current (static power). In the existing 10T SRAM has drawback of the decreased bitline swing which reduces the noise immunity of the cell. This problem can be overcome by using the proposed 12TSRAM Cell.

III. PROPOSED SRAM CELL

In the proposed SRAM cell presents a 50 % of supply voltage precharge and charge recycling technique for low power read operation. In the proposed cell a four transistor (4T) read port is implemented. Read bitline (RBL) is charged and discharged through the read port according to the state of stored bit. Read port is powered by virtual power rails that run horizontal and are shared by the cells of a word. The dynamic control of read port power rails reduces the RBL leakage substantially.

The proposed SRAM cell structure is shown in Fig. 3. Storage nodes Q and QB are comprised of transistors M1 through M4. More specifically, transistors M1 through M4 are arranged as a pair of inverters cross-coupled with each other. Transistors M7 through M10 comprise supply switches defined as two pairs of PMOS devices, such that each pair of PMOS devices have source terminals coupled to the supply voltage and drain terminals coupled to one of the two inverters. Additionally, a gate terminal of a single supply transistor is coupled to a write word line. Write access switches are comprised of transistors M5 and M6 as the conventional 6T and 8T SRAM cells are. These six devices—M5 through M10—relate write operation. Two NMOS devices M11 and M12 form a read port as in the conventional 8T SRAM cell12T SRAM is fully operated in static mode during read and write operation.

Read operation is conducted through devices M11 and M12 as shown as in a conventional 8T SRAM cell, the storage node QB is decoupled from the read bit lines RBL by device M11. In this case, M11 is turned on. When RWL is enabled, a path from RBL to virtual ground develops transparent and virtual ground is driven to ground by a driver circuit. Once this path is clear, charges on the floating bit line, i.e. replica bitline begin to be discharged through the read path. This process will give rise the accomplishment of read operation. After the read operation completion, read word line is disabled and read bitline is precharged to supply voltage levels. While virtual ground is driven to supply voltage, due to this the leakage, lack of differential voltage between replica bitline and virtual ground can be reduced when the 12T SRAM cell is connected to the unused word line. It brings about more rows of cells shared in bit lines since the leakage has been an obstacle increasing the number of rows of cells.

The write operation of the 12T SRAM cell is the key feature in the cell design. Device M5 to M10 six devices in total are related to write operation. The basic principle is to make an SRAM cell operate in static mode without charge contention.

The proposed 12T bit cell intensely improves the cell write margin by reducing the charge conflict due to the feedback structure of an SRAM cell. Its distinctive structure allows reliable operation during writing by blocking the power supply route. Since there is no charge contention, no sizing constraint exists.

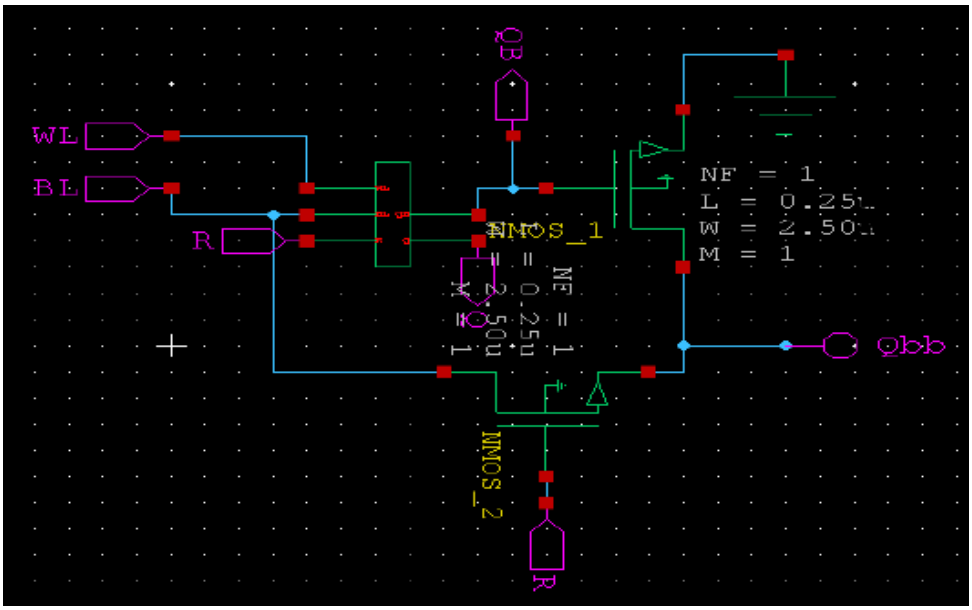

Fig.4. Proposed 12T SRAM cell

IV. RESULTS AND DISCUSSION

This section provides the simulation analysis of the proposed SRAM cell. It estimate the impact of the SRAM cell on the power dissipation and delay during the SRAM cell read operation. The schematic of the SRAM cell is designed and implemented by using schematic editor Cadence Virtuoso and Simulation has been done in 90 nm technology with a power supply of 1V. The Fig.5 shows the simulation results of proposed SRAM cell read operation at 50% supply voltage.

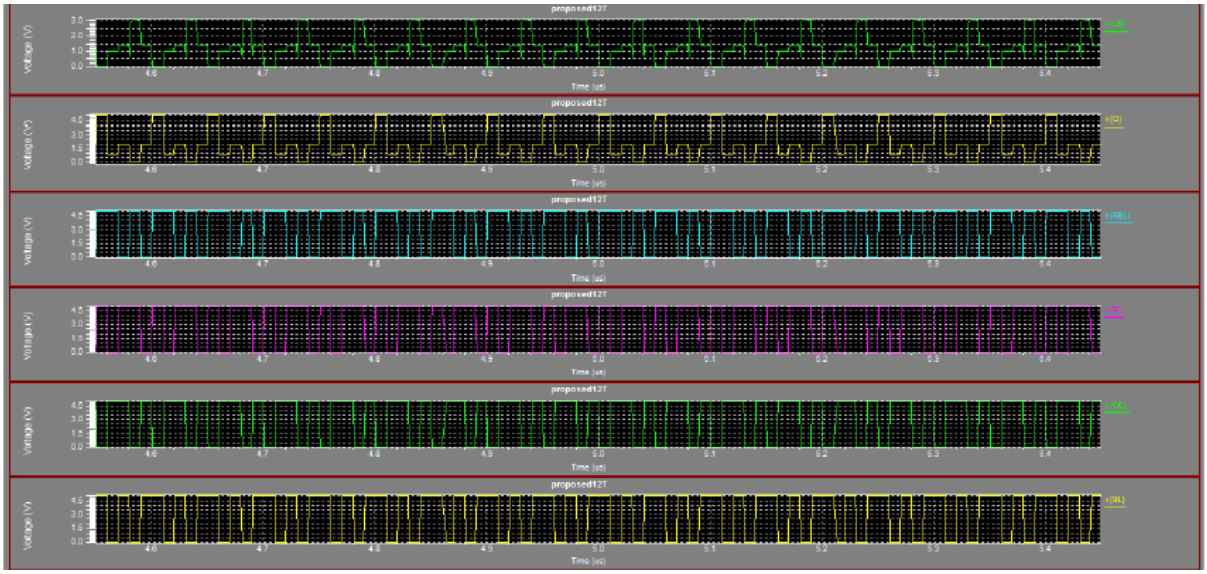

Fig.5. Simulation results of SRAM cell

Table1: Performance parameters comparison of SRAM cell

S. No	Parameter	Existing 10T SRAM Cell	Proposed 12T SRAM Cell
1	Delay	12.542ps	9.7356ps
2	Power consumption to read	1.22mW	0.98mW

The table1 shows the comparison of SRAM cell parameters such as delay and power with existing method. It is observed that delay and power consumption is reduced in the case of proposed method.

V. CONCLUSION

Power dissipation has become a major issue as the demand of battery operated devices has increased. In this paper a low power and high speed l2T SRAM cell has been proposed. This proposed SRAM cell has two voltage sources which are used for reducing the voltage swing during switching activity. The reduction in voltage swing results in reduction of dynamic power dissipation. The simulation shows that the same SRAM cell dissipates less power as of 20% and 1.37× the delay in comparison with the existing 10T SRAM cell. Although numbers of transistors and area are increased in the proposed SRAM cell in comparison to those of conventional 6T SRAM cell and 10T SRAM cell but low power dissipation and high speed can dominate over this drawback.

REFERENCES

[1]. B. Wang, T. Q. Nguyen, A. T. Do, J. Zhou, M. Je, and T. T. H. Kim.2015 "Design of an ultra-low voltage 9T SRAM with equalized bit line leakage and CAM-assisted energy efficiency improvement," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 2, pp. 441–448.

[2]. S. Lin, Y.-B. Kim, and F. Lombardi.2008, "A low leakage 9t SRAM cell for ultra-low power operation," in Proc. 18th ACM Great Lakes Symp. VLSI, 2008, pp. 123–126.

[3]. S. Lutkemeier, T. Jungeblut, H. K. O. Berge, S. Aunet, M. Porrmann, and U. Ruckert. 2013, "A 65 nm 32 b sub threshold processor with 9T multi-Vt SRAM and adaptive supply voltage control," IEEE J.Solid-State Circuits, vol. 48, no. 1, pp. 8–19.

[4]. T. Song, S. Kim, K. Lim, and J. Laskar. 2010, "Fully-gated ground 10T-SRAM bitcell in 45 nm SOI technology," Electron. LettS. vol. 46, no. 7, pp. 515–516.

[5]. M. H. Abu-Rahma, M. Anis, and S. S. Yoon.2010, "Reducing SRAM power using fine -grained wordline pulse width control," IEEE Trans. Very Large-scale Integr. (VLSI) Syst., vol. 18, no. 3, pp. 356–364.

[6]. G. Pasandi and S. M. Fakhraie. 2015, "A 256-kb 9T near-threshold SRAM with 1k cells per Bitline and enhanced write and read operations," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 11, pp. 2438–2446.

[7]. S. Ahmad, M. K. Gupta, N. Alam, and M. Hasan. 2016, "Single-ended Schmitt-trigger-based robust low-power SRAM cell," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 8, pp. 2634–2642.

[8]. B. D. Yang . 2010 "A low-power SRAM using bit-line charge-recycling for read and write operations," IEEE J. Solid-State Circuits, vol. 45, no. 10, pp. 2173–2183.

[9]. H. Noguchi et al. 2008, "Which is the best dual-port SRAM in 45-nm process technology? 8T, 10T single end, and 10T differential," in Proc. IEEE Int. Conf. Integr. Circuit Design Technol. Tut, pp. 55–58.

[10]. B. Wang, T. Q. Nguyen, A. T. Do, J. Zhou, M. Je, and T. T. H. Kim. 2015 "Design of an ultra-low voltage 9T SRAM with equalized bitline leakage and CAM-assisted energy efficiency improvement," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 2, pp. 441–448.
[11]. H. Jeong, T. Kim, T. Song, G. Kim, and S. O. Jung. 2015, "Trip-point bitline precharge sensing scheme for single-ended SRAM," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 7, pp. 1370–1374.
[12]. B. H. Calhoun and A. P. Chandrakasan. 2007, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," IEEE J. Solid-State Circuits, vol. 42, no. 3, pp. 680–688.
[13]. R. Saeidi, M. Sharifkhani, and K. Hajsadeghi. 2014, "A subthreshold symmetric SRAM cell with high read stability," IEEE Trans. Circuits Syst. II, Express Briefs, vol. 61, no. 1, pp. 26–30.
[14]. J. Singh, S. P. Mohanty, and D. Pradhan, 2012, Robust SRAM Designs and Analysis. New York, NY, USA: Springer-Verlag,.