ANALYTICAL MODELLING AND SIMULATION OF LNA USING DOUBLE GATE MOSFET

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Abstract: All the ultra wideband (UWB) circuits can be realized or designed by using short channel devices like CMOS but these short channel devices are always influenced by short channel effects. Use of Double gate metal oxide transistors or DGMOSFET is found to be an alternative to overcome this drawback. This paper presents design of a two stage low noise amplifier using 30nm double gate MOSFET in order to achieve better gain and less power consumption for 3.1 - 10.6 GHz ultra wide band applications. Various performance parameters of LNA are varied via back gate tuning in 30nm DG-MOSFETs. These parameters include power, gain, input impedance, noise figure and return losses. Low power of 12mW, minimum Noise figure (*NFmin)* of 1.41db, high gain of more than 10db, wideband input matching of 50ohms and third order intercept point (IIP3) of - 5.1dBm is to be achieved. These performance parameters are either comparable or better to some of the recent LNA designs in 60 GHz frequency at different technologies.

Index Terms: **Introduction, DGMOSFET, LNA Design using DGMOSFET, Conclusion**

I. INTRODUCTION

Over the years for economical applications the demand of Ultra Wide Bands circuits is increasing exponentially because of its wide bandwidth, low power level(up to -41.3Db/MHz),high data-rate(up to 480Mbps),multi-band applications and low cost [1-6]. Reason behind the increased growth for designing these circuits include wireless personal area networks, medical imaging systems ground and vehicular penetrating radars, and sensor nodes for wireless networks [6]. The first module of UWB receiver is LNA and it has an important significance on the sensitivity and dynamic range of the whole range receiver system[4]. In order to enhance the performance of these systems and to satisfy the demand of mm wave applications LNA needs to integrate features such as wide band input matching, high power gain, absolute stability in the whole band, low and flat NF, and low power dissipation to improve the battery life of handheld devices[2-7]. To achieve all these features LNA is designed by using 'DOUBLE GATE MOSFET'. The LNA's designed by using conventional CMOS suffers from high short channel effects, high gate resistance, increased substrate loss, normal trans conductance and high channel charging resistance so it makes CMOS a dubious choice for its design and moreover in accurate compact models add to its demerits. Alternatively some devices like3[RD] - 5TH semiconductors like GaN, GaAs are also used for the design of few LNA's [8] and Compound semiconductors like SiGe devices [9] and FINFETs [10] are also known to add a little benefit over conventional devices But perhaps of these little benefits, these are not considered as better alternatives due to their high integration cost, power consumption and IC handling issues. Hence the exploration of CMOS to reach around 280GHz in 45nm technology [11] . Other advantages like low fabrication cost, low power consumption and compact structured design strongly recommend CMOS a better choice for RF circuit designs.

Now feedback in CMOS based LNA is also an important issue for switching towards the DGMOSFETs based LNA. Feedback techniques can be used in circuits in which the active devices poles are in frequencies well above the feedback loop bandwidth. It has been possible to use feedback in high frequency LNA circuits [12] With increasing *ft* of MOS transistors in last few years. Feedback techniques are often adopted in designing low noise amplifiers in order to shift the optimum noise impedance to the desired point [13] but for shifting the noise impedance and for enhancing the overall gain of the amplifier the circuit needs the on chip inductors to resonate with the parasitic capacitors to improve gain, but the issue is that it needs lager area to realize this type of circuit and on the other hand if we switch to inductor free models like resistive type feedback more number of stages are required to achieve high gain and hence the power loss and area required increases because of resistive loss. Other than this if other techniques like current steering techniques like gain inductive gain peaking technique and current reuse technique are used all those suffer from parasitic effects and leads to noise figure degradation.

Also same case is in electrostatic discharge protection in which due to high impedance and low breakdown voltage in CMOS circuits, ESD protection in the I/O pads is an important issue in these RF circuits though LNA with CMOS transistors in sub-threshold regime is useful in very low power applications[14].however, by this way the transistors gm is very low and hence cannot be used in very high frequencies, in which increased losses in different parts of circuit necessitates high gm for transistors. The trans conductance of CMOS transistors decreases with decreasing the drain current which leads to the evolution of DGMOSFETs. Thus DG MOSFETs which is the solution to all the above problems are identified as future generation devices with promising low power characteristics. This forms the scope of the paper.

The organization of this paper is as follows section 2[nd]deals with the DC and AC parameters of DGMOSFETs using core model. Section 3[rd]involves design of LNA using DGMOSFETs, Section 4th involves the conclusion.

II.   DGMOSFET

The conventional MOSFETs show heavy short channel effects like drain induced barrier (DIBL) and poor on-off characteristics as the channel length of devices goes down in the sub-50nm range. The Double Gate (DG) MOSFETs efficient enough to replace the conventional MOSFETs in this particular regime because of their outstanding immunity to the short channel effects, improved on-off characteristics and better control of gates on the channel[15].Since the scalability and on-off characteristics of DG-MOSFETs are defined by the sub threshold slope of the device, accurate modeling of DG-MOSFETs are of great significance for the designing of switching circuits for VLSI and ULSI applications. Pramod Kumar Tiwari and S.Jit [16] proposed a sub threshold swing model for symmetric Double gate MOSFETs explaining the enhanced features of DG-MOSFETs.
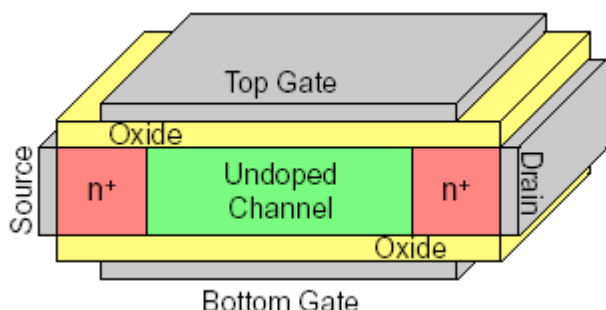

Figure 1 General DG-MOSFET Structure [17]

Double gate MOSFET comprises of a conducting channel (usually undoped), surrounded by the gate electrodes on either side of the channel. This dual gate ensures that no part of the channel is far away from a gate electrode and which in turn ensure that the channel width is not comparable with device width and thus reducing short channel effects.Fig.2 shows the graph reduced short channel effects in DG-MOSFET. For small channel lengths potential barrier at the drain is lowered as Vds increases, allowing more electrons to flow in to the drain. This effectively lowers Vt, causing a larger Ioff.
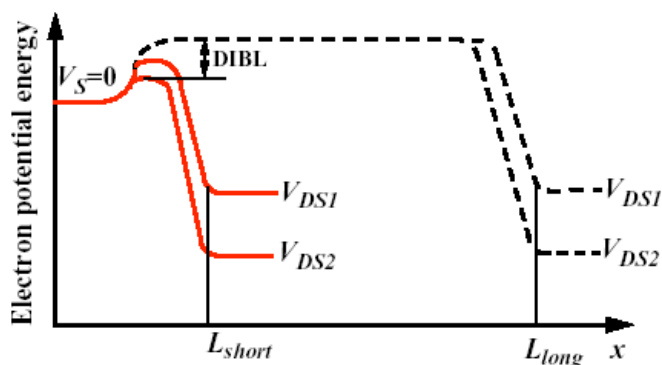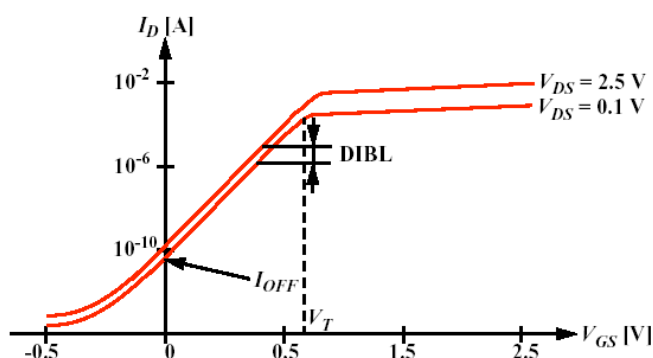

Figure 2 Potential energy versus distance [18]

Figure 3[19]

Another parameter Ioff which is defined as the drain current at Vgs=0V and Vds=Vdd. Ideally Ioff is zero but generally it is produced due to thermionic emission, quantum mechanical tunneling and band to band tunneling. It increases as we move the body further away from the control of the gate.
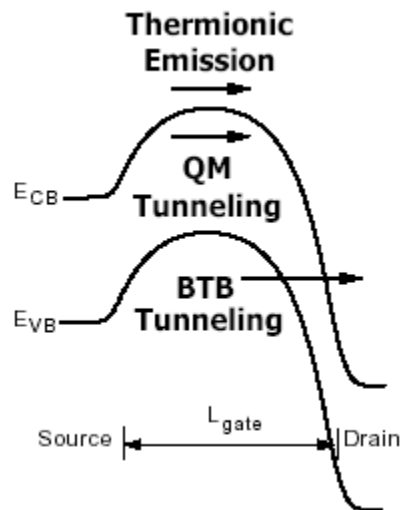
Figure 4[20]

Reduction in Ioff is the main advantage of using DG-MOSFETs for designing of LNA over conventional MOSFETs. By placing a second gate on the opposite side of the device, the gate capacitance of the channel is doubled and the channel potential is better controlled by the gate electrode, thus limiting Ioff.

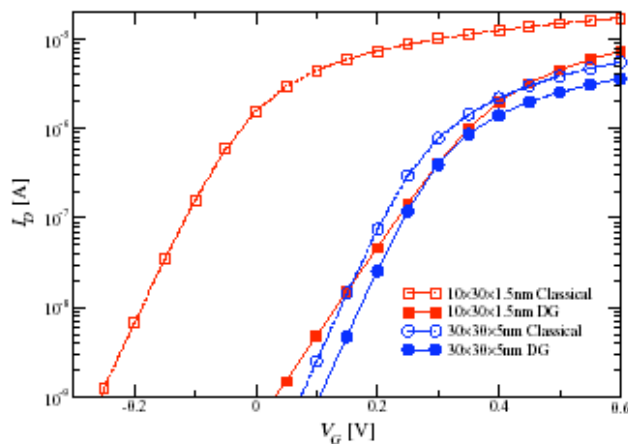

Figure. 5,[21]

Following reduction of Ioff another advantages like in DG-MOSFETs undoped channel eliminates intrinsic parameter fluctuations and minimizes impurity scattering and also allows higher current drive capability.

III.   LNA DESIGN USING DOUBLE GATE MOSFET

Most of the broadband LNA's find numerous applications in communication systems that too in their receivers and also in instrumentation equipment. Basically low noise amplifiers belongs to that section of electronic amplifiers which are particularly used where the received signal from antenna are barely recognizable to enhance or in other words we can say that it amplify the signals of low strength without adding any noise. It is designed closed to receiving device to make sure that there minimum loss in signal strength due to interference. In a receiver system the signal to noise ratio (SNR) of the received signal is high and it needs to be degraded at most by 50% so the LNA is used in the first circuit block in the receiver chain. And this is the reason why its noise performance dominates the systems sensitivity. The main objective of this work is to obtain high voltage gain, lesser power consumption, low and flat noise figure and absolute stability over the whole frequency band.

The following circuit topology in fig.6 shows a two stage low noise amplifier in which two DG-MOSFETs and one simple n type MOSFET are used in a 2 stage common source cascade topology. The transistor T1 is a common source transistor which operates in symmetric mode while the other two transistors T2 and T3 operates in independent mode. These two transistors T2 and T3 are connected in cascade manner where the transistor T2 is in common gate configuration. For optimized gain performance and better input return losses the width of the transistors are taken to be 20nm and length is 40nm. The supply Vdd is kept constant at 1.2 V which ensures that the applied voltage do not exceed the operating voltage of the devices and they may not get destroyed.
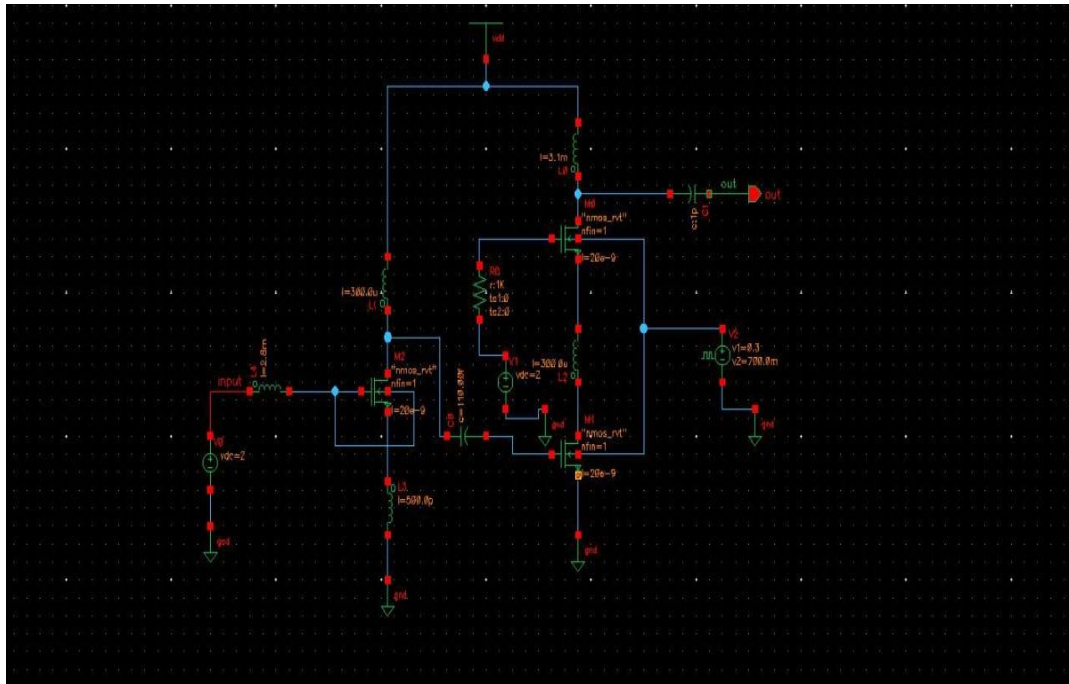
Figure 6 LNA design using DGMOSFET

Now to obtain minimum noise figure in the wideband impedance matching network a series peaking circuit which consists of an inductive load L2 and a capacitor C1is employed at the input where L2 resonates with inter stage capacitance C1 enabling high operating frequency.[22]

The inductive degeneration circuit consists of L3 which yields wide band impedance matching and allowing maximum power transfer with reduced input VSWR. The inductor L4 present in middle of the two transistors T2 and T3 compensates for low Ft [23] of DG-MOSFET which is about 200GHz at 45nm [24]. Inductive load L1 is set to resonate with gate source capacitance of T1 and also T2 is biased at 2V (Vb).The back gate voltage Vbg of both DG-MOSFETs is varied between o.3v to 0.7v and the results are recorded and plotted which will be shared in next paper.

IV. CONCLUSION

In this work a two stage DG-MOSFET based LNA has been designed where it has been tried to prove that DG-MOSFET is much viable option for the design of highly efficient nano scale mm-wave LNA rather than other conventional devices mainly CMOS. At the input a series peaking circuit was employed to achieve a wideband impedance matching of the generator impedance to the source impedance which results in minimum noise figure. Source degeneration circuit is also used which ensures the maximum inter-stage power transfer and thereby increasing the overall voltage gain. Now the back gate voltage plays the key role here which is varied and the results are simulated. The two gates of double gate mosfet ensures that no part of the channel is far away from the gate reducing the short channel effects. Further work will be presented in next paper which will be consisting of results recorded and simulations.

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