

# A Power Quality Improved Bridgeless Converter Based Computer Power Supply

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## ABSTRACT

Poor power quality, slow dynamic response, reduced output voltage regulation, high device stress, harmonic rich, periodically dense, peaky, distorted input current are the major problems which are frequently encountered in conventional switched mode power supplies (SMPSs) used in computers. To mitigate these problems, it is proposed here to use a non-isolated bridgeless buck-boost single ended primary inductance converter (SEPIC) in discontinuous conduction mode (DCM) at the front end of an SMPS. The bridgeless SEPIC at the front end provides stiffly regulated output dc voltage even under frequent input voltage variations and loads. The output of the front end converter is connected to a half bridge dc-dc converter for isolation and also for obtaining different dc voltage levels at the output that are needed in a computer. Controlling a single output voltage is able to regulate all the other dc output voltages as well.

**Key Words - Bridgeless Converter, Power Factor Improvement, Switch Mode Power Supply, Power Factor Correction, Power Quality Improvement**

## 1. INTRODUCTION

Normally, a half-bridge voltage source inverter (VSI) is used at the output for high-frequency isolation and multiple dc output voltages in computer power supplies because it provides better core utilization than any other uni polar converter and it is cost effective compared to push-pull and full-bridge converters. It is observed from the available literature that the bridgeless converter-based multiple-output SMPS has not been attempted so far, particularly targeting SMPSs for PCs. Therefore, an attempt is made here to reduce the current harmonics and to achieve high PF at the utility interface in a multiple-output SMPS by using a bridgeless buck-boost converter at the front end. The diode bridge at the front end is eliminated, and two buck-boost converters are connected back-to-back so that each takes care of one half cycle of the ac supply. The bridgeless buck-boost converter is designed in DCM for single control loop and for inherent PFC. This regulated dc voltage is given to half-bridge VSI for obtaining multiple-output dc voltages. The half-bridge VSI is designed in continuous conduction mode to reduce the component stress. Many electronic appliances powered up from the utility utilize the classical method of ac-dc rectification which involves a diode bridge rectifier (DBR) followed by a large electrolytic capacitor. The uncontrolled charging and discharging of this capacitor instigates a harmonic rich current being drawn from the utility which goes against the international power quality standard limits [1-2].

Modern ac-dc converters incorporate power factor correction (PFC) and harmonic current reduction at the point of common coupling (PCC) which improves voltage regulation and efficiency [3-5] at the load end. Personal computer is one of the electronic equipment which is severely affected by power quality problems. Single stage and two stage conversion of ac voltage into dc voltage have been used in computers to maintain harmonic content within limits and also to obtain stiffly regulated multiple outputs. Single stage power conversion is simple, compact and cost-effective. However, it suffers from poor dynamic response, control complexity, high capacitance value and high component stress. So, two stage conversion of ac voltage into multiple dc voltages is mostly preferred in computers [6]. The component count of the two stage power supply is high in comparison to its single stage counterpart; also, it provides better output voltage regulation, fast dynamic response and blocks the 100Hz component in the first stage itself so that large capacitors at the output side are avoided. Various front end converters have been employed in the power supplies for providing PFC and output voltage regulation.

A boost converter is the common choice for providing PFC in power supplies. However, it is not the preferred choice in computer power supplies due to its large input voltage range [7]. The output voltage of a boost converter cannot be controlled to a value less than 300V for a 220V ac input supply. Therefore, buck-boost converter is preferred in computers where wide variations in input voltages and load are expected [8-9]. The efficiency of a two stage SMPS is lower than the conventional SMPS; to eliminate this disadvantage, a new bridgeless front end converter is proposed in this paper for computer power supplies. The elimination of DBR at the front end results in reduced conduction losses and large output voltage range with enhanced efficiency [10-13]. At the output of the front end converter, a half bridge converter is used which provides isolation, regulation and multiple dc outputs [14 -16]. The authors demonstrated various power quality improvement methods with different controllers [17-21]. Matrix converter based power conversions also increasing the power quality by reducing steady state error, THD reduction [22-24]. The half bridge converter is a common choice because it offers better core utilization. It is observed from the available literature that the power quality improvement in SMPSs using bridgeless PFC converter has not been attempted by many researchers so far. In this work, a bridgeless single ended primary inductance converter (SEPIC) is used at the front end of the SMPS. Test results of the proposed multiple-output SMPS are found in line with the simulated performance demonstrating its improved power quality and output voltage regulation.

## 2. PROPOSED SYSTEM TECHNIQUE

This proposed paper deals with the design, analysis, simulation, and development of a power-factor-correction (PFC) multiple output switched-mode power supply (SMPS) using a bridgeless buck–boost converter at the front end. Single-phase ac supply is fed to a pair of back-to-back-connected buck–boost converters to eliminate the diode bridge rectifier, which results in reduction of conduction losses and power quality improvement at the front end. The operation of the bridgeless buck–boost converter in discontinuous conduction mode ensures inherent PFC operation and reduces complexity in control. The performance of the proposed multiple-output SMPS is evaluated under varying input voltages and loads by simulating this circuit in MATLAB/ Simulink environment, and the results obtained through simulation are validated experimentally on a developed prototype. Both simulation and experimental results demonstrate the improved performance of the proposed SMPS.

To simulate the proposed bridgeless-converter-based multiple output SMPS, it is essential to estimate the component values. To derive the necessary design equations, the switches and diodes are considered to be ideal, and the switching frequency is considered very high compared to the line frequency (50 Hz). This enables considering the average quantity in one switching cycle for analysis purposes.

### 2.1 Bridgeless PFC converter based computer SMPS

#### 2.1.1 Performance of Conventional SMPS

The conventional computer SMPS draws a harmonic rich, distorted peaky input current with a high crest factor and low PF from the single phase ac mains. The THD of the input current is observed of the order of 80% and the PF is 0.4 which affects the distribution system. This violates the set guidelines of harmonic emission and is not recommended by the power quality standards. Therefore, it is highly recommended to improve the power quality of the conventional computer SMPS.

#### 2.1.2 Performance of SMPS under Varying Input Voltages

The performance of the PFC bridgeless converter based SMPS which is recorded at full load and rated voltage condition. The unity PF operation is obtained with the input current being sinusoidal while the output voltage of the PFC converter is regulated to 300V. The inductor current of positive half cycle converter  $i_{Lp1}$  and the negative half cycle operated converter  $i_{Ln1}$  and are in CCM as per the design.

The inductor current of positive half cycle converter  $i_{Lp1}$  operates in positive half cycle of the input voltage and inductor current of negative half cycle converter  $i_{Ln1}$  operates when the input voltage is negative. Both the currents touch zero in each switching cycle which verifies the design criteria of inductor being in DCM. The upper inductor operates in DCM when input voltage is positive and the lower inductor operates in DCM when the input voltage is negative. The capacitor voltages of both the converters which operates alternately in positive and negative half cycles of input voltage and are in CCM as per the design. The full load performance of PFC converter based SMPS. The input current THD in this condition is recorded as 6.5%. To demonstrate the performance of SMPS at wide input voltage range, the test results are 170V and 300V condition and are presented. At 170V-270V, the input current remains sinusoidal while the PF is maintained to unity. The dynamic performance during input voltage variation and the output voltage is maintained constant within few power cycles of input voltage.

#### 2.1.3 Performance of SMPS under Light Load

The light load performance of SMPS is recorded by switching on and off some loads. The test results demonstrate the fairly improved power quality and the input current being sinusoidal with its THD being 7.3% which is within the limit set by IEC 6100-3-2. The input and output voltages and currents when a step change is applied in load. The output voltage remains constant while the input current is changed to maintain the power balance. The component count of the proposed bridgeless PFC converter based power supply is high because two PFC converters are added in the front end in comparison to the classical PFC based SMPS. However, the input current in the proposed SMPS flows through fewer components compared to the classical PFC based power supply. Therefore, the efficiency of the bridgeless PFC converter based SMPS is higher than the conventional PFC converter based SMPS.

Table.1 shows the comparison of PFC based SMPS and proposed SMPS system. Test results demonstrate the excellent performance of the proposed bridgeless converter based SMPS under all operating conditions and hence it can be recommended as an effective solution for mitigation of power quality problems for computer application

**Table.1 Comparison between Classical PFC and Proposed PFC**

Component		Conventional PFC	Proposed PFC
Slow diode		4	2
Fast recovery diode		1	2
High Frequency switch		1	2
Current conduction path	Lp1 charging	2 Slow diodes, 1 switch	1 Slow diodes, 1 Switch
	Lp1 discharging	2 Slow Diodes, 1FastRecovery Diode	1 Slow Diodes, 1 fast Recovery Diode
	Lp1 Zero Current	2 slow diodes	1 slow diodes

3. SIMULATION RESULTS AND DISCUSSION

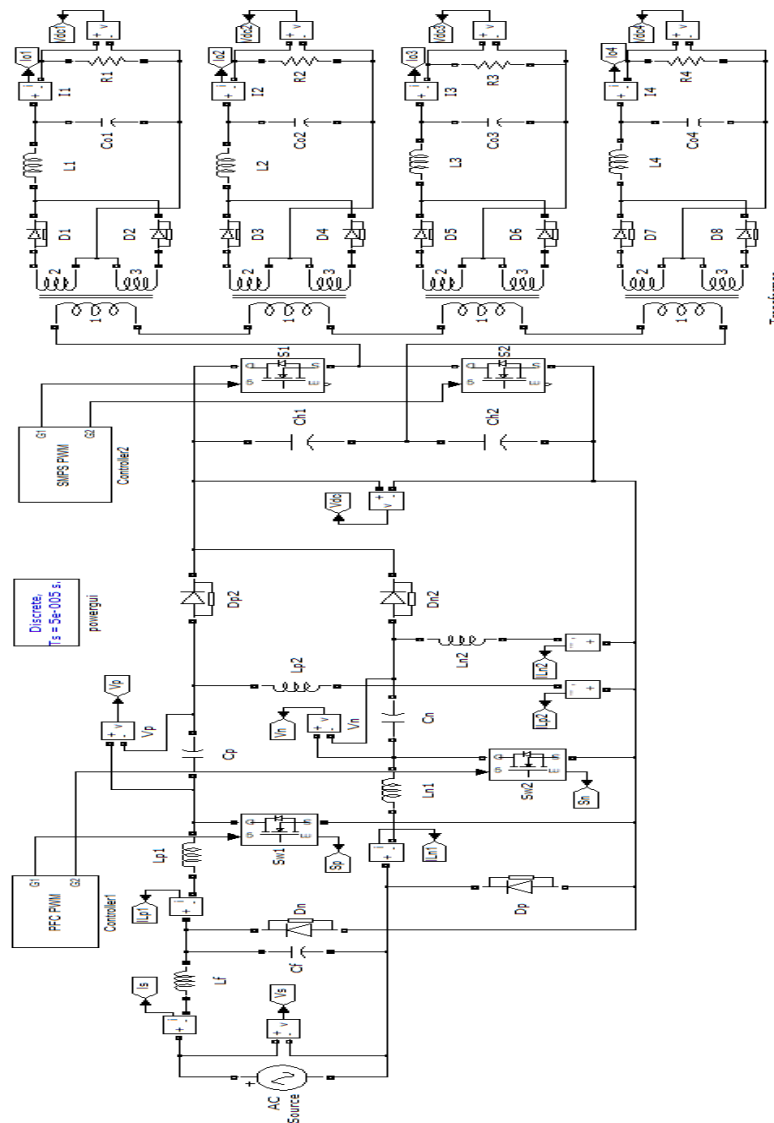
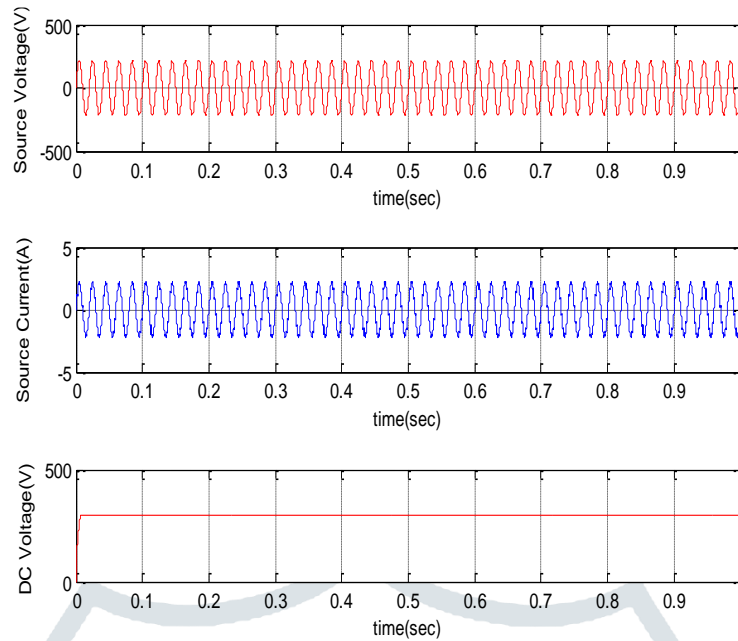


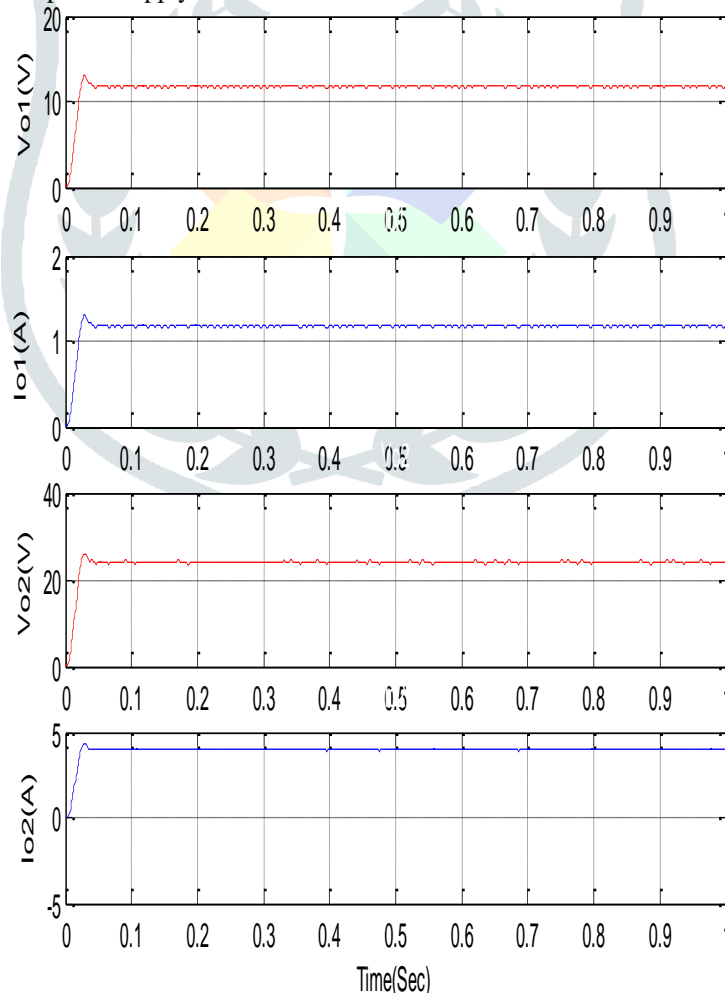
Fig-1. Simulation diagram of PFC converter based SMPS

Fig.1 shows the simulated results of PFC converter based SMPS. It shows the various performance indices such as input voltage/current, input inductors ( $L_{p1}$ ,  $L_{n1}$ ), output inductors ( $L_{p2}$ ,  $L_{n2}$ ), intermediate capacitor ( $C_p$ ,  $C_n$ ), output voltage ( $V_{PFC}$ ) and output voltages / current ( $V_{o1}/I_{o1}$ ,  $V_{o2}/I_{o2}$ ,  $V_{o3}/I_{o3}$ ,  $V_{o4}/I_{o4}$ ). The simulated performance is discussed in the following sections.

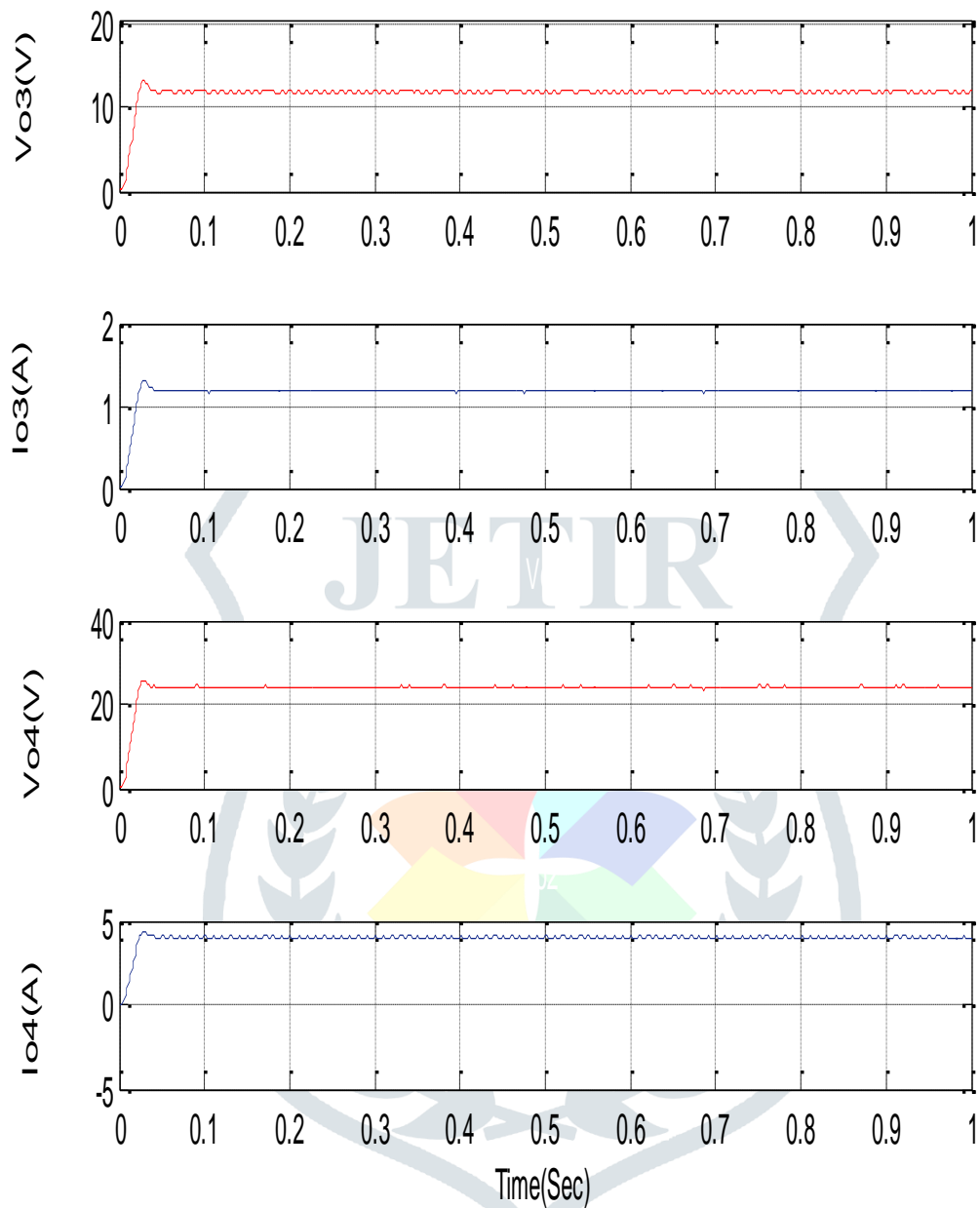


**Fig-2.** The input ac voltage/current

Full load performance of the PFC bridgeless converter based computer SMPS is shown in Fig.2. The input ac voltage and current are found to be sinusoidal with a harmonic distortion of 3.33%. The output voltages are maintained constant with their respective output currents. Simulink models but also during the development phase where the developer generates inputs to test the system. By the substitution of the Constant and Signal generator blocks of Simulink the stimulation becomes reproducible. Figure 4 shows the Performance of the computer power supply at rated condition.

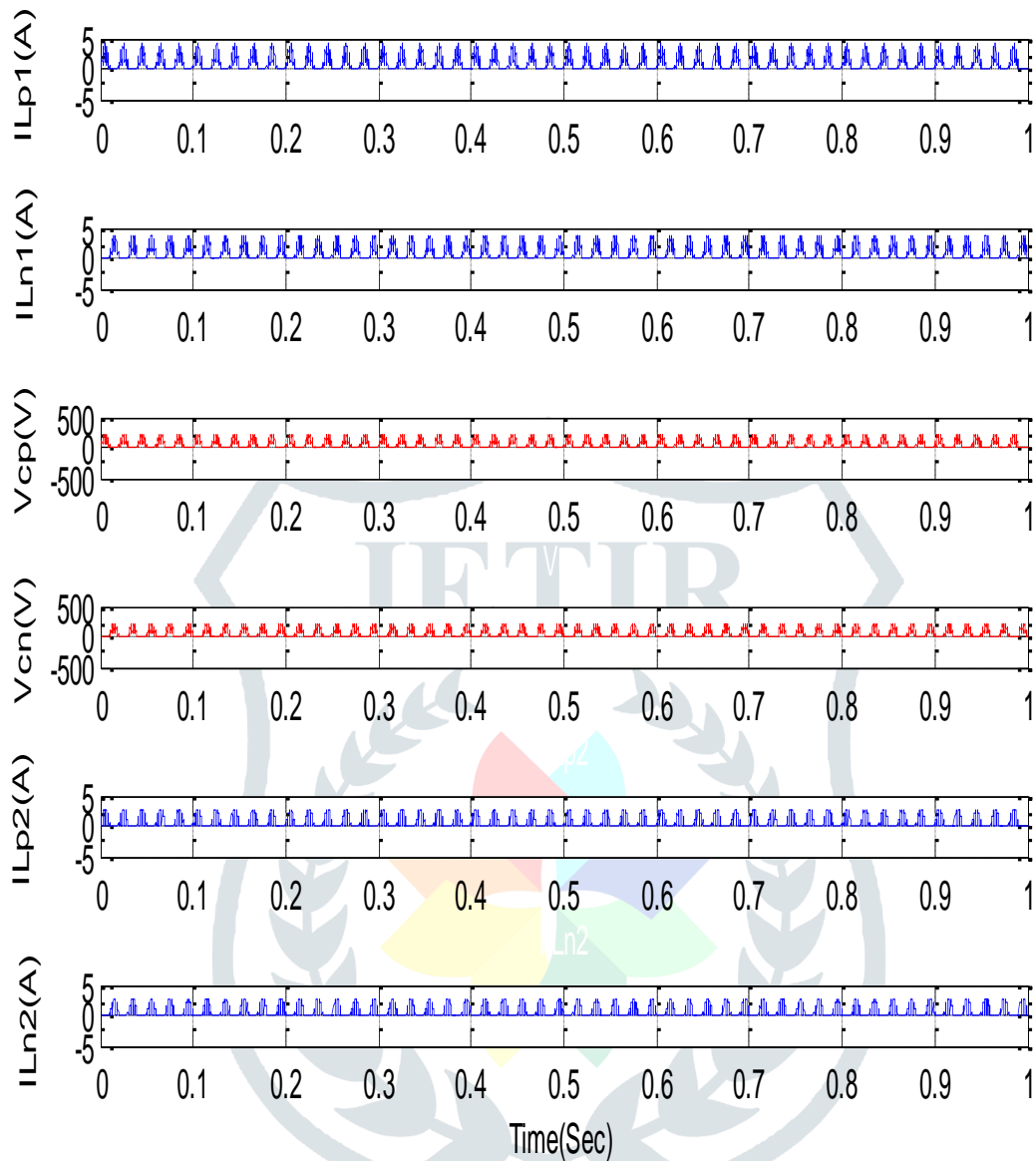


**Fig-3.** Performance of the computer power supply at rated condition.



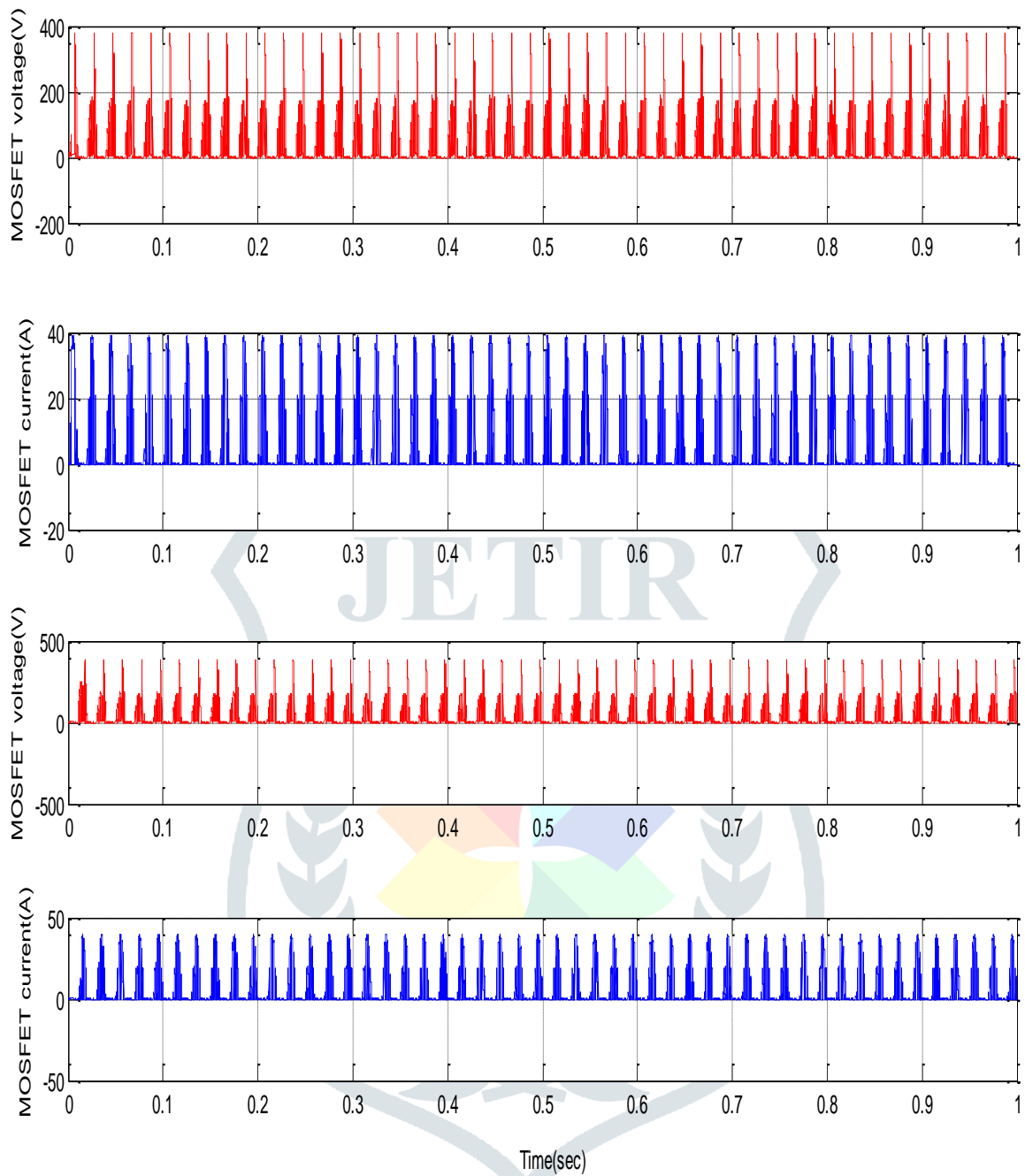
**Fig-4.** Performance of the computer power supply at rated condition

A power supply unit (or PSU) converts mains AC to low voltage regulated DC power for the internal components of computer personal computers universally use switched-mode power supplies. Some power supplies have a manual switch for selecting input voltage. Figure 4 Shows the Performance of the computer power supply at rated condition.



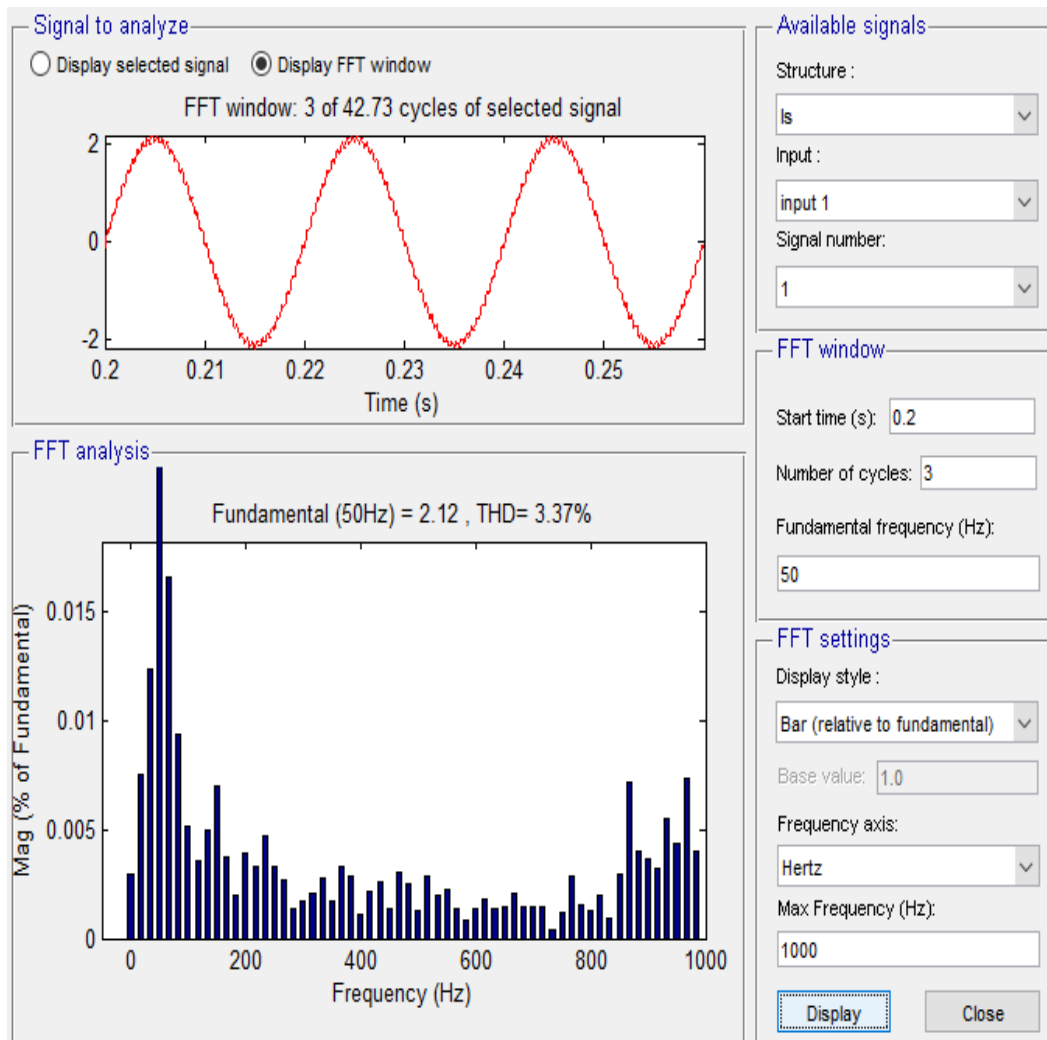
**Fig-5.** Wave form of various components of converter

The above figure 5 shows the current and voltages of positive and negative currents of both inductor and capacitor. The principle of operation converter is based on switch mode action of its switches commutation of the switch generate very fast current and /or voltage transient .The transient behaviour of a source is characterised.



**Fig-6.** Wave form of various components of converter

Figure 6 shows the different MOSFET current and voltage waveforms of converter. The MOSFET characteristics cut off region is a region in which the MOSFET will be off.



**Fig-7.** Input current and its harmonic spectrum at full load condition

The above figure 7 shows the total harmonic distortion of proposed SMPS is 3.37%. Harmonic distortion often stated as a measurement called Total Harmonic distortion or THD, which is a percentage of the overall signal compose of harmonic distortion. This because there could be relatively high amount of harmonic distortion in lower order which could compose a substantial percentage of the output.

#### 4. CONCLUSION

A bridgeless non-isolated SEPIC based power supply has been proposed in this paper to mitigate the power quality problems prevalent in any conventional computer power supply. The proposed power supply is able to operate satisfactorily under wide variations in input voltages and loads. The design and simulation of the proposed power supply is initially carried to demonstrate its improved performance. Further, a laboratory prototype is built and experiments are conducted on this prototype. Test results obtained are found to be in line with the simulated performance. They corroborate the fact that the power quality problems at the front end are mitigated and hence, the proposed circuit can be a recommended solution for computers and other similar appliances.

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