DESIGN OF FLIP FLOPS BASED ON QUANTUM DOT CELLULAR AUTOMATA

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Abstract: **As the device dimension is shrinking day by day the conventional transistor based CMOS technology encounters serious hindrances due to the physical barriers of the technology such as ultra-thin gate oxides, short channel effects, leakage currents & excessive power dissipation at nano scale regimes. Quantum Dot Cellular Automata is an alternate challenging quantum phenomenon that provides a completely different computational platform to design digital logic circuits using quantum dots confined in the potential well to effectively process and transfer information at nano level as a competitor of traditional CMOS based technology. This paper has demonstrated the implementation of circuits like D, T and JK flip flops using a derived expression from SR flip-flop. The kink energy and energy dissipations has been calculated to determine the robustness of the designed flip-flops. The simulation results have been verified using QCA Designer simulation tool.**

Index Terms **– QCA, D, T and JK flip flops etc...**

1. INTRODUCTION

Harvest prospect of almost energy free computation is crucial inspiration of reversible logic circuit analysis. In VLSI design, the most important factor is power dissipation. For every bit of information loss, it dissipates heat in an order of k_BTln2 Joules; where k_B is Boltzmann constant, T is operating temperature. Bennett proved that if the computation is carried out in reversible way, k_BTln2 energy dissipation will not take place due to information loss. Reversible circuits are a special type of circuit that does not lose any information. A gate is called reversible if its funct×ion computes as bijective in manner. A reversible logic gate is a gate, if it has k inputs and k outputs with one to one mapping between input and output vector, and vice versa. Number of garbage outputs, quantum cost, and delay are essential cost metrics in reversible circuits.

Garbage outputs cannot be utilized as reversible logic circuit's outputs, used to preserve reversibility characteristic but don't accomplish necessary actions. In strategy of the reversible circuits, the exploration was initially restricted to design of the combinational logic circuits, as feedback can't be allowed in the reversible computing, which was simply a convention. Yet, in the research article, has also proved that the feedback can permissible in the reversible computing. Consistent with this, a sequential arrangement is reversible if its combinational part is reversible (i.e., the combinational system is acquired with removing delay elements; thus breaks the conforming arcs). Moreover, this is also revealed that the reversible finite automata can be formed with its transition functions' reversible realization and can be used as a com- binational part of anticipated sequential circuit. First design of the reversible sequential circuit was accomplished using the same concept. Here the proposed reversible sequential was reversible JK latch in which have feedback loop from the output. Also researcher has disproved the assertion that reversible sequential circuits can't reversible in behavior. In current literatures on proposal of the reversible sequential circuit design, major metric of optimization is reversible gate count. The quantity of reversible gates can't be decent cost metric for complexity analyze as every reversible gates may have different computational complexities and types; also each reversible gates may has different delay, quantum costs. Innovative approach of reversible latches design are introduced in this proposed article that diminish delay, number of garbage outputs, quantum cost; and the designs are more optimal likened to pre- existing latches[1].

There are various emergent nano-technologies, such as superconductor flux logic family, and optical computing, quantum-dot cellular automata computing, etc., where dissipated energy because of information ruin will be very important factor of overall heat extravagance of the circuit. Depending on the positions of the electron, QCA provides an alternative way of computation. Quantum dot cellular automata (QCA) exhibit small feature size, extreme low-power dealing and high clock frequency. Thus, the propound methodology of reversible latches design have been implemented in molecular QCA framework.

This paper is organized as section II describes Litarature review and in section III discussed about QCA and Section IV describes the proposed method. Section V shows the simulation results and comparison between existing and proposed methods and section VI concludes the paper followed by references.

2. LITARATURE REVIEW

[1] R. Landauer,"Irreversibility and heat generation in the computational process," IBM J. Res. Develop., vol. 5, pp. 183 - 191, 1961.

In we introduced a method to realize symmetric and non-symmetric functions using 4*4 multi-valued Fredkin Gate of Picton. Picton himself used this gate for realization of Digital Summation Threshold Logic Device (DSTL). However, our previous design required two MV Fredkin gates per cell and introduced two garbage bits per cell, and Picton's approach used gates that are not realizable in truly reversible (quantum) logic. In both ours and Picton's approaches, all cells were programmed by the same constants. We found however that a better design can be done using the recently invented 3 * 3 Kerntopf gate. Our new design presented below has a regular structure and introduces only one garbage output bit per cell. Moreover, because the cell is controllable from the input, it can be also

programmed to realize one more set of functions, which leads to essential improvement of the whole idea and to a new kind of programmable structure which we call RPGA.

[2] T. Toffoli, 1980. "Reversible computing," Tech. rep. Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science.

This is an abridged version of a much longer report of the same title, to which the reader may turn for further details, most proofs, and extended references. Here, the numbering of formulas, figures, etc. reflects that of the original version. Mathematical models of computation are abstract constructions, by their nature unfettered by physical laws. However, if these models are to give indications that are relevant to concrete computing, they must somehow capture, albeit in a selective and stylized way, certain general physical restrictions to which all concrete computing processes are subjected. One of the strongest motivations for the study of reversible computing comes from the desire to reduce heat dissipation in computing machinery, and thus achieve higher density and speed. Briefly, while the microscopic laws of physics are presumed to be strictly reversible, abstract computing is usually thought of as an irreversible process, since it may involve the evaluation of many-to-one functions.

[3] E. Fredkin, E. and T. Toffoli. 1982."Conservative logic," Int. J. Theor. Physics 21, 219 - 253.

Since many of the necessary technicalities have been thoroughly covered in a companion paper, "Reversible Computing" (Toffoli, 1981), here we shall have more freedom to present the ideas of conservative logic in a discursive fashion, stressing physical motivation and often making appeal to intuition. Computation--whether by man or by machine--is a physical activity, and is ultimately governed by physical principles. An important role for mathematical theories of computation is to condense in their axioms, in a stylized way, certain facts about the ultimate physical realizability of computing processes. With this support, the user of the theory will be free to concentrate on the abstract modeling of complex computing processes without having to verify at every step the physical realizability of the model. Thus, for example, a circuit designer can systematically think in terms of Boolean logic (using, say, the AND, No'r, and FAN-Ore primitives) with the confidence that any network he designs in this way is immediately translatable into a working circuit requiring only well-understood, readily available components (the "gates," "inverters," and "buffers" of any suitable digital logic family). It is clear that for most routine applications one need not even be aware of the physical meaning of the axioms. However, in order to break new ground one of the first things to do is find out what aspects of physics are reflected in the axioms: perhaps one can represent in the axioms more realistic physics--and reveal hitherto unsuspected possibilities [8].

3. QCA

The fundamental structure in quantum dot cellular automata is a QCA cell which is a squared cell with four quantum dots placed at its corners and two free electrons. These electrons can tunnel quantum mechanically by modulating tunnel barriers between dots and assemble diagonally due to Coulombic repulsion (Lent et al. [1]). The two electronic arrangements, representing cell polarization P = −1 and P = +1, can be encoded as logic 0 and 1, respectively as shown in Figure 1[2].

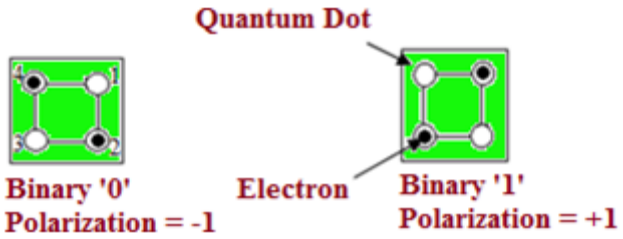


Fig. 1: Quantum cell with polarization

Polarization:

Polarization is a property of certain electromagnetic radiations in which the direction and magnitude of the vibrating electric field are related in a specified way.

P=(p1+p3)-(p2+p4)/p1+p2+p3+p4

There are mainly two types of quantum cell orientations namely 45˚ and 90˚. In order to transfer information from one cell to another cell QCA wire is used which is shown in figure..2 &1.3[3].

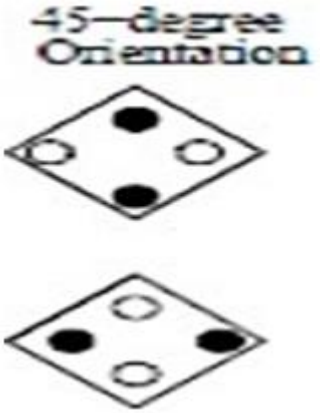


Fig. 2: 45 degree QCA cell

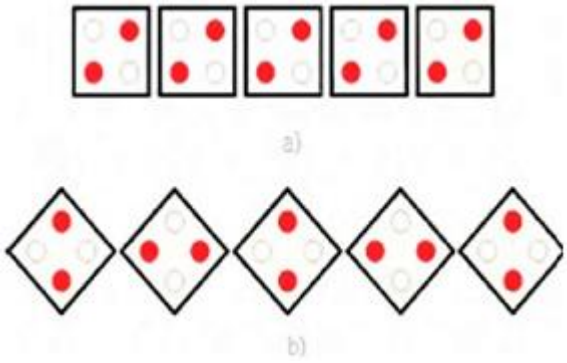


Fig.3: 90 degree QCA cell

QCA gates the elementary gates in QCA design are majority gate and an inverter as shown in Figure. A majority gate is realized with five QCA cells with three inputs and one output. It takes input from three cells and provides decision on the fourth cell. The output is based on the majority of input cells. If majority of input cells are polarized as logic 1, then output of the gate is also 1. The majority gate realizes a three-variable logic function as follows.

M (A, B, C) = AB + AC + BC (1)

Equation (1) represents the basic Boolean expression for majority gate, using which essential functions like logical AND logical OR can be implemented by fixing one input to logic 0 or 1, respectively. Another fundamental gate is inverter as shown in Figure1.4 &1.5. If the cells are placed then output is complement of the input realizing an inverter. This way all the basic gates and hence universal gates can be implemented using majority gates and QCA inverter [4].

4. PROPOSED METHOD

The main advantage of realizing configurable hardware is low device cost and efficient utilization of device area. Till date, all the existing configurable designs in QCA strictly follow design rules mentioned below as in – Fixing input cells (control inputs) to logic "0" or "1" to produce different functions. – Displacing some of the input cells to change the distance between driver cells of the device to generate different functionality.

Flip-flops are sequential circuits whose output depends both on the present input as well as the past output [12].It is a one bit binary storage device capable of storing binary information '1'or '0'.In this paper, most commonly used three types flip-flops namely D,T & JK flip flop are designed from the derived equations of SR flip-flop.

To ensure that QCA systems perform optimally there are some general design rules that should be followed while creating these systems? These design rules are based on the experience gained in creating and simulating the systems described later in this paper. They are as follows:

1. As a result of the non-linear cell-cell response function, which has a very high gain at the crossover point it has been found that cells tend to self re-enforce a weak input signal. It is wise then to ensure that at least two adjacent cells are present in any clocking zone to ensure this re-enforcing action takes place.
2. To ensure the proper result from the output of a majority gate, it is important that each of the signals arrives at the input at the same time and with the same signal strength. This can be easily accomplished by placing the cells that make up the majority gate in a separate clocking zone as its inputs as shown inThe three inputs to the gate are in one clocking zone. The majority gate itself is in the succeeding clocking zone. The output is taken off in yet another clocking zone. 3. Coplanar wire crossing is possible using a normal chain of QCA cells and an inversion chain of cells. This is possible because of the symmetry at the junction in which neither state of one wire with respect to the other is favorable, hence the ground states of the two wires are independent of each other. Imperfections in the layout of the system can lead to a breakdown in the symmetry of this system. To avoid the possibility of any switching interference while in the quantum analog state, the two lines are connected to different clocking zones [16].

Proposed Expression to Design Flip-flops:

Here its can simply construct any flip-flop in a much easier way just by modifying the inputs. All the flip-flops have been designed in this paper using the circuit as shown in the figure 4. . The design of SR, D, T, JK flip flops are realized using QCA designer simulation tool in this paper.

A. SR Flip-Flop

The first proposed QCA RS flip flop layout. The inner loop of the flip flop has a delay of one clock cycle; therefore at the output, Q is available 5 clocking zones after R and S have been applied. Fig.4.3 shows the second proposed RF flip flop. In this layout, the inner loop of the flip flop has a delay of one clock cycle; but at the output, Q is available 4 clocking zones after R and S have been applied.

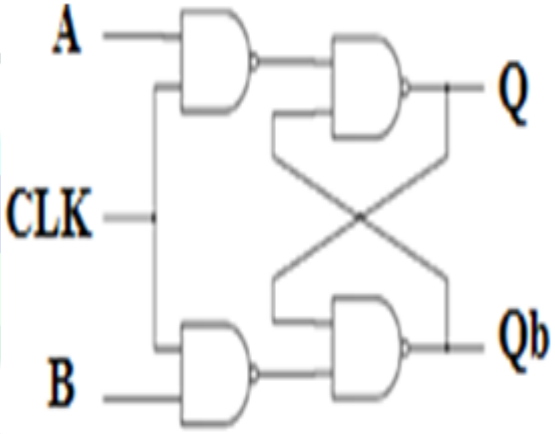


Fig .4: SR Flip Flop

The S-R flip-flop has two inputs namely, SET(S) and RESET(R), and two outputs Q and Q bar which are complement to each other. The clock pulse input acts as an enable input to the other two inputs S and R. We have simply replaced A by S and B by R from our proposed equation to generate SR flipflop.

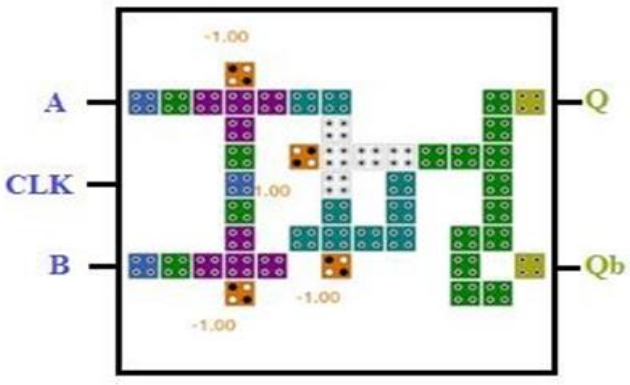


Fig. 5: QCA cells for SR Flip Flop

B. JK Flip-Flop

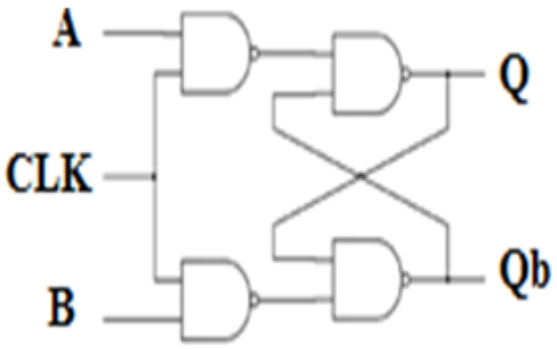


Fig.6 JK Flip Flop

A JK flip flop is a refinement of the SR flip flop, in which the indeterminate state of the SR type is defined in the JK type. In a JK flip flop, the input J is for set and the input K is for clear. The inputs J and K in a JK flip flop behave like the inputs S and R in a SR flip flop to set and clear the flip flop. When both J and K inputs are set to logic 1, the flip flop switches to its complement state, i.e., if Q=1, it switches to Q=0 and vice versa (Q is the output). The Output Q is ANDed with K and Clock inputs so that the flip flop is cleared during a clock pulse only if Q was previously 1. Similarly, output QO is ANDed with the inputs J and Clock so that the flip flop is set with a clock pulse only if QO was previously 1. Because of the feedback connection in the JK flip flop, the Clock signal, which remains at 1 after the outputs have been complemented once, will cause repeated and continuous transitions of the outputs. To avoid this undesirable operation, the Clock pulse must have time duration, which is shorter than the propagation delay through the flip flop.

The limitation of SR flip-flop is overcome in JK flip-flop. The inputs J and K behave as inputs S and R to set and reset the flip-flop respectively. When J=K=1, the flip-flop output toggles i.e. switches to its complement state. A JK flip-flop has been obtained from our proposed expression by adding two additional AND gates.

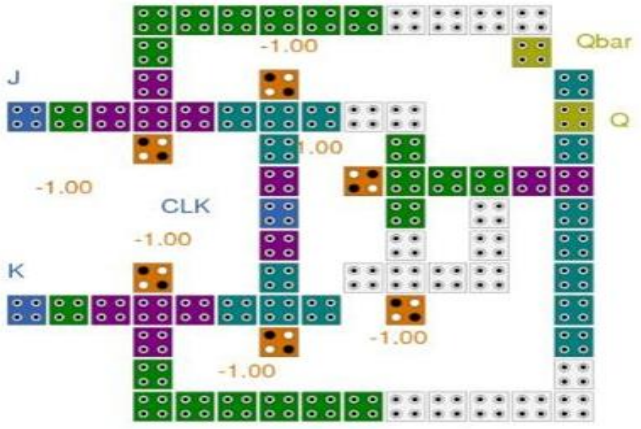
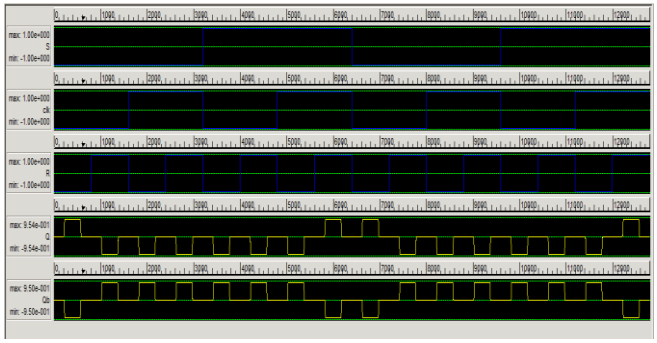


Fig.7 QCA cells for JK Flip Flop

5. SIMULATION RESULTS

A. Result of SR Flip-Flop



B. Result of JK flip-flop

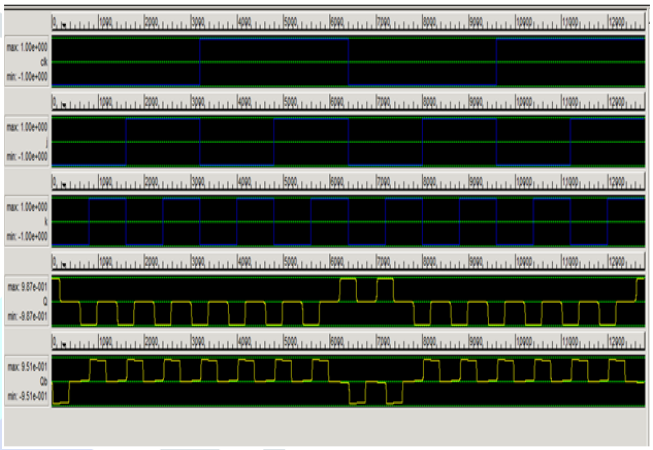


Table I: Comparison analysis with Existing method to proposed method

Existing Method	Area	Delay(Ns)
P-D Latch	289	6
N-D Latch	278	6
N-T Latch	410	7
Proposed Method	**Area**	**Delay(Ns)**
SR Flip Flop	39	2
JK Flip Flop	80	3

6. CONCLUSION

In this paper we have developed a standard equation from SR flip flop and using that equation other flip flops like D, T and JK flip-flops are subsequently designed. This is a new approach of designing flip-flops with less hardware complexity in nanotechnology. Any memory storage device can be built using the flip-flops designed in the above mentioned approach. The layout has been generated and simulation results are verified using QCA Designer simulation tool. The stability of the circuit has been clearly determined by the 3 -D plots of kink energy of the two possible combinations of the output cell. In future there is a scope for design other sequential circuits like registers,

counters, memory blocks and other flip flops using this generalized block.

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