COMPARATIVE ANALYSIS OF 3 LEVEL AND 5 LEVEL FLYING CAPACITOR BASED MULTI LEVEL INVERTER

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Abstract: ***As conventional two level inverter has limited power handling capability and high harmonic distortion in the output voltage, Multilevel inverter concept is growing as the new class of power converters for high and medium power applications. Multilevel inverters synthesize a near sinusoidal voltage from several levels of dc voltages with has minimum harmonic distortion. In present days, for control of multilevel inverters, Carrier Based Pulse Width Modulation (CBPWM) techniques gained importance because of simplicity in expansion to higher levels and can be applied to Sinusoidal and Space Vector modulation schemes. This paper discusses about adoption of Carrier Based Sinusoidal Modulation technique for 3 and 5 Level Flying Capacitor Multi Level Inverter(FCMLI). A comparative study of the performance of Three and Five level FCMLI is presented in terms of THD in the inverter voltage. Simulations are carried out using MATLAB/SIMULINK to validate effective suppression of harmonics when higher level inverter is adopted.***

Index Terms–Flying capacitor, multilevel inverter, CBPWM.

I. INTRODUCTION

Multilevel inverters have advantages like less voltage stress on switches, absence of EMI problems, less dv/dt ratio, high efficiency and less common mode voltage. Also they are suitable for high current and high voltage applications. The number of levels corresponds to the number of voltage steps in the output phase of the inverter. In multilevel inverters, effective harmonic elimination and voltage control is possible as the switches are controlled individually. Use of bulky snubber circuits can be avoided as the switches are operated from a fractional voltage of total dc link voltage.

An inverter with output voltage level greater than two is considered as multilevel inverter. The inverter voltage synthesized from increased levels is closer to sinusoidal wave shape with less harmonic content. Higher voltage levels can be achieved without device sharing problem as the voltages are spanned by series devices. But, due to complex control circuit and circuit layout, the number of voltage levels is restricted.

At present, three benchmark topologies are available such as i) Diode or Neutral Clamped multilevel inverter ii) cascaded H-bridge inverter and iii) flying or clamped capacitor multilevel inverter [1]. Diode Clamped multilevel inverters have limitations viz. several blocking voltages of diodes, inner diodes clamped indirectly and unbalanced dc link voltage. In cascade H- bridge inverters, more number of inverters are required suppress the harmonics. Also these inverters require complex dc voltage regulation drop. The flying capacitor multilevel inverter does not have such limitations imposed in above inverters [2]. However, the capacitor clamped inverters have advantage of splitting the voltage equally on several devices of smaller ratings connected in series. Another advantage is that several switch combinations are possible for a given voltage level which is useful for charging and discharging the capacitors. In this paper, a comparative study on three phase three and five level clamping capacitor multilevel inverters is analyzed with different modulation techniques.

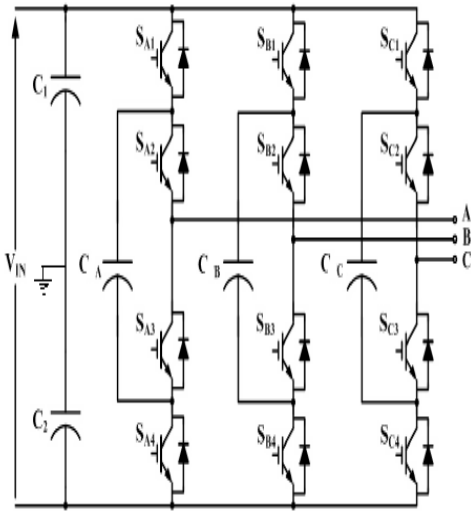
A. Flying Capacitor Multilevel Inverters

In 1992, Meynard and Foch proposed that capacitor clamped as flying capacitor inverter. It involves in series connection of clamped capacitors. In this configuration the voltage on each capacitor is differed from one another. The size of the output voltage is given from the voltage increment between two adjacent capacitors.

It requires bulk capacitors to clamp the voltage [7] [8]. The voltage rating of each capacitor is almost equal to the main power switch. In a m-level flying capacitor inverter will require (m-1)*(m-2)/2 number of clamping capacitors per phase along with (m-1) dc bus capacitors [5] [6].

B. Three Level Flying Capacitor Multilevel Inverters

Table 1: Switching States of 3-Level FCMLI



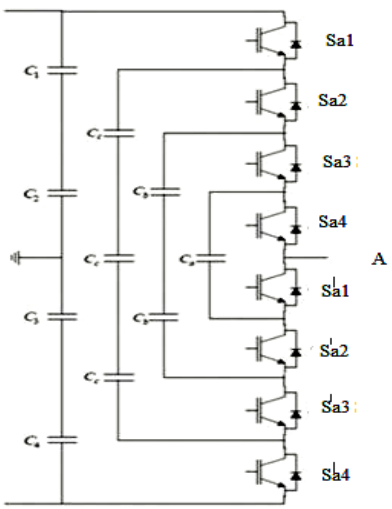
Vo	Sa1	Sa2	Sa3	Sa4
+Vdc	**1**	**1**	**0**	**0**
0	**1**	**0**	**1**	**0**
-Vdc	**0**	**0**	**1**	**1**

Fig. 1 Three -Level FCMLI

C. Five Level Flying Capacitor Multilevel Inverters

In capacitor clamped inverter, all the switches need not be conducting in a consecutive series. Also, the control system can be designed such that charging and discharging of required capacitors can be done to balance voltage across various levels as it has got phase redundancies. In a five level inverter, voltage synthesis is more flexible compared to diode clamped inverter. Fig 2. Show one phase of a five level inverter and its output can be synthesized by switch combinations as shown in table2.

Table 2: Switching States of 5-Level FCMLI



Vo	Sa 1	Sa 2	Sa 3	Sa 4	S'a 1	S'a 2	S'a 3	S'a 4
+Vdc	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
+Vdc/ 2	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**
0	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**
-Vdc/2	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**
-Vdc	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**

Fig.2 Five-Level FCMLI

II. MODULATION TECHNIQUES

Different PWM control strategies are evolved to reduce the Total Harmonic Distortion. With some modifications to conventional PWM strategies can be applied to MLI [3][4]. There are different Multi carrier based High frequency schemes namely i) Phase Shift PWM ii) Phase disposition PWM iii) Phase Opposition Disposition PWM iv) Alternate Phase Opposition

Disposition PWM v) Alternate Phase Shift PWM vi) Variable Frequency PWM vii) Alternate Variable Frequency PWM viii) Carrier Over Lap PWM.

In multilevel Inverters, modulation index is given by

$$MI = \frac{A_m}{(m-1)A_c}$$

This Paper presents comparison between PD and POD SPWM schemes to trigger the devices of 3 level and 5 level capacitor clamped inverter.

A. PD-SPWM Control Techniques

In this scheme, in order to generate pulses, a triangular wave is compared with sinusoidal wave. This technique can be applied to multi level inverter using several carrier waves. To generate 'm' level output (m-1) carrier are required. In phase disposition technique, all the carriers above and below reference line have same magnitude, frequency and all are in same phase. This method is widely used it results low harmonic distortion in output voltage.

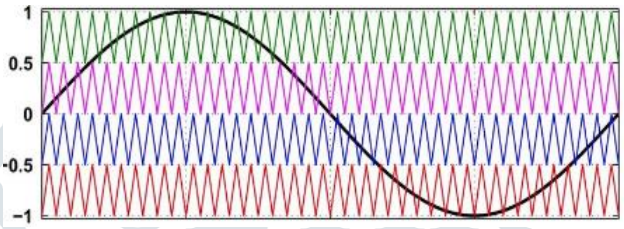


Fig.3 PD- SPWM Technique

B. POD-SPWM Control Techniques

In this technique, all the triangular waves above reference line are in same phase and below reference line are also in same phase. But, the waves above and below zero reference line are phase shifted by 180^0 from one another.

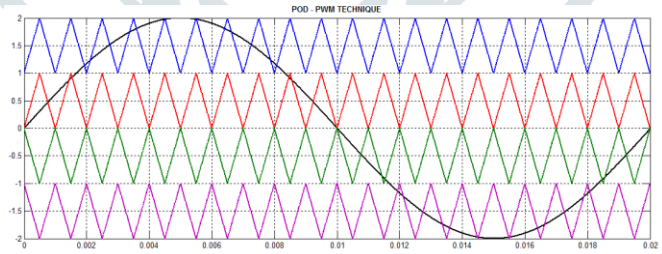


Fig.4 POD- SPWM Technique

III. SIMULATION RESULTS

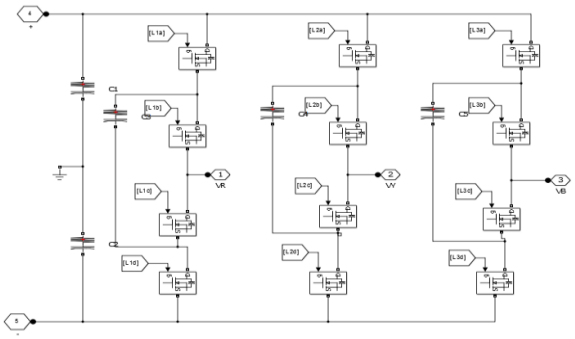


Fig.5 Simulink diagram of 3L inverter

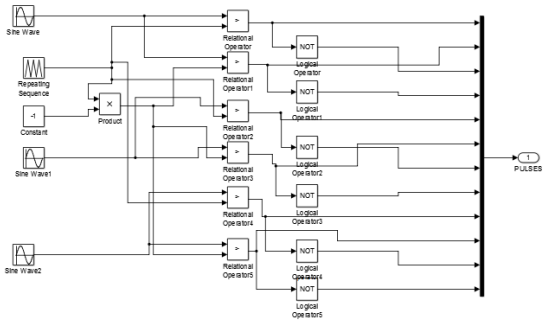


Fig.6 Pulse generation for 5L inverter

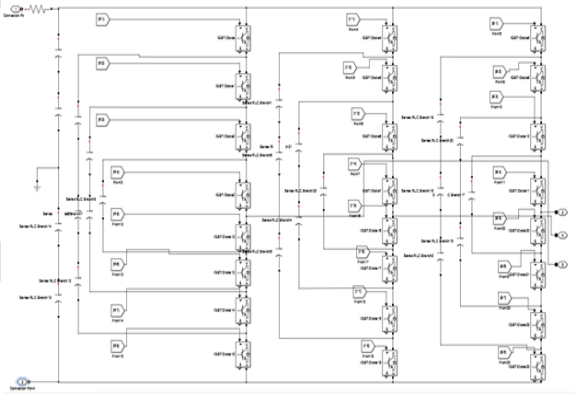


Fig.7 Simulink diagram of 5L inverter

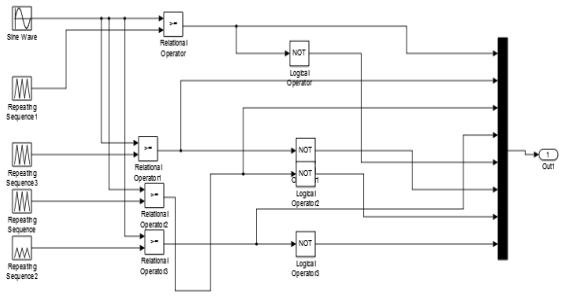


Fig.8 Pulse generation for 5L inverter

A. Analysis of Three level inverter with PD-SPWM

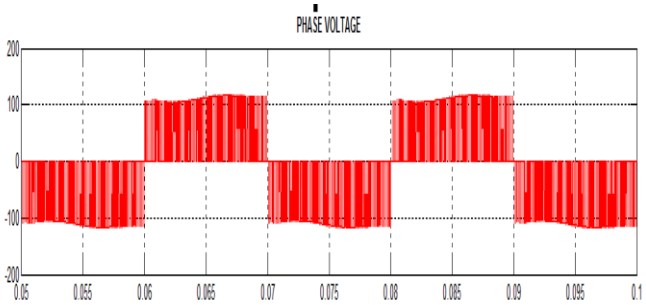


Fig. 9 Output voltage for one phase

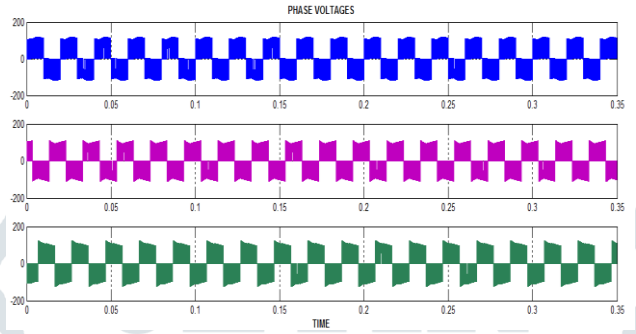


Fig. 10 Three phase output voltages

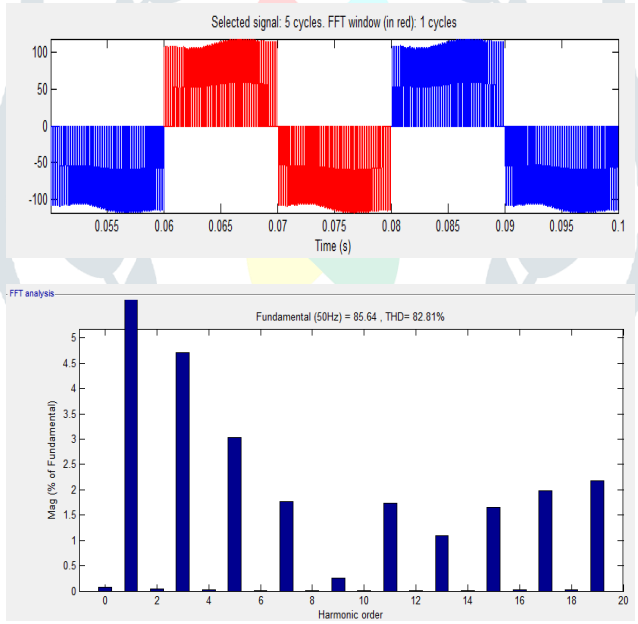


Fig. 11Harmonic of phase voltage

The above Fig. 9 shows Phase voltage of three level inverter with PD CBPWM for one phase.

The performance of the inverter is validated using harmonic spectrum of phase voltage and is found as 82.81% which is shown in Fig.11.

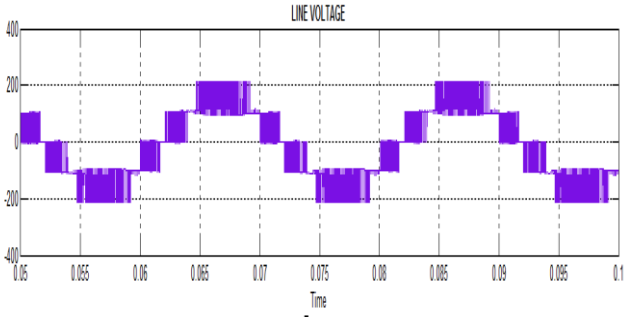


Fig. 12 Output voltage for one line

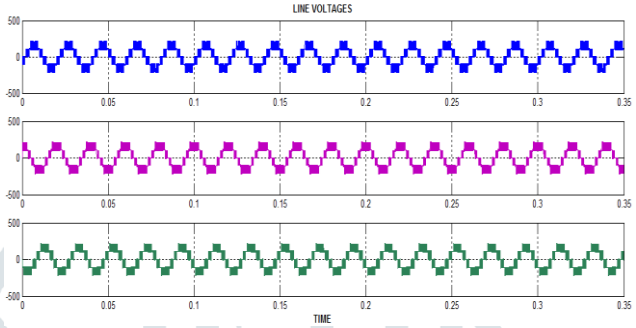


Fig. 13 Output line voltages

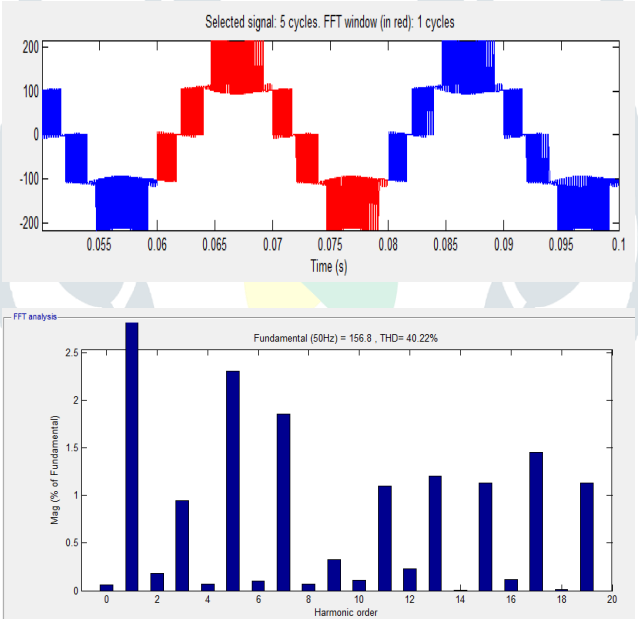


Fig. 14 FFT analysis of line voltage

The Fig. 12shows line voltage of three level inverter with PD CBPWM. To validate the performance of the inverter, FFT analysis is done on the output line voltage and is found to be 40.22%.

B. Analysis of Three level inverter with POD CBPWM

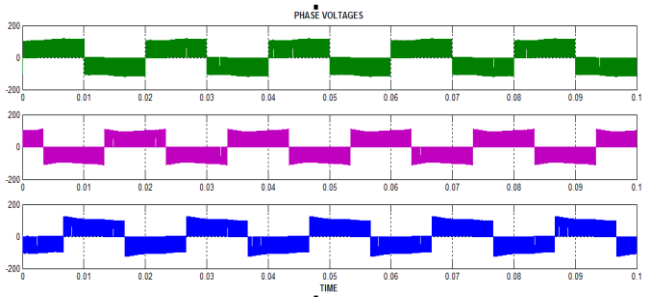


Fig.15 Output phase voltages

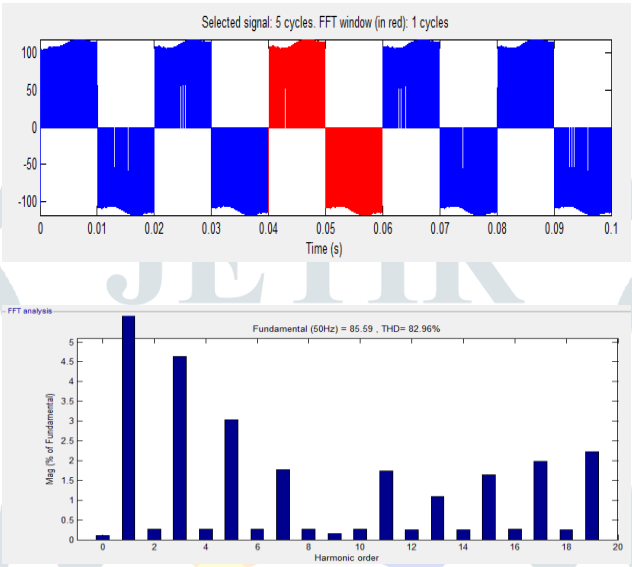


Fig.16 FFT analysis of phase voltage

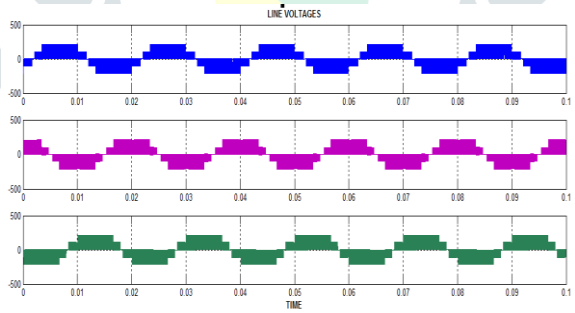
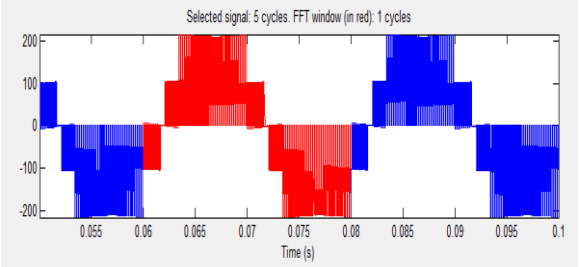


Fig.17 Output line voltages



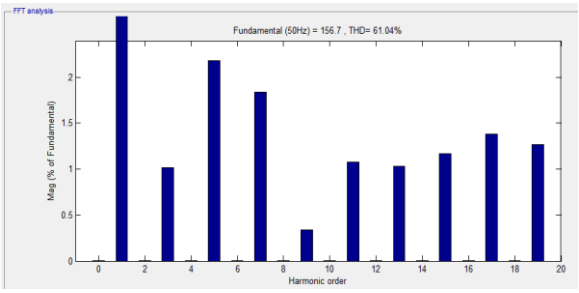


Fig.18 FFT analysis of line voltage

Fig. 15 and Fig. 17 shows simulation results of phase and line voltages of the three level inverter employing POD CBPWM. FFT analysis shows the THD in phase voltage and line voltage to be 82.96% and 61.04% respectively.

B. Analysis of Five level inverter with PD CBPWM

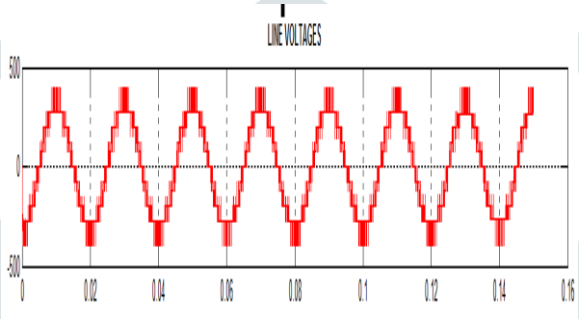


Fig.19 Output voltage for one line

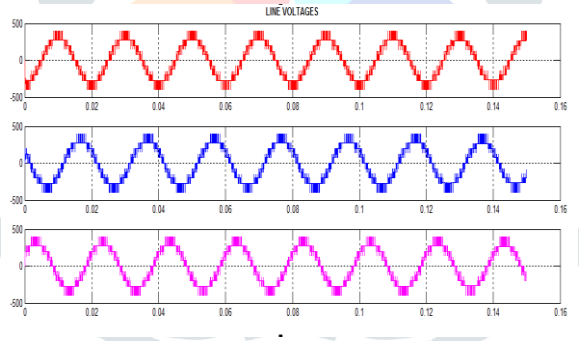
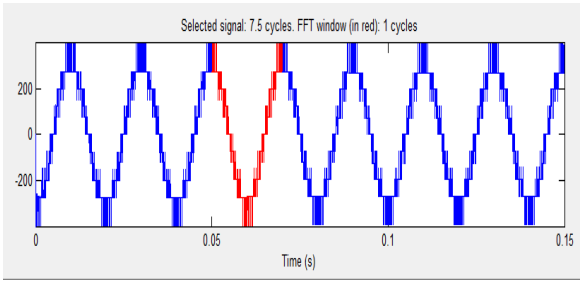


Fig. 20 Output line voltages



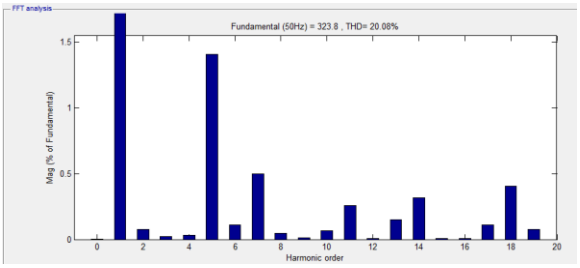


Fig.21 FFT analysis of line voltage

Fig. 21 shows FFT analysis on line voltage of 5 level inverter with PD CBPWM. It is found to be 20.08%.

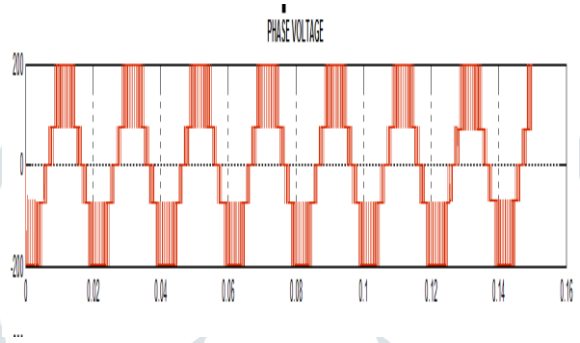


Fig. 22 Output phase voltage for one phase

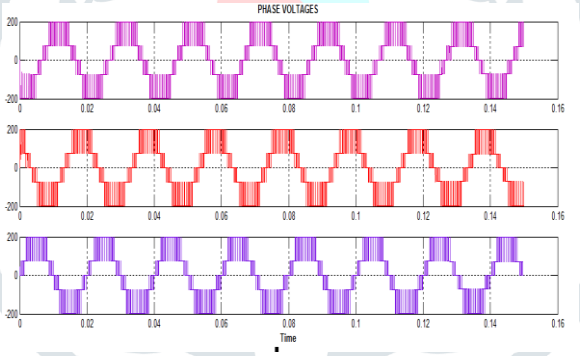
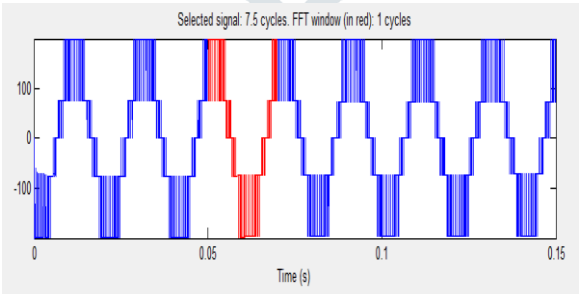


Fig.23 Output phase voltages



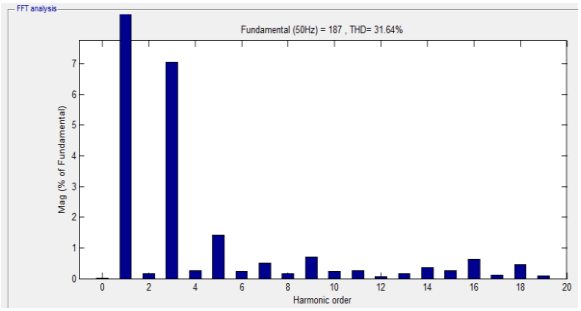


Fig.24 FFT analysis of phase voltage

Similarly, FFT analysis on phase voltage of 5 level inverter with PD CBPWM is proved to be 31.64%.

C. Analysis of Five level inverter with POD CBPWM

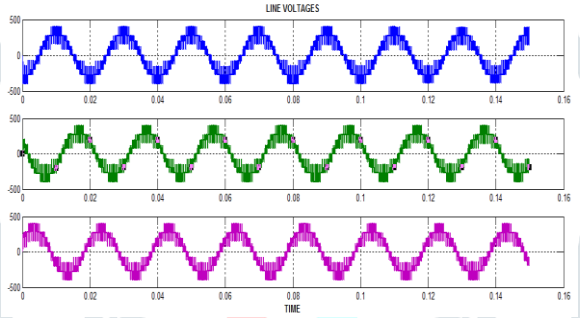


Fig.25 Output line voltages

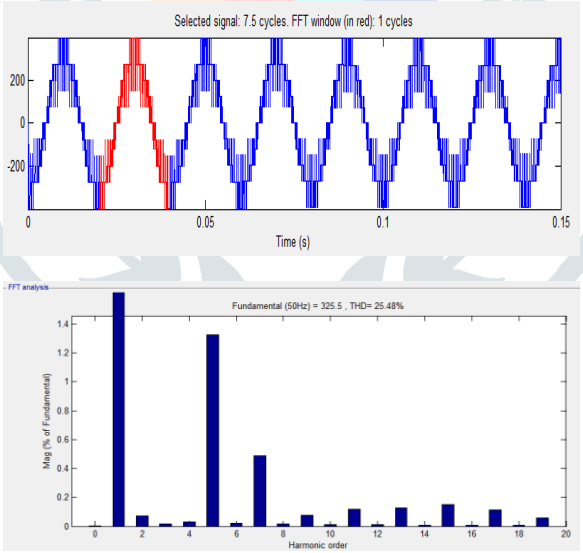


Fig.26 FFT analysis of line voltage

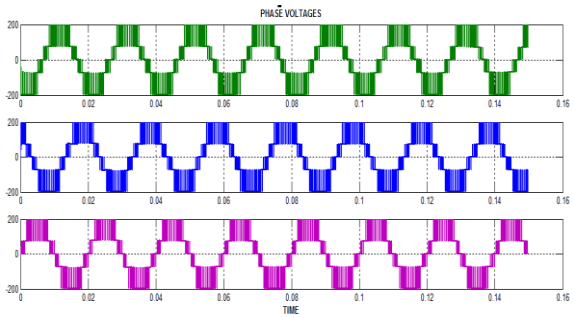


Fig.27 Output phase voltages

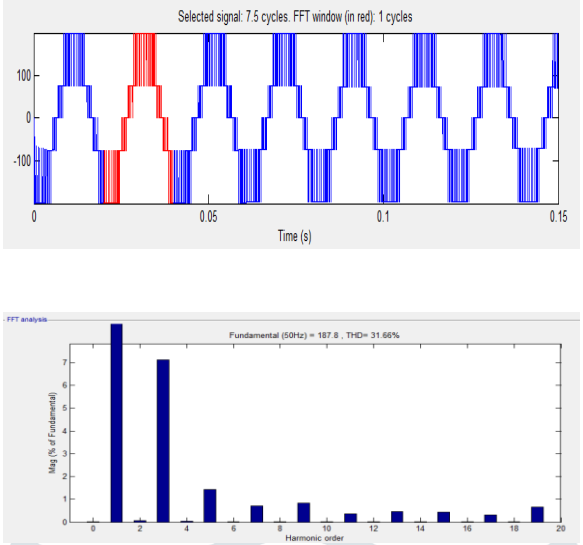


Fig.28 FFT analysis of phase voltage

Fig. 26 and Fig. 28 shows FFT analysis on line and phase voltages of 5 level inverter with POD CBPWM and are25.48% and 31.66% respectively.

Table.3: Results Of Three Level and Five level FCMLI With PD and POD CBSPWM Control Schemes.

S. No.	Control Scheme	% THD			
		3 LEVEL		5 LEVEL	
		PHASE VOL-TAGE	LINE VOL-TAGE	PHASE VOL-TAGE	LINE VOL-TAGE
1.	PD CB SPWM	82.81	40.22	31.64	20.08
2.	POD CB SPWM	82.96	61.04	31.66	25.48

The above Table.3 presents a comparative study of performance of 3 level and 5 level Capacitor Clamped Multilevel Inverter with PD CBPWM and POD CBPWM. From this table, it is evident that the %THD in the output voltage is low when PD CBPWM control scheme is employed. At the same time, 5 level inverter shows better performance compared to 3 level inverter.

IV. CONCLUSION

The 3-level and 5-level Flying Capacitor based Inverters are simulated using Carrier Based SPWM technique. For the purpose of evaluation of the performance of both the inverters, simulations were carried out employing Phase Disposition and Phase Opposition Disposition Carrier Based PWM techniques for Three and Five level inverters. The simulation results show that the THD in the inverter voltage is reduced when the voltage level is boosted. Also, the THD in the output voltage is less with PD method when compared to POD method. It is concluded that the performance of 5-level inverter with PD CBPWM method is better compared to POD CBPWM method and is superior than that of 3-Level inverter.

REFERENCES

1. J. Rodriguez, J.S. Lai and F.Z. Peng," Multilevel inverters: A survey of topologies, Control and Applications", IEEE Trans.Industrial Elecronics, Vol.49,No.4 pp.724-738,2002.

2. L.Xu, and V.G .Agelidisd, "Active capacitor voltage control of flying capacitor multilevel converters", IEE Proc. Electr. Power Appl., vol. 151, no.3, pp. 313-320, May. 2004.

3. C.Feng, J.Ling, and V.G.Angelidis, "Modified phase shifted PWM control for flying capacitor multilevel converters", IEEE Trans. Power Electron., vol. 22, no.1, pp. 0178-0185, Jan. 2007.

4. Sourabh Rathore, Mukesh Kumar Kirar and S.K Bhardwaj," Simulation of Cascaded H-Bridge Multilevel Inverter using PD, POD, APOD Techniques", Electrical & Computer Engineering: An International Journal (ECIJ) Volume 4, Number 3, September 2015.

5. A.M.Y.Ghias, J.Pou, M.Ciabotaru, and V.G.Agelidis, "Voltage balancing method for the multilevel flying capacitor converter using phase-shift PWM", IEEE Intern. Conf. on Power and Energy, vol. 2, pp. 0274-0279, Dec. 2012.

6. A.Shukla, A.Ghosh, and A.Joshi, "Static shunt and series compensation of an SMIB system using flying capacitor multilevel inverter ", IEEE. Trans. Power Del., vol. 20, no.4, pp. 2613-2622, Oct 2005.

7. L.Zhang, and S.J.Watkins, "Capacitor voltage balancing in multilevel flying capacitor inverters by rules-based switching pattern selection", IET. Electron. Power Appl., vol. 1, no.3, pp. 339-347, May. 2007.

8. F. Salinas, M. A. González, and M. Escalante," Voltage balancing scheme for flying capacitor multilevel converter", IET. Electron. Power, vol. 6, pp. 835-842, Feb. 2013.