A Novel Design of Merging Flip-Flop With Adaptive Clock Gating

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Abstract : Adaptive Clock-Gating (ACG) and Merging Flip-Flops in which several FFs are grouped and share a common clock driver are two effective low-power design techniques. Combining these techniques into a single grouping algorithm and design flow enables further power savings. We study MBFF multiplicity and its synergy with FF data-to-clock toggling probabilities. A probabilistic model is implemented to maximize the expected energy savings by grouping FFs in increasing order of their data-to-clock toggling probabilities. The clock signal driving a FF is disabled when the FFs state is not subject to change in the next clock cycle. Data-driven gating is causing area and power overheads that must be considered. In an attempt to reduce the overhead, it is proposed to group several FFs to be driven by the same clock signal, generated by enabling the clock signals of the individual FFs. Pseudorandom bit generators (PRBGs) are widely used in many electronic equipment, thus many researchers are proposing novel solution addressed to improve the inviolability performances required in cryptographic applications. LFSR is the most used topology to implement PRBG.

Index Terms **- Clock gating (CG), clock network synthesis, low-power design, Merging flip-flop.**

I. INTRODUCTION

The data of digital systems are usually stored in flip-flops (FFs), each of which has its own internal clock driver. In an attempt to reduce the clock power, several FFs can be grouped into a module called a multi bit FF (MBFF) that houses the clock drivers of all the underlying FFs. We denote the grouping of *k*FFs into an MBFF by a *k*-MBFF. Kapoor *et al.* [1] reported a 15% reduction of the total dynamic power processor design. Electronic design automation tools, such as Xilinx Liberate, support MBFF characterization. The benefits of MBFFs do not come for free. By sharing common drivers, the clock slew rate is degraded, thus causing a larger short-circuit current and a longer clock-to-*Q* propagation delay *t*pCQ. To remedy this, the MBFF internal drivers can be strengthened at the cost of some extra power. It is therefore recommended to apply the MBFF at the RTL design level to avoid the timing closure hurdles caused by the introduction of the MBFF at the backend design stage. Due to the fact that the average data-to-clock toggling ratio of FFs is very small [2], which usually ranges from 0.01 to 0.1, the clock power savings always outweigh the short-circuit power penalty of the data toggling.

An MBFF grouping should be driven by logical, structural, and FF activity considerations. While FFs grouping at the layout level have been studied thoroughly, the front-end implications of MBFF group size and how it affects clock gating (CG) has attracted little attention [3]. This brief responds to two questions. The first is what the optimal bit multiplicity k of data-driven clock-gated (DDCG) MBFFs should be. The second is how to maximize the power savings based on data-to-clock toggling ratio (also termed activity and data toggling probability).

One of the major dynamic power reduced by clock gating method in computing and consumer electronics products in the overall system's clock signal then reduce the 30%–70% of the total dynamic power consumption and then reduce the overall circuit power to reduce15- 20% of Grouping Flip Flop data driven clock gating method [4]. Clock gating is major method of educing clock signal. Generally, when a logic unit is clocked, it is based on the sequential elements receiving the clock signal, sequentially they will toggle in the next cycle whether it is required or not. The data driven clock gating circuit using clock enabling signals are manually added for every FF as a part of a design methodology [5].

In this paper, a model for data-driven gating is developed based on the toggling activity of the constituent FFs. The optimal fan out of a clock gate yielding maximal power savings is derived based on the average toggling statistics of the merging FFs, process technology, and cell library in use. In general, the state transitions of FFs in digital systems depend on the data they process. Assessing the effectiveness of data-driven clock gating requires [6], therefore, extensive simulations and statistical analysis of the FFs activity. Another grouping of FFs for clock switching power reduction, called Multi bit FF (MBFF). MBFF attempts to

physically merge FFs into a single cell such that the inverters driving the clock pulse into its master and slave latches are shared among all FFs. MBFFs the advantages are [7]: 1) smaller design area due to shared clock drivers and less routing resource 2) Less delay and less power of clock network due to fewer clock sinks 3) Controllable clock skew because of common clock and enable signals for the group of flip flops and reduced depth of a clock tree.

II. DATA DRIVEN CLOCK GATING:

An MBFF grouping should be driven by logical, structural, and FF activity considerations. While FFs grouping at the layout level have been studied thoroughly, the front-end implications of MBFF group size and how it affects clock gating (CG) has attracted little attention [8]. This brief responds to two questions. The first is what the optimal bit multiplicity k of data-driven clock-gated (DDCG) MBFFs should be. The second is how to maximize the power savings based on data-to-clock toggling ratio.

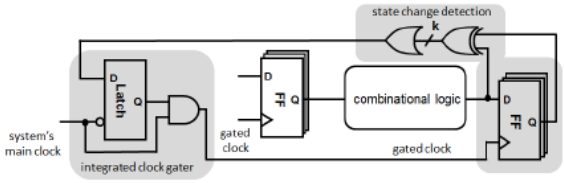


Fig.1. DDCG integrated into a *k*-MBFF

Fig. 1 illustrates a DDCG integrated into a *k*-MBFF. The shaded circuits reside within a library cell. Given an activity *p*, the group size *k* that maximizes the energy savings solves the equation

$$(\mathbf{1}-\boldsymbol{p})^{\boldsymbol{k}}\,\boldsymbol{ln}(\mathbf{1}-\boldsymbol{p})\boldsymbol{C_{FF}}+\frac{\boldsymbol{C_{latch}}}{\boldsymbol{k^2}}=\mathbf{0} \qquad \textbf{(1)}$$

where C_{FF} and C_{latch} are the clock input loads of an FF and a latch, respectively. The solution to (1) for various activities is shown in Table I for typical C_{FF} and C_{latch}. The above optimization does not take into account the clock driver sharing, which also affects the optimal grouping as shown below. To grasp the power savings of a *k*-MBFF achievable by DDCG, Fig. 1 was simulated with SPICE for various activities *p* and *k* = 2, 4, 8.

Clearly, the best grouping of FFs that minimizes the energy consumption can be achieved for FFs whose toggling is highly correlated. Using toggling correlations for MBFF grouping has the

drawback of requiring early knowledge of the value change dump vectors of a typical workload. Such data may not exist in the early design stage. More commonly available information is the average toggling bulk probability of each FF in the design, which can be estimated from earlier designs or the functional knowledge of modules. FFs' toggling probabilities are usually different from each other. An important question is therefore how they affect their grouping. We show below that data-to-clock toggling probabilities matter and should be considered for energy minimization.

In data driven clock gating methodology is used to reduce the power consumption and reduce the delay of the circuit. The data driven clock gating is power reducing using in merging flip flop and integrated clock gating circuit. The block diagram of merging flip flop using data driven clock gating circuit is shown in fig 2. The ICG is disable then the output of state change detector is input of the ICG circuit. State change detector is XORed output and k enabling signal of the Flip Flop, by ORed the input of ICG circuit.

The arithmetic circuit is used by logic circuit of data driven clock gating circuit. The merging Flip-flop reduces the unwanted clock signal of circuit. The unwanted glitches are reduced in data driven clock gating circuit

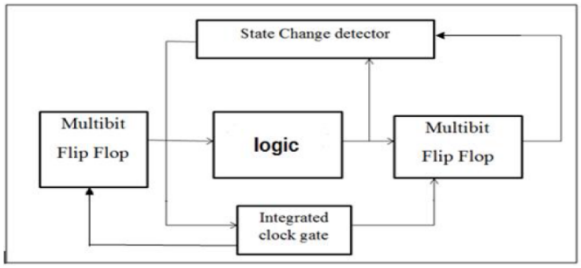


Fig. 2 Block diagram of merging flip flop using data driven clock gating

III. Adaptive Clock Gating

An adaptive clock gating circuit is shown in Fig. 3. By XORing gate its output with the present input of Integrated Clock Circuit that will appear at its output in the next clock cycle, an FF checks whether its state is subject to change, thus finding out whether its clock can be disabled in the next cycle. The outputs of k XOR gates are ORed and then latched to generate a joint gating signal for k FFs [2]. The combination of a latch With AND gate is called Integrated Clock Gate (ICG), commonly used by industrial electronic design automation (EDA) tools. The practical Data Driven Clock Gating block diagram is given above. The function of module list is given that State Change Detector, Merging Flip-Flops and Integrated Clock Gating.

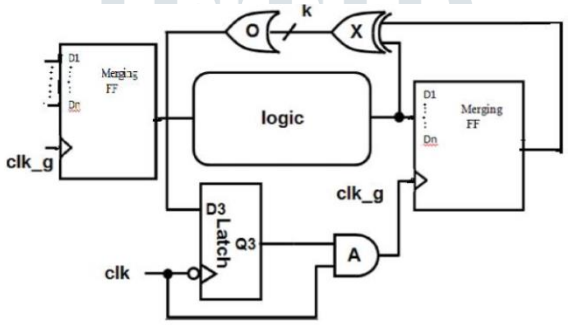


Fig. 3 Circuit diagram of practical Adaptive Driven Clock Gating

A. Clock Gating

Clock gating circuit is power consumed by 50 % of dynamic power. The clock gating reduce dynamic power by combinational logic circuit and then the circuit reduce clock pulse and sharing the clock signal in merging flip-flops and reduce clock signal[9]. The profitable EDA tools are supported clock gating technique. There are two types of clock gating technique. They are Latch-based clock gating and Latch-free clock gating. The latch-free clock gating technique uses a simple AND or OR . The latch-based clock gating technique is a level-sensitive. In this project using in latch based clock gating technique. The latch-based clock gating technique is called Integrated Clock Gate (ICG). The Integrated Clock will be disables in the next cycle by XORing the output of the present data input and it will reveal at the output in the next cycle. Then the output of the XOR gates are ORed for generating the gate signal for the FF's which is to be used to avoid the glitches. The Integrated clock gate (ICG) can be used by the environmental tools by the combination of LATCH with the AND gate. These latches could be used in ultra-low power applications for a digital filter. The data driven clock gating signal are being used as an enabling signals in this applications. There will be a trade-off for ICG is the number of clock pulses could be disabled. The pulses could also be a trade-off for the hardware over-head. While increase the number of flip-flops the hardware overhead decreases to obtain by ORing the enable signals. The level of this high and the low state of signals could be processed in the same versa to give the proper output.

B. Merging Flip-Flops

Merging Flip-Flops is an effective method to reduce clock power consumption [10]. Merging Flip-Flops can significantly reduce the number of individual loads on the clock tree, reducing overall dynamic power used in the clock tree. Area and leakage power saving can also be achieved simply by sharing the clock inverters in the flip flops with a single structure [11]. Merging Flip-Flops provide a set of additional flops that have been optimized for power and area with a minor trade-off in performance and placement flexibility [12]. The Flip flops share a common clock pin, which decrease the overall clock loading of the N Flops in

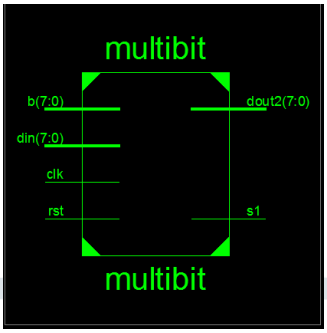
the Merging Flip-Flops cell, reduces area with a corresponding reduction in leakage and reduce dynamic power on the clock tree significantly.

C. State Change detector

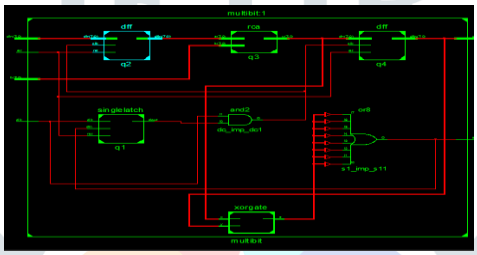
State Change detector is detecting the high state or low state. The high state is denoted by '1'and low state is denoted by '0'. The state change modification process depends on the outputs of merging FFs and combinational logic outputs. State Change detector module made up-off XOR gate and OR gate.

IV. Results And Discussion

Block Diagram:

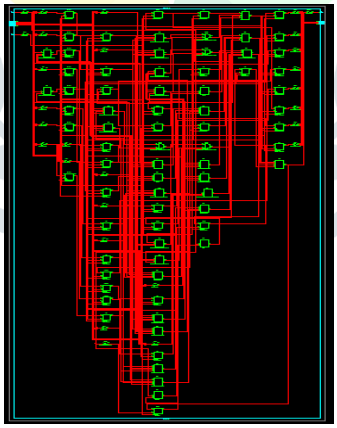


RTL schematic:



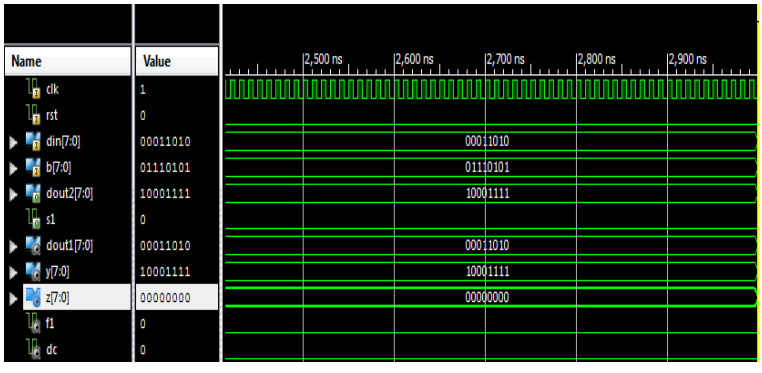
The above figure shows the RTL schematic of the Design. In this Design we can observe the internal modules of the Design.

Technology Schematic:



The above figure shows the Technology schematic of the Design. In this Design we can observe the Look up tables (LUTs) modules of the Design.

Output:



The above figure shows the simulation results of the Design. In this Design we can observe the input and output waveforms. From the comparison table shown below the proposed design proves to be better in terms of power and area.

COMPARISON TABLE

TABLE 1:

Parameters	Existing system	Proposed system
Area (Luts)	62	31
Power (mW)	89mw	63mw

V. Conclusion

The objective of the system is to reduce the area and power of data driven clock gating technique. In proposed method using merging FFs for combined clock gating is used for dynamic power savings. Analysed, the results of grouping and merging FFs architectures, simulation and synthesis. As the result of the area, delay parameters, grouping FF using data driven clock gating is more effective than the merging FF using data driven clock gating. In case of grouping FFs using data driven clock gating is extraordinary power saving for merging FFs using data driven clock gating. In this paper, analysis between grouping FFs using data driven clock gating and merging FFs using data driven clock gating. Furthermore, real time application of DSP cores, a network processor control block, and a 3-D graphics accelerator using in merging FFs using data driven clock gating in an attempt to yield further power savings.

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