4-BIT BURST ERROR CORRECTION WITH EFFICIENT DECODING BY USING DOUBLE ERROR CORRECTION CODE

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Abstract: **There has been recent interest on designing Double Error Correction (DEC) codes for 32-bit data words that support fast decoding as they can be useful to protect memories. To that end, solutions based on Orthogonal Latin Square codes have been recently presented that achieve fast decoding but require a large number of parity check bits. In this letter, a DEC code derived from Difference Set codes is presented. The proposed code is able to reduce the number of parity check bits needed at the cost of a slightly more complex decoding. Therefore, it provides memory designers with an additional option that can be useful when making trade-offs between memory size and speed.**

Index Terms **– Error correction codes, memories, Difference Set codes, Orthogonal Latin Square codes.**

1. INTRODUCTION

Error Correction Codes (ECCs) are commonly used to protect memories so that errors do not affect the data they store. Traditionally, Single Error Correction-Double Error Detection (SEC-DED) codes have been used, but as technology scales there is a need for more powerful error correction capabilities, for example Double Error Correction (DEC) codes. This poses a problem as parallel decoders for traditional DEC codes are much more complex and result in a significant increase in area, power and delay compared to the SEC-DED codes. This has motivated the use of alternative DEC codes that can be efficiently decoded using one step majority logic voting, such as Difference Set (DS) or Orthogonal Latin Square (OLS) codes. The main limitations of these codes are that only one block length is supported in the case of DS codes while DEC OLS codes require significantly more parity check bits.

Arranging the data into a matrix form at the logical level and then adding several simple ECCs in different directions can also provide a powerful error correction capability for memories. For example, Horizontal Vertical Diagonal (HVD) codes and Matrix codes have been proposed. These codes can be decoded with limited complexity but unfortunately have a large number of parity check bits that increase the memory size.SRAM reliability faces serious challenges from radiationinduced soft errors (transient faults induced by ionizing radiation) and process-variation-induced defects in sub-100nm technologies. SRAM cells are designed with minimum geometry devices to increase density and performance, resulting in reduced critical charge to upset cells and more pronounced effects from process variations. Therefore, it has become conventional to protect memories with the application of error correcting codes (ECC) such as single-error correcting (SEC) Hamming code, single-error-correcting double-error-detecting (SEC-DED) extended-Hamming, or SEC-DED Hsiao codes. With multi-bit upsets (MBU) becoming a major contributor to soft errors, conventional SEC or SEC-DED codes may not be sufficient to meet reliability goal. To mitigate these effects, the use of more powerful ECC and/or memory scrubbing with conventional ECC are being suggested. SEC-DED codes also have a relatively low performance overhead which makes them an ideal candidate for the protection of main and cache memories.

Especially, SEC-DED codes with fixed code word parity enable efficient hardware implementations since they facilitate the double error detection. Another factor that influences the latency of these codes is the density of the parity-check matrix, also called H-matrix, which is defined as the percentage of 1-elements with respect to the total number of matrix elements .Here, we propose a way to reduce the H-matrix density for SEC-DED codes with fixed code word parity based on a generalization of the restrictions used until now. We prove that the fixed code word parity is ensured if a subset of H-matrix rows can be found such that it intersects each H-matrix column in an odd number of 1-elements. Hsiao and extended Hamming H-matrices correspond to the extreme cases when this subset contains only one or all matrix rows, respectively. The reported experimental results prove that the generalized H-matrices enable faster implementations. Such generalizations can be applied to reduce the H-matrix density of any linear block code with fixed parity.

Error detection and correction codes play a key role in memory protection and reliability improvement. These codes are usually implemented in hardware, but require extended memory bus architecture to accommodate parity bits and additional encoding/decoding circuitry. The reliability issue can be solved using other forms of redundancy than hardware redundancy because hardware redundancy schemes like duplication or triple modular redundancies are expensive. In low-cost satellite projects, the reliability of a system can be improved by cost effective software error detection and correction code schemes. An important advantage of using software-based code scheme is that, one can change it dynamically to meet the observed response of the memory devices. This is particularly beneficial when, as is often the case in low-cost satellite design, there is little chance to test the devices prior to flight.Although SEUs are the major concern in space and terrestrial applications, multiple bit upsets (MBU) and multiple event transient (MET) are also became important problem in designing memories because of these points:

(1) Scaling down technology to increases the error rate.Therefore the probability of having multiple errors increases.(2) MBUs, METs can be induced by direct ionization or nuclear recoil after passing a high-energy ion.

(3) The experiments in memories under proton and heavy ions fluxes show the probability of having multiple errors is increased when the size of memory is increased. Therefore, achieving acceptable reliability levels for modern VLSI chips is a key issue. Unfortunately, packaging and shielding cannot effectively be used to shield against soft errors since they may be caused by neutrons which can be easily penetrate through packages. In order to maintain good level of reliability, it is necessary to protect memory cells using protection codes.One of the most common data memory widths is 32-bit.Unfortunately, there is no DEC DS or OLS code with that data block size. This has motivated the development of OLS based solutions that provide fast decoding but require a significant number of parity check bits. In this letter, a DEC solution for 32 data bit words based on DS codes combined with SEC-DED codes is proposed

and evaluated. The results show that the scheme can reduce the number of parity check bits at the expense of a moderate increase in the decoder complexity.

This paper is organized as section II describes Litarature review and in section III discussed about Proposed System and Section IV describes shows the simulation results and comparison between existing and proposed methods and section V concludes the paper followed by references.

2. LITARATURE REVIEW

[1] V. Gherman, S. Evain, N. Seymour, and Y. Bonhomme, Generalized parity check matrices for SEC-DED codes with fixed parity, in Proc. IEEE on Line Testing Symp., July 2011.

Single Error Correction-Double Error Detection (SEC-DED) codes provide an effective way to increase the reliability of semiconductor memory subsystems[1]. For example, any type of one chip failure can be masked and two chip failures can be detected in SECDED-protected memory subsystems if each bit of any code word is stored in a different memory chipSEC-DED codes also have a relatively low performance overhead which makes them an ideal candidate for the protection of main and cache memories. Especially, SEC-DED codes with fixed code word parity enable efficient hardware implementations since they facilitate the double error detection. Another factor that influences the latency of these codes is the density of the parity-check matrix, also called H-matrix, which is defined as the percentage of 1-elements with respect to the total number of matrix elements. Nowadays, only extended Hamming and Hsiao H-matrices are available to implement SEC-DED codes with fixed code word parity. In an extended Hamming H-matrix, the fixed code word parity is encoded with the help of an all-one row, while in a Hsiao H-matrix, this is ensured by the restriction to have only columns with an odd number of 1-elements. In general, the Hsiao H-matrices enable faster implementations due to a lower density and to a more uniform distribution of the 1-elements over the matrix rows.Here, we propose a way to reduce the H-matrix density for SEC-DED codes with fixed code word parity based on a generalization of the restrictions used until now. We prove that the fixed code word parity is ensured if a subset of H-matrix rows can be found such that it intersects each H-matrix column in an odd number of 1-elements. Hsiao and extended Hamming H-matrices correspond to the extreme cases when this subset contains only one or all matrix rows, respectively. The reported experimental results prove that the generalized H-matrices enable faster implementations.

[2] R. Naseer and J. Draper, DEC ECC design to improve memory reliability in sub 100 nm technologies, Proc. IEEE ICECS, pp. 586-589, 2008. SRAM reliability faces serious challenges from radiation induced soft errors (transient faults induced by ionizing radiation) and process-variation-induced defects in sub-100nm technologies. SRAM cells are designed with minimum geometry devices to increase density and performance, resulting in reduced critical charge to upset cells and more pronounced effects from process variations. Therefore, it has become conventional to protect memories with the application of error correcting codes (ECC) such as single-error correcting (SEC) Hamming code, single-error-correcting double-error-detecting (SEC-DED) extended-Hamming, or SEC-DED Hsiao codes. With multi-bit upsets (MBU) becoming a major contributor to soft errors, conventional SEC or SEC-DED codes may not be sufficient to meet reliability goals. To mitigate these effects, the use of more powerful ECC and/or memory scrubbing with conventional ECC are being suggested.BCH (Bose-Chaudhuri-Hocquenghem) codes are a class of powerful random error-correcting cyclic codes. Although BCH codes have been used in communication systems, they are typically not applied in high-speed memory applications due to their relatively large redundancy requirements and decoding complexity. For example, Table I shows the amount of redundancy required by SEC-DED and double error-correcting (DEC) BCH codes for typical data widths.

[3] C. Argyrides, D.K. Pradhan, T. Kocak, Matrix Codes for Reliable and Cost Efficient Memory Chips, IEEE Transactions on Very Large Scale Integration Systems, vol. 19, No. 3, 2011, pp.420-428. As CMOS process technology scales, high-density, low-cost, high-speed integrated circuits with low voltage levels and small noise margins will be increasingly susceptible to temporary faults. In very deep sub micrometer technologies, single-event upsets (SEUs) like atmospheric neutrons and alpha particles severely impact field-level product reliability, not only for memory, but for logic as well. When these particles hit the silicon bulk, they create minority carriers which if collected by the source/drain diffusions, could change the voltage level of the node.This issue has drawn a growing attention from the fault tolerance community due to the recent increase of the soft error rate of combinational logic circuits.

[4] S. Liu, Y. Xiao, G.Mao, Extend orthogonal Latin square codes for 32 bit data protection in memory applications, Microelectronics Reliability, Elsevier, vol. 63, August 2016, pp. 278-283. Soft errors caused by radiation particles have become a serious reliability concern for memories used in space. The state of a memory cell that is affected by the errors can be upset, which may cause serious accidents in a spacecraft, including the loss of information, functional failure, or loss of control. For many years, error correction codes (ECCs) have been traditionally used to protect memories against soft errors.

The organization of a memory protected by ECCs are shown in Fig. 1. R additional cells that store the parity bits are added to each k bit word in the memory array. The encoder turns the k-bit data into an n-bit code word, where n = k + r, then for the errors in the code word, the decoder can correct them and output the original k-bit data if the code has an enough correction capability. The number of parity bits and complexity of encoder and decoder circuits decide the overhead of system. Single error correction-double error detection (SEC-DED) codes are the typical alternative due to their simple implementation.

However, as technology scales down, the radiation induced charge can be shared by several nodes in a cell or several neighboring memory cells. It is more likely that a single radiation particle bit will upset multiple cells, which is known as multiple cell upsets (MCUs).

3. PROPOSED METHOD

A. Algorithm

Step 1:

The binary 16-bit input data bits are given to SEC-DED encoder .

Step 2:

The SEC-DED encoder generates block wise parity bits i.e., first block and second block generates five parity bits. But difference set codes(DS) generates nine parity bits.

Step 3:

Encoder output parity bits are given as input to the SEC-DED error corrector along with the input binary data bits .

Step 4:

Whenever the SEC-DED error corrector is activated then use the correction signal from the DS code to perform

correction. Whenever the SEC-DED error corrector is not activated ,then use the correction signal from the SEC-DED code to perform correction.

Step 5:

Brust errors are used to correct four biterrors ,if the number of binary data inputs increases parity bits generation decreases.

B. Encoding

The only DEC DS code that exists is a (21,11) code that is One Step Majority Logic Decodable (OS-MLD) and can correct double errors and detect triple errors. The proposed scheme is based on this code that is firstly optimized by removing one parity bit to obtain a (20, 11) DEC code that is also OS-MLD but that cannot detect triple errors. To explain the proposed code, we will first describe the encoding process illustrated in fig 5.1. It can be seen that the 32-bit data word is divided into three blocks, the first consists of bits 1 to 11, and the second of bits 12 to 22 and finally the third block includes bits 23 to 32. Therefore, the first two blocks have 11 bits and the last one only 10 bits. The xor of the blocks is used as an input to a (20, 11) DS encoder to obtain 9 parity check bits, s1d, s2d... s9d.

The first and second data blocks are fed into two SEC-DED encoders to obtain other two groups of 5 parity check bits: s1a, s2a... s5a and s1b, s2b... s5b. As a result of the encoding, we obtain 19 parity check bits. This compares favorably with previous proposals based on OLS codes that require 21 to 23 parity check bits[2].

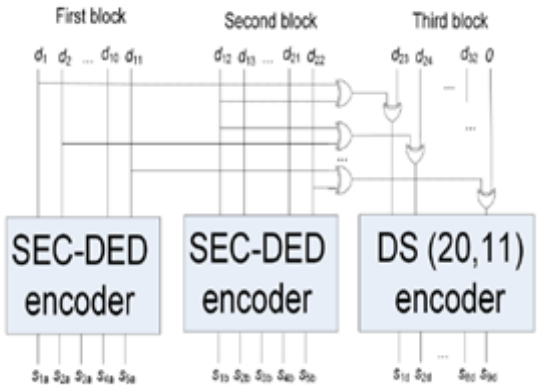

Fig 1: Proposed Encoding Technique

C. Decoding

For the bits in the first and second blocks, the correction of the data bits can be implemented as follows: If the DED is not activated, then use the correction signal from the SEC-DED code to perform correction. In this case, there can be at most one bit in error in the block and therefore the SEC correction signal can be used.

If the DED is activated, then use the correction signal from the DS code to perform correction. In this case, there cannot be errors on the other blocks as we assume a maximum of two errors. Therefore, the DS correction signals for the two bits will be activated and can be used for correction.

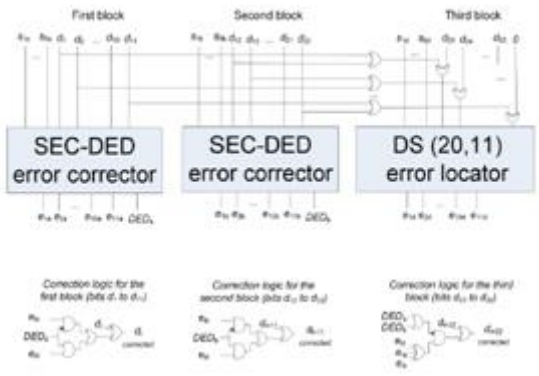

Fig.2: Proposed Decoding technique

D. Bit Error correction

In the following, two solutions to provide 4-bit burst error correction are described. The first one is based on the interleaving of SEC-DAEC codes while in the second optimized4-bit burst error correction codes are presented**.**

i. Interleaving of SEC-DAEC codes:

A well known method to construct a t-bit burst error correction code is to interleave codes with lower error correction capabilities. For example, to achieve 4-bit burst error correction for a 32 bit data word, we can divide the data bits into four blocks such that block 1 contains bits d1, d5, d9..., block 2 bits d2, d6,d10,... and so on. Then each block can be protected with a SEC code and parity bits are also placed so that bits of the same block are separated. The physical placement for this example as well as the four SEC code words marked as B1, B4 are illustrated in Figure 1. It can be easily checked that this code can correct 4-bit burst errors. The decoding is shown in Figure2 and is simple as we just need four parallel SEC decoders. However, the number of parity check bits will be large as we need four code words.

ii. Minimum redundancy 4-bit burst error correction codes

Another method to construct a 4-bit burst error correction code is based on the principle of the syndrome decoding. If one error pattern can be corrected, the corresponding syndrome should be unique. Additionally, the all zeros syndrome is needed for the error free case.

4. SIMULATION RESULTS

A. Encoding

The input binary16 bit data is given to the SEC-DED encoder , it performs the hamming code operation when single error occurs and it performs operation based on OLS codes when double error occurs SEC-DED encoder generates block wise parity bits along with difference set codes i.e., It generates totally 19 parity bits .

Fig 3. Double error correction encoder output

B. Decoding

The output of encoder is given as input to the decoder ,the input of decoder consist of both parity bits along with input binary data .If the DED is not activated, then use the correction signal from the SEC-DED code to perform correction. In this case, there can be at most one bit in error in the block and therefore the SEC correction signal can be used. If the DED is activated, then use the correction signal from the DS code to perform correction. In this case, there cannot be errors on the other blocks as we assume a maximum of two errors. Therefore, the DS correction signals for the two bits will be activated and can be used for correction.

Fig.4: Double error correction decoder output

C. Area:

The total area occupied by the SEC-DED uses 24-look up tables (LUT).

```
#      OBUF                    : 33

Device utilization summary:
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Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                  24  out of  63400     0%
    Number used as Logic:               24  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    24
   Number with an unused Flip Flop:     24  out of     24   100%
   Number with an unused LUT:            0  out of     24     0%
   Number of fully used LUT-FF pairs:    0  out of     24     0%
   Number of unique control sets:        0

IO Utilization:
 Number of IOs:                         74
 Number of bonded IOBs:                 65  out of    210    30%

Specific Feature Utilization:
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Fig.5: Area for DEC

D. Delay

The delay introduced for the SEC-DED for encoding and decoding is 1.638 ns.

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=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 182 / 32
-------------------------------------------------------------------------
Delay:               1.638ns (Levels of Logic = 4)
  Source:            d<10> (PAD)
  Destination:       dout<21> (PAD)

  Data Path: d<10> to dout<21>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             12   0.001   0.607  d_10_IBUF (d_10_IBUF)
     LUT4:I0->O            11   0.097   0.558  k2/f1/Mxor_ded1_xo<0>1 (ded1)
     LUT4:I1->O             1   0.097   0.279  k3/j2/g9/Mxor_dc_xo<0>1 (dout_19_OBUF)
     OBUF:I->O              0.000          dout_19_OBUF (dout<19>)
    ----------------------------------------
    Total                    1.638ns (0.195ns logic, 1.444ns route)
                                     (11.9% logic, 88.1% route)

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Cross Clock Domains Report:
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Fig.6. Delay for DEC

E. Power

The total power consumption for SEC-DED is 0.82 watts.

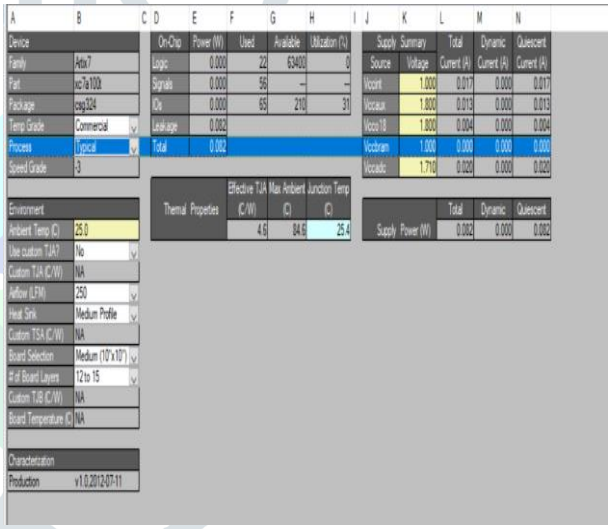

Fig.7 :Power for DEC

F. Burst errors

When the 32 bit input data is given then it reduces the number of parity bits and it corrects upto 4 bits of errors ,so that the area and power consumption will be reduced.

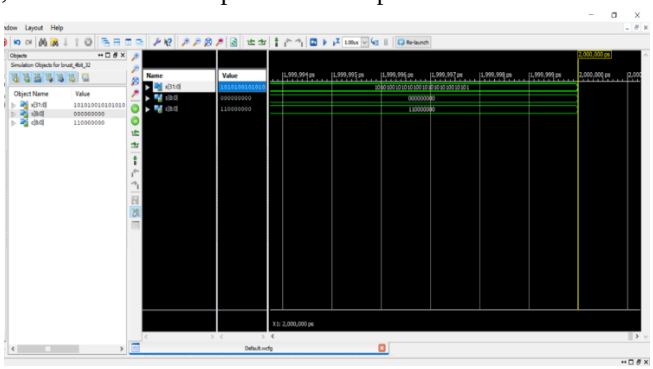

Fig.8: 4-bit burst error correction

G. Area

The total area occupied by the burst error uses 12-look up tables (LUT).

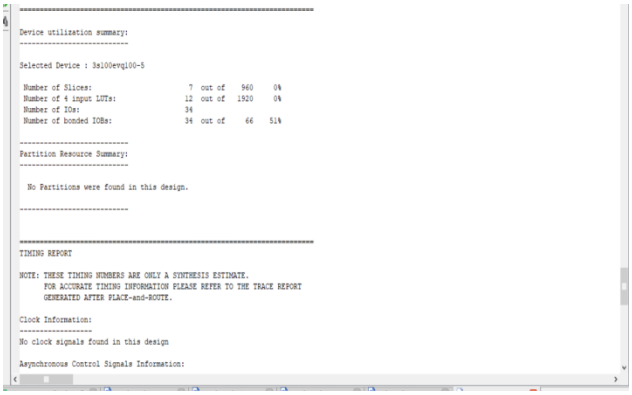

Fig.9: Area for 4-bit burst error

H. Delay

The delay introduced for the burst error for encoding and decoding is 6.99 ns .

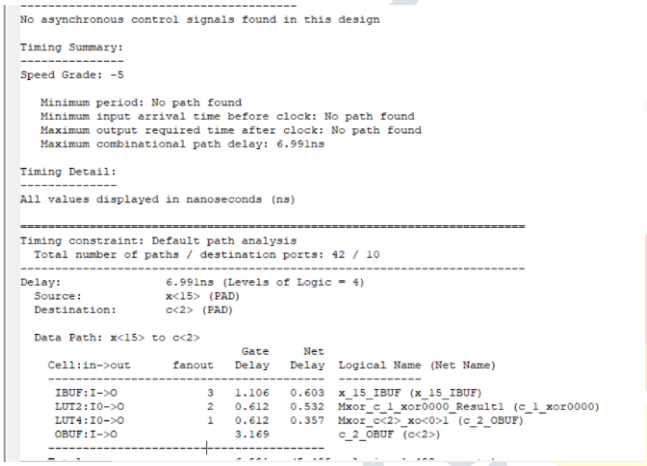

Fig.10: Delay for 4-bit burst error

I. Power

The total power consumption for burst error is 0.34 watts.

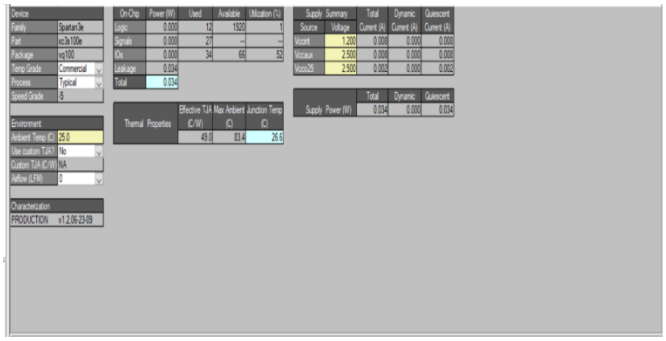

Fig.11. Power for 4-bit burst error

5. CONCLUSION

In this letter a Double Error Correction (DEC) code to protect 32 bit data word memories has been proposed. The code is based on the use of a DEC Difference Set (DS) code combined with two Single Error Correction-Double Error Detection (SEC-DED) codes. The proposed solution reduces the number of parity check bits compared to existing schemes based on Orthogonal Latin Square (OLS) codes while providing a decoding delay that is lower than that of a traditional Bose Chaudhuri Hocquenghem (BCH) DEC code. Therefore it provides memory designers with another option that can be useful to trade-off delay and memory size. This will be useful for applications that cannot tolerate the BCH decoding delay but for which existing solutions have some delay margin. Finally, the scheme proposed in this paper can be used to combine other OS-MLD DEC codes with SEC-DED codes to protect different word lengths. This is however constrained by the availability of OS-MLD DEC codes. The study of this generalization is left for future work.

Correction of error bits more than four bits are to be made easy and understandable. Correction of error bits are more complex in terms of binary bits, in the further project we can correct any form of data. Position of occurrence of errors can also be detected and corrected easily.

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