A Novel Design of Low Power and Area Efficient Line Decoder

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Abstract : Many pass-transistor logic families have been presented as of now, however no methodical synthesis technique which doesn't take signal strength on circuit execution into consideration. In the pass transistor logic, a Karnaugh based strategy which productively synthesized Pass Transistor Logic (PTL) circuits, that have adjusted loads on original and correlative complemented input signals was created. The technique was applied to the fundamental two-input and three-input logic gates in Complementary Pass Transistor Logic (CPL), Double Pass Transistor Logic (DPL) and Dual Value Logic (DVL). These techniques were general and can be reached out to blend any pass-transistor organize which expended more power[1]. In this undertaking, Complementary Pass Transistor logic is utilized which contains just NMOS transistor to construct 2-4 Decoder circuits[1]. Decoder based CPL is utilized to configuration low power memories. Use of memories is to store the data and it is one of the moderate of processor and outer interface. Since CPL is being utilized, the power is decreased. CPL based decoder for memories is planned and its performance measurements of rapid and low power is analyzed utilizing MICROWIND Tool. The proposed design of CPL is to reduce the transistor count and also achieve the better Power, area and delay performance when compared to CMOS and GDI technology based Designs.

Index Terms - Complementary metal–oxide–semiconductor (CMOS), Gate Diffusion Input (GDI),Pass Transistor Logic (PTL), Complementary Pass Transistor Logic (CPL), Static Random Access Memory (SRAM)

I. INTRODUCTION

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits. They consist of complementary N-type metal-oxide-semiconductor (nMOS) pull down and P-type metal-oxide semiconductor (pMOS) pull up networks and present good performance as well as resistance to noise and device variation[1]. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design.

Pass transistor logic (PTL) was mainly developed in the 1990s, when various design styles were introduced aiming to provide a viable alternative to CMOS logic and improve speed, power, and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors[2]. Pass transistor circuits are implemented with either individual nMOS / pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g., SRAM)[3]. In This paper we developed a mixed-logic methodology for their implementation, opting for improved performance compared to single-style design like CMOS, GDI and PTL logics.

Rest of the paper is organized as follows, in section II we portrayed the earlier designs of decoder with CMOS, GDI and PTL logics. In section III,the proposed CPL Logic based Decoder is presented and is implemented in SRAM. In section IV we displayed the experimental results. Finally in section V we conclude the paper.

II. EARLIER WORKS

CMOS technology:

CMOS comprises of complementary N-type metal oxide semiconductor nMOS (pull down) and P-type metal oxide semiconductor pMOS (pull up) systems. CMOS rationale is planned against voltage scaling and decrease in transistor quantity. It works at low voltages and little transistor sizes[5]. In CMOS logic the information sources are associated with transistor gate only so as to decrease the unpredictability of circuit plan. CMOS gadgets are high noise resistance and low static power utilization. The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation. This allows integrating many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance.

Components Design with CMOS Logic:

We can design any logic gate using CMOS logic for example in the below figure 1 we portrayed NOT, AND and OR gates

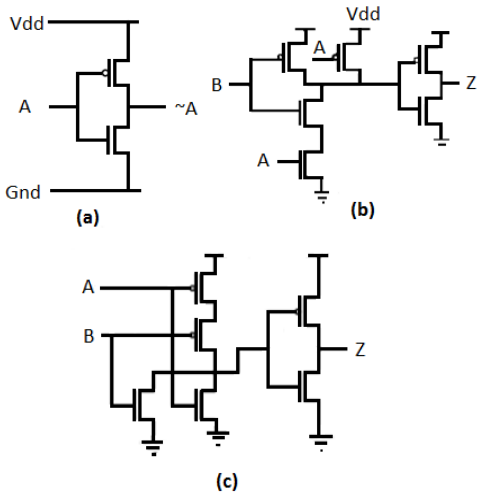


Fig.1 (a) NOT gate (b) AND gate (c) OR gate

2-4 Line Decoder:

A 2–4 line decoder produces the 4 min-terms D0−3 of 2 input factors A and B. Its logical task is condensed in Table I. Contingent upon the input blend, one of the 4 outputs is chosen and set to 1, while the others are set to 0. A reverse 2–4 decoder creates the reciprocal min-terms I0−3, in this way the chosen output is set to 0 and the rest are set to 1[4]. In regular CMOS design, NAND and NOR gates are preferred in the place of AND and OR, because we can implement those with 4 transistors, instead of 6, accordingly we can implement larger functions with higher productivity.

Table I Truth table of 2 to 4 Decoder

Input		Output			
A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

A 2–4 decoder can be implemented with 2 inverters and 4 NOR gates Fig. 2(a), whereas an inverting decoder requires 2 inverters and 4 NAND gates Fig. 2(b), both yielding 20 transistors.

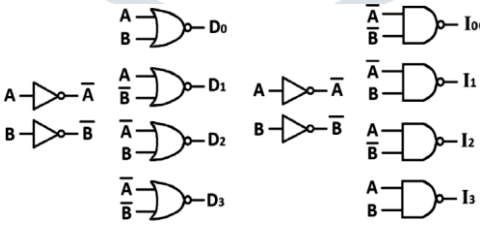


Fig.2 20-transistor 2–4 line decoders implemented with CMOS logic. (a) Non inverting NOR-based decoder. (b) Inverting NAND-based decoder.

Pass Transistor Logic:

In conventional logic families input is applied to gate terminal of transistor but in PTL it is applied to source/drain terminal. Here the width of PMOS is taken equal to NMOS so that both transistors can pass the signal simultaneously in parallel. Signal degradation occurs in pass transistor logic[6][7]. The main advantages of pass transistor are fewer devices to implement the logical functions as compared to CMOS

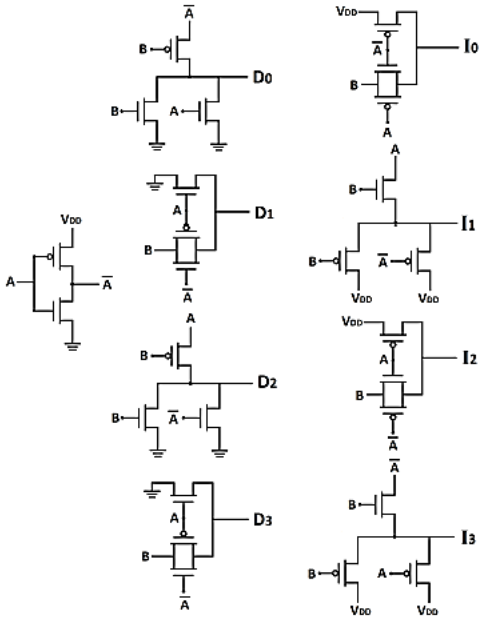


Fig.3 14-transistor 2-4 line decoders using PTL logic

GDI technology:

There are different low power strategies that are accessible these days where GDI is one of them. Nowadays a GDI is the most usually utilized strategy with the goal to decrease power as it lessens the switching of output. Additionally GDI method is utilized so as to reduce the quantity of transistors required for the structure which aides in decreasing the size of chip. The most fundamental cell in a GDI procedure is an inverter cell which is framed by the mix of a PMOS and a NMOS transistor[10]. Table II gives the operation details of basic GDI cell where for example if we want an AND gate operation terminal P is connected to ground and terminals G and N are the inputs of and gate. Similarly we can generate many operations based on different input combinations.

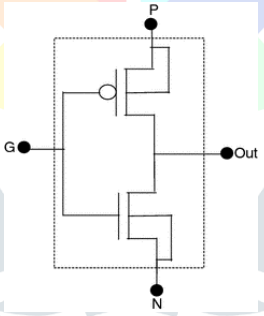


Fig.4 Basic GDI Cell

Table II Various Logic functions of GDI Cell

N	P	G	Output	Function
0	A	B	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	$A+B$	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{A}$	NOT

2-4 line decoder using GDI*:*

GDI uses 4 AND gates and 2 Inverters and it requires a total of 12 transistors to design the 2-4 Decoder. Depending on the input combination one of output is selected and set as 1 and others are 0 thereby reducing the transistor count in GDI when compared to CMOS. The 2-4 inverting decoder uses 4 OR gates and 2 Inverters and it requires a total of 12 transistors. Reduced transistor count results in power dissipation.

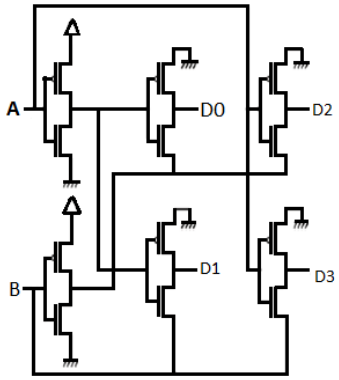


Fig.5 12T 2-4 Decoder using GDI

III. PROPOSED WORK

Complementary Pass Transistor Logic:

Complementary pass-transistor logic consists of complementary inputs/outputs, a NMOS pass-transistor network, and CMOS output inverters. The circuit function is implemented as a tree consisting of pull-down and pull up branches. Since the threshold voltage drop of NMOS transistor degrades the "high" level of pass-transistor output nodes, the output signals are restored by CMOS inverters. CPL has traditionally been applied to the arithmetic building blocks and result in high-speed operation due to its low input capacitance and reduced transistor count[6][8].

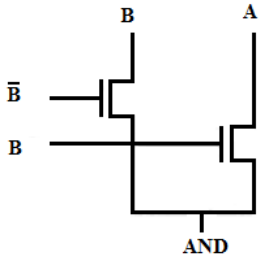


Fig.6 Circuit for two input AND function in CPL

The advantage of high functionally with few pass transistors and of small input capacitances in the CPL styleand less wiring overhead makes its better choice[7][9]. CMOS is good in reliability, but on the other side CPL has the benefits of hardware reduction having lesser number of transistors. Thus CPL reduces the circuit delay and less number of components reduces the area and power consumption of the circuit.

2-4 Line decoder using CPL logic

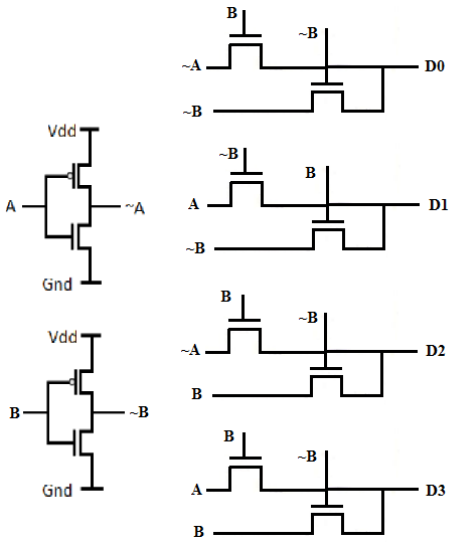


Fig.7 2-4 line decoder using CPL

APPLICATION

Static Random Access Memories (SRAM):

Memory is the process in which information is encoded, stored, and retrieved. Encoding allows information from the outside world to be sensed in the form of chemical and physical stimuli. In this first stage the information must bechanged so that it may be put into the encoding process. Storage is the second memory stage or process[8]. This entails that information is maintained over periods of time. Finally the third process is the retrieval of information that has been stored.

CPL logic for 2 to 4 decoder is implemented in 4*4 SRAM memories. Clock signal is being connected to all PMOS circuits. Only during the negative edge of the clock pulse PMOS will be active. As a result of which the power is minimized. The proposed CPL for 2*4 decoder implemented in 4*4 SRAM memories is shown in the figure below

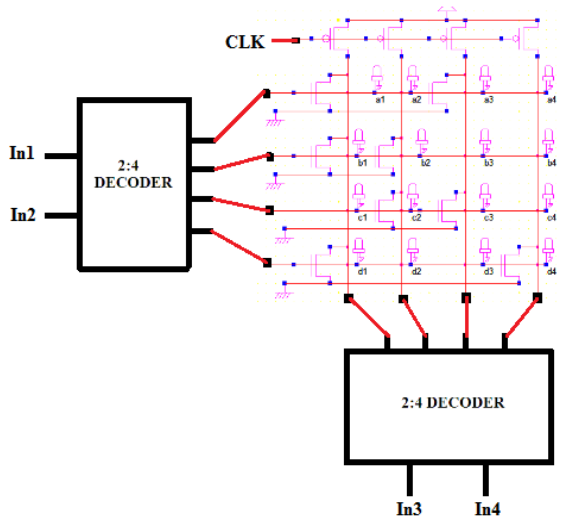


Fig.8 4*4 SRAM using 2-4 Line Decoder

Table III Comparison of existing and proposed SRAM Design

Parameters	Existing	Proposed
Power	5.498mW	0.706mW
Area	874um^2	672um^2

IV. EXPERIMENTAL RESULTS

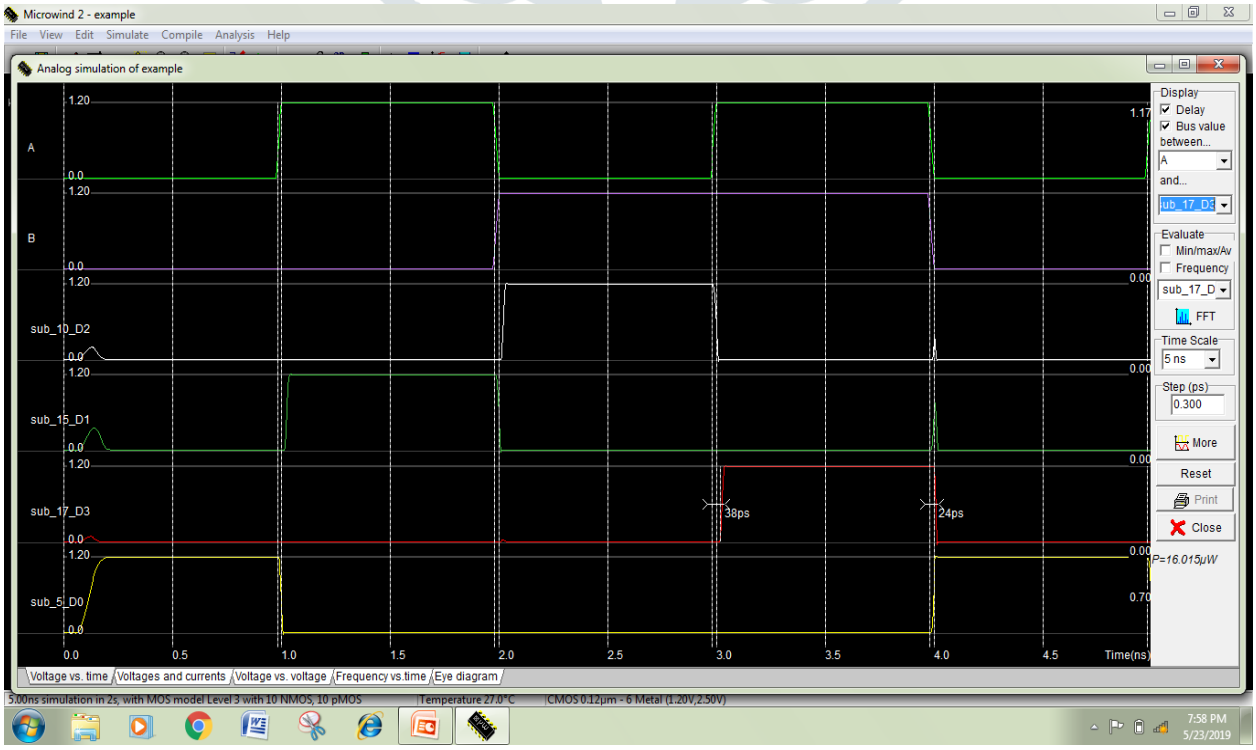


Fig.9 Simulation output of 2-4 decoder using CMOS

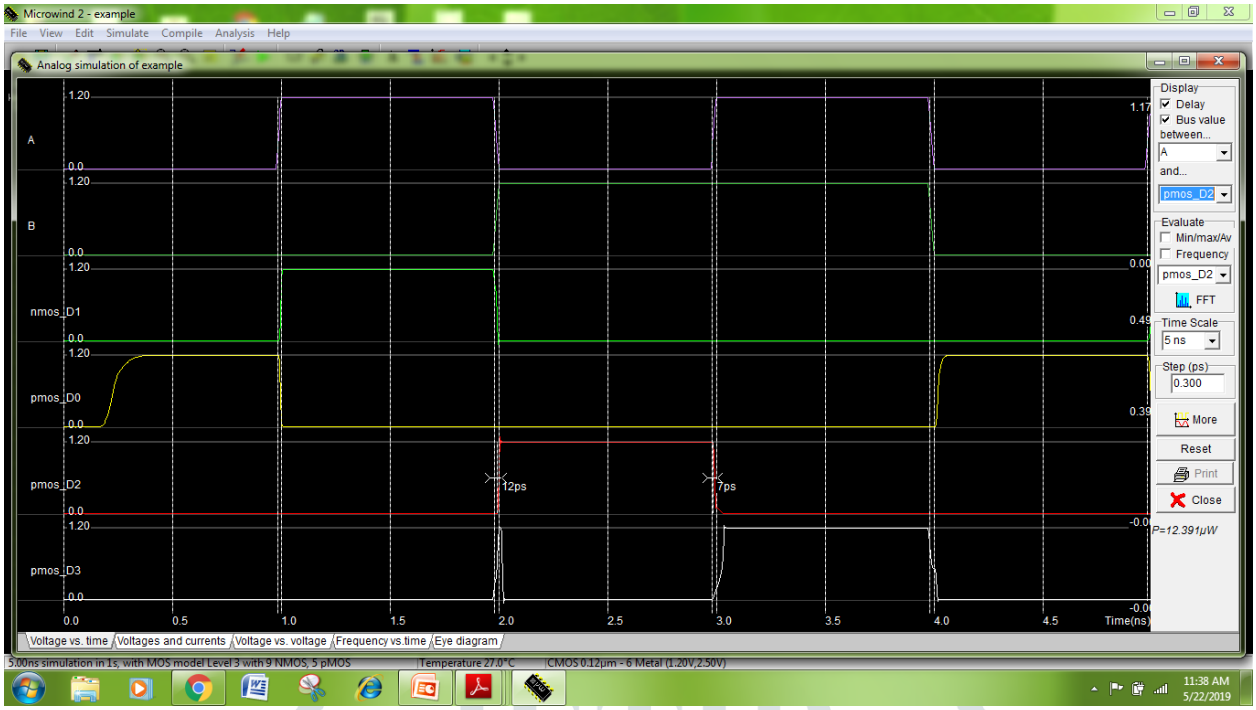


Fig.10 Simulation output of 2-4 decoder using PTL

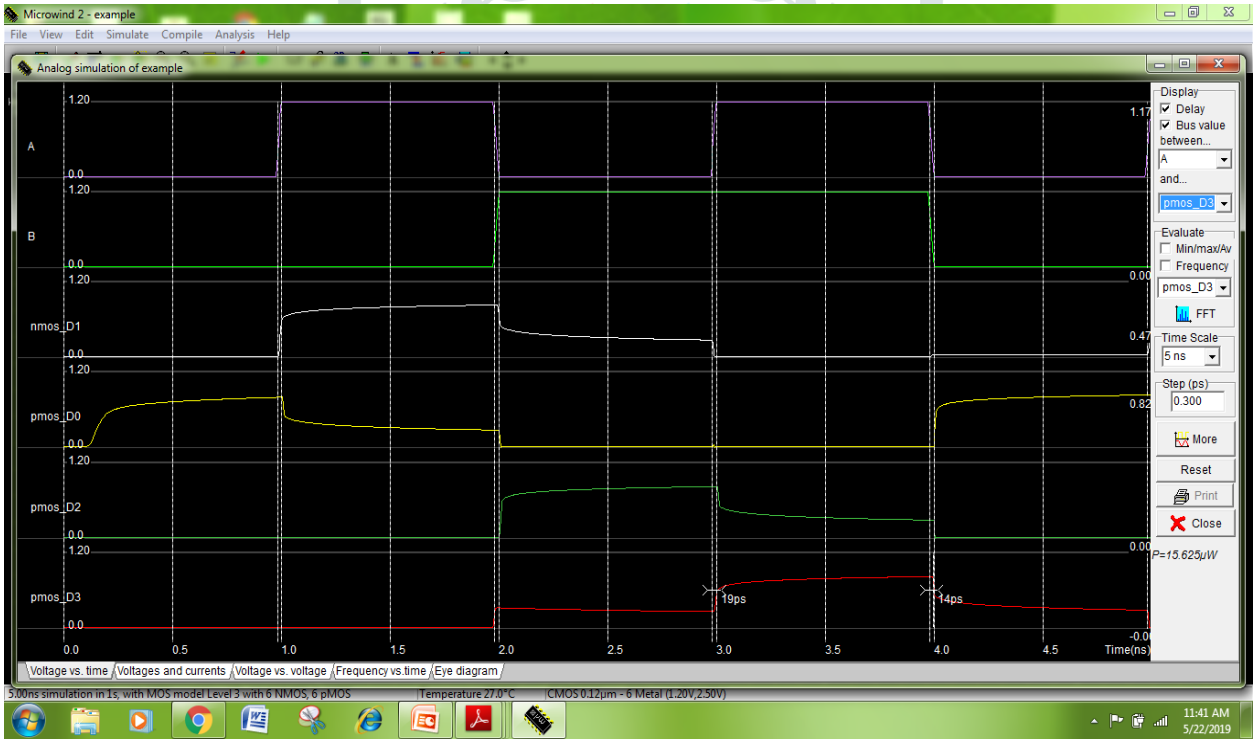


Fig.11 Simulation output of 2-4 decoder using GDI

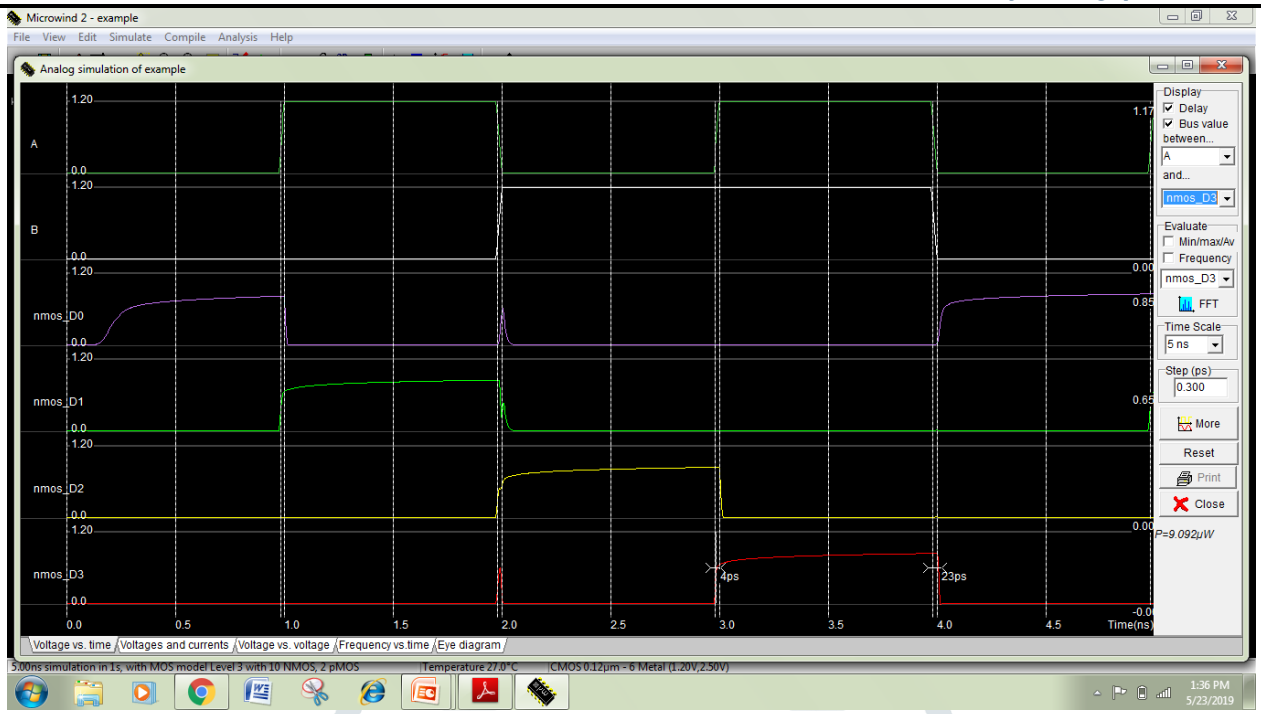
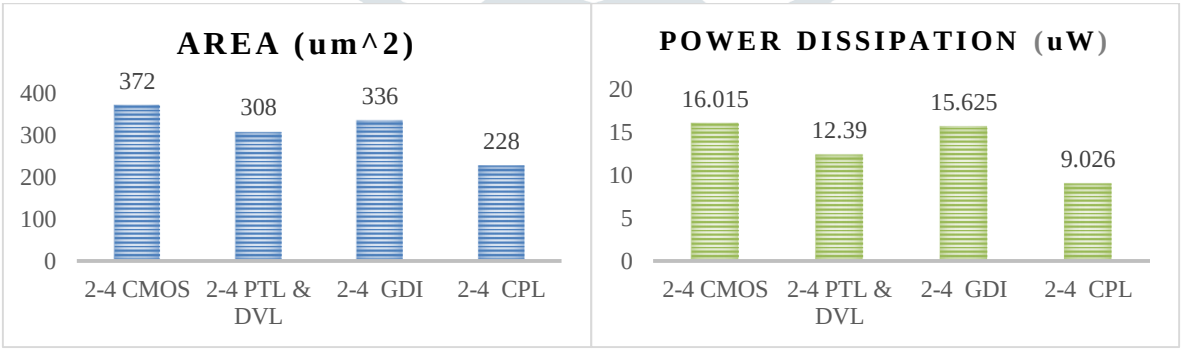


Fig.12 Simulation output of 2-4 decoder using CPL

Table IV Comparison between different decoder designs

Decoder Type	Transistor count	Area (um^2)	Power Dissipation(uW)
2-4 CMOS	28	372	16.015
2-4 PTL & DVL	14	308	12.39
2-4 GDI	12	336	15.625
2-4 CPL	12	228	9.026

The Proposed 2-4 decoder with complementary pass transistor logic is have better area and power dissipation when compared to other transistor logics.



V. CONCLUSION

New logic CMOS families utilizing Pass Transistors Circuit strategies have been proposed with the target of improving speed of operation and power utilization. In this paper, CPL for 2-4 decoder has been created and placed in SRAM memories which limits the quantity of transistor and then preserves the speed of the design and furthermore accomplishes the power utilization.

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