IMPLEMENTATION OF LOW POWER MEMORY CELLS

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Abstract: - The fast development of versatile battery worked gadgets has made low power IC design. The SRAM units have turned into a vital part in current SOCs. For SRAM power, stability, delay and area are the real concerns. What's more, they are exchange offs to one another. In any case, all are critical and should be in worthy range. CMOS SRAM cell is less power devouring and have less perused and compose time. Higher cell proportions can diminish the read and compose time and enhance security. PMOS transistor with less width diminishes the power utilization. Traditional SRAM cell plans are control eager and poor entertainers in this new time of quick portable processing. In this paper, low power SRAM cell plans have been broke down for power utilization, compose delay and compose control defer item. These plans are contrasted and the ordinary 6T SRAM, 7T SRAM, 9T SRAM cells. In this paper we mostly focused on power and security and we planned an upgraded proposed 10T-SRAM cell for low power utilization.

Index Terms- 10T SRAM, 9T SRAM, 7T SRAM, 6T SRAM.

I. INTRODUCTION

Least component measure scaling driven by Moore's law prompted to improve the check of transistors the usefulness of a chip. Numerous new applications seemed, for example, remote sensors, PDAs, and tablet gadgets. In these gadgets, draw out the battery life is the principal configuration issue. SRAM clusters possess over 90% of the bite the dust zone in present-day SOCs as per ITRS forecasts [1], so its capacity rules the general power utilization. Supply voltage scaling is one of the compelling approaches to decrease control utilization of advanced circuits and this technique is intriguing for SRAM creators as there is an extensive number of written works that center around close or sub-edge SRAM cell structure. In the late pattern of planning rapid, low power gadgets so as to propel innovation numerous procedures have surfaced to make an appropriate harmony between region speed and power. As the years advance the extent of the chips are getting decreased and furthermore the circuit complexity [1] is getting high. The use of advanced memory's expanding definitely and then there is no computerized framework without memory [1]. For instance to store program guidelines, beginning qualities, transitional information results and so on. The use of battery worked gadgets and versatile hardware gadgets are likewise expanded definitely. So as to expand the battery life of gadgets we should focus on power utilization and power dissemination of the gadget [2]. The memory present in the gadget likewise adds to the power utilization or dispersal of it, primarily SRAM (Static irregular access memory) which is utilized as reserve memory. For SRAM we need to give consistent power supply to each SRAM cell so as to hold the information in it. As a result of this, the power scattering in SRAM is exceptionally extensive. To lessen the power dissemination the supply voltage is downsized as it were. Alongside supply voltage, edge voltage likewise diminished to expand the operation. Along with the static power dissemination, the steadiness of the SRAM cell diminishes with the scaling of the supply voltage. So an ordinary 6T can't give dependable outcomes at voltages as low as of limit voltage [3]. Along these lines, there is a requirement for structuring a strong SRAM cell which works at such low voltages and scatters less static power. To accomplish this we plan an SRAM cell with various structures.

II. 7T SRAM CELL

The proposed 7T SRAM cell appeared in Fig. 1. This cell has a single finished read and composes activities. Peruse get to a transistor and a read bit line of this cell is marked by M6 and BLT, separately. Free read and compose ways in this cell enables us to pick a base estimated transistor for the read access and a bigger access transistor for the compose activity. By utilizing this technique, the contention of access transistors is loose. To upgrade read dependability and compose capacity, two distinct systems are considered. M7 goes about as the confinement transistor that secludes the left storage node (q) from the voltage improvement on the correct storage node (QB) amid the read activity. Truth be told, by declaring the entryway of this transistor to ground in the read task, the left storage node (q) will be secluded from the voltage upgrade on the correct storage node (QB) when BLT releases through M2 and M6. This disconnection upgrades the reading strength of the cell. In the hold state, M7 is on to keep the information in solid positive input. Subsequently, the hold condition of this cell is like that of the customary 6T cell [4].

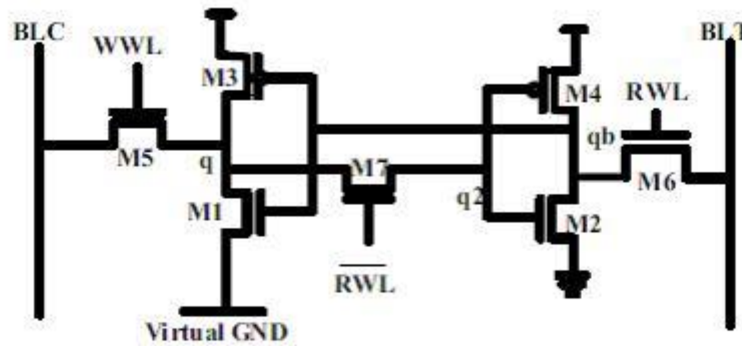

Figure 1: 7T SRAM cell Schematic

In comparison with the conventional 6T cell, the write/compose task of the proposed cell has two noteworthy contrasts. The first is that it is single-finished. Allude to Fig. 1, M5 goes about as the compose get to a transistor which can be measured extensive to upgrade the compose capacity without crumbling of the read stability [5]. The second contrast of the compose task of this cell and the regular 6T is that this cell utilizes a virtual ground to debilitate one of the consecutive inverters and diminish the quality of the positive criticism. Thusly, composing information on this cell is done effectively. To anticipate utilizing additional voltage rails in the SRAM square, we utilize the circuit proposed in [7] to make two unique voltages as indicated by the cell activity. In the read and hold expresses, the virtual ground hub is associated with the ground to save the put-away information utilizing a solid criticism, so the hold condition of this cell is like the conventional 6T cell. While in the compose task, the virtual ground hub is associated with the wellspring of a PMOS transistor (which is poor at pulling a node to ground), so the voltage of this hub increments and the compose activity is done effectively.

III.9T- SRAM CELL

In our 9T SRAM cell there is a diode associated NMOS (N5) as appeared in figure 2.This NMOS scales the VDD which lessens the dynamic power to incredible degree as [6]

$$P = \alpha FCV_{DD}^2 \ldots .(1)$$

Where, α = switching factor, F = frequency, C = capacitance, VDD = supply voltage.

The stability of cell is diminished because of scaling of VDD in light of the fact that there is likelihood of flipping the substance of capacity hubs as a result of pre-charged piece lines while read activity (chiefly when cell working at low supply voltages). The security diminished because of scaling of VDD is remunerated by the additional PMOS transistors P3 and P4 which are dependably ON are included among driver and access transistors. This structure builds the read soundness [4]. For instance while perusing '1' QN is at '1' and QNB hub is at '0'. At the point when WL is empowered the voltage isolated in arrangement along N4 get to transistor, P4 leading PMOS and N2 driver transistor stifle ascending of QNB voltage to VDD-VTN4-|VTP4|, Where VTN4 and VTP4 are limit voltages of N4 and P4respectively. So this smothered voltage can't flip the substance of cell. While composing the information if hub QN is at '1' and QNB is at '0' to compose '0' at hub QN, BL is associated with ground and BLB is raised to VDD and WL is empowered. The hub Q changes from VDD to '0' and hub QNB is released from '1'to '0' state. The hub QN can't be dipped under |VTP3|.because PMOS isn't ideal passer of '0'. In any case, falling of QN causes P2-N2 inverter to trigger and cross coupled inverters bring flip of state. The static power scattering is additionally diminished due to stacking of MOSFETS (PMOS, PMOS NMOS)[7].

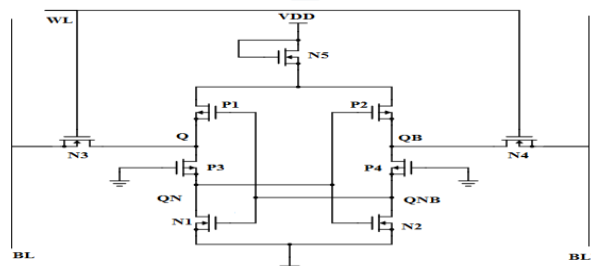

Figure 2: 9T -SRAM Cell

IV. 6T-SRAM CELL

A six-transistor SRAM cell (6T SRAM cell) is ordinarily utilized as the memory cell. however, the 6T- SRAM cell delivers a cell of bigger size than that of a DRAM cell, bringing about a low memory thickness. In this manner, regular SRAM cells that utilization the 6T RAM cell experience issues in fulfilling the developing need of a bigger memory limit in portable applications. Likewise the traditional six transistor (6T) SRAM cell demonstrates poor solidness at little component measure with low power supply[8].During the read activity, the strength radically diminishes because of the voltage division between the entrance and driver transistors. Impressive research work has been done in the course of recent years to structure a low power SRAM cell, which additionally brought about a critical debasement in SRAM cell information security. With every innovation age, the scaling

of CMOS gadgets results in arbitrary varieties in the quantity of dopant molecules in the channel area of the gadget. This causes irregular varieties in the gadget parameters like the threshold voltage Vt and is normally known as random dopant fluctuation (RDF) .Since SRAM cells work on carefully adjusted Transistors, and the customary six transistor (6T) SRAM cell demonstrates poor strength amid read activity, it is imperative to consider these issues amid new memory cell plans. Configuration proposed in different papers furnishes topologies for cells with higher read strength at the expense of expanded zone because of higher transistor tallies. Likewise segregated read bit-lines (separate from the compose bit lines) increment dynamic power utilization and unpredictability while structuring the general memory unit [9].

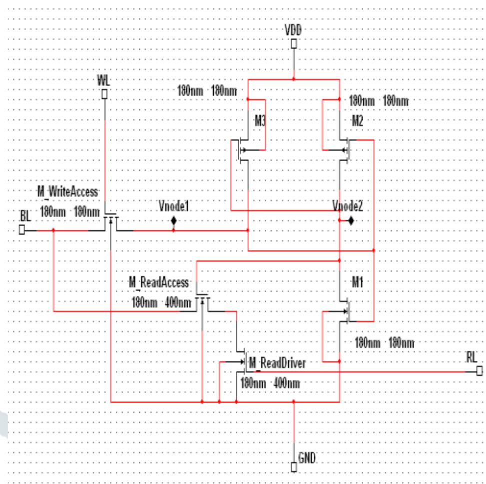

Figure 3:6T-SRAM CELL

V. 10T-SRAM CELL

In detail, based on the physical mechanism with reasonable transistor size, a robust 10T SRAM CELL is first proposed to enhance the reliability level in aerospace radiation environment while keeping the main advantages of low power consumptions. The 10-T SRAM CELL has enhanced read speed along with good read and write stability. Though the read-write power of the proposed cell is higher with respect to the existing 10-T cells, it consumes a lower power as compared to the convention 6-T SRAM CELL. The proposed 10-T SRAM CELL can be used where the speed and robustness are the primary requirements. It is apparent that at both operating frequencies. The proposed 10-T SRAM CELL designs have significantly less read power consumptions.

For the proposed 10T SRAM cell figure(4) describe its basic schematic structure from the fig it can be seen that the proposed 10T SRAM cell consists of 10 transistors in that PMOS and NMOS transistors from M1 TO M11 but in that M7 is absent .Both NMOS transistors M8 and M10 are defined as access transistor and they are connected with word line (WL).When the WL is low(WL=0) read/write operations are not performed. When the WL is high (WL=1) read /write operations are performed and then M8 and M10 are in ON condition. The stored nodes are Q, Qn. In that two nodes are responsible for keeping the stored value correctly. To transmit the digital signal to output port. While read operation is performed a digital sense amplifier has been used and they are connected to two bit lines BL and bln.

Assuming that the stored value of the proposed 10-T SRAM cell is 1 in digital logic, i.e., Q = 1, QN = 0 as shown in Fig. 5. It is easily concluded that the proposed SRAM 10Tmemorycell is steadily maintaining the stored value when WL is driven by a low voltage (WL=0). Before normal read operation, due to precharge circuitry, the voltages of the bit lines BL and bln will be raised to 1 in digital logic. In a read operation, WL is in high mode (WL = 1), and then two access transistors M8 and M10 are turned ON immediately. Nodes Q, QN, are keeping the stored value, and the voltage of bit line BL is also unchanged. However, the voltage of bit line BLN is decreased due to the discharge operation through ON transistors M11 and M10. Once the voltage difference of bit lines is a constant value that has been confirmed the differential sense electronic equipment and connecting with two- bit lines, the stored digital signal in the memory cell will be output as soon as possible. The purpose of a write operation is to alter the hold on the logical worth properly. Therefore, before the write operation, the write electronic equipment, write the voltages of bit line BL are going to zero BL in digital logic. Contrary to the voltage of bit line BL, the voltage of bit line bln will be 1. When the voltage of WL is supply voltage VDD (WL = 1), write operation is executed. Transistors M9, M2, M6, and M1 are turned ON. At the moment, the states of transistors M11, M3, M5, and M4 will be OFF, so that the logical value of this memory cell is rightly changed to 0. Therefore, write operations can also be completed successfully.

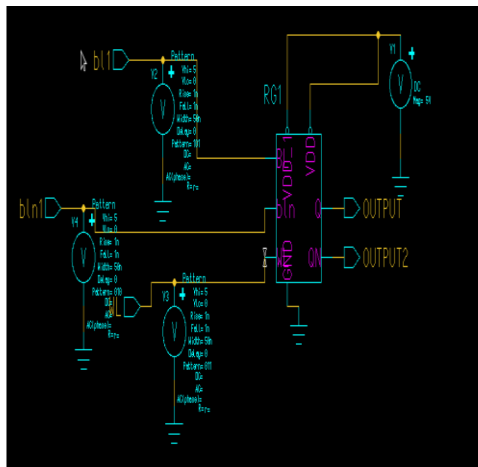

Figure 4:10T-SRAM CELL block diagram

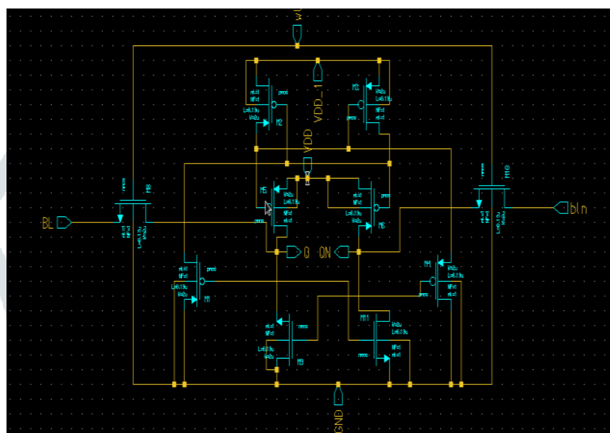

Figure 5:10T-SRAM CELL schematic diagram

VI. RESULTS & DISCUSSION

7T-SRAM CELL:

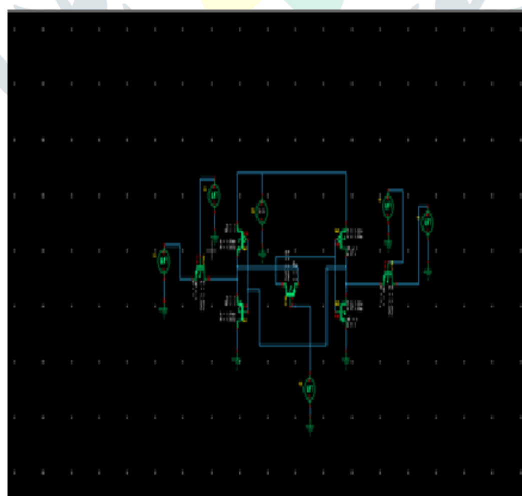

Figure 6: Schematic of 7T SRAM Cell

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VV5 from time 1e-009 to 1e-006
Average power consumed -> 4.356290e-004 watts
Max power 4.419557e-003 at time 1.05e-008
Min power 4.354369e-003 at time 1e-007


Parsing                       0.10 seconds
Setup                         0.03 seconds
DC operating point            0.01 seconds
Transient Analysis            0.54 seconds
Overhead                      0.64 seconds
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Total                         1.31 seconds

Simulation completed
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Figure 7: Power Consumption of 7T SRAM Cell

9T SRAM CELL:

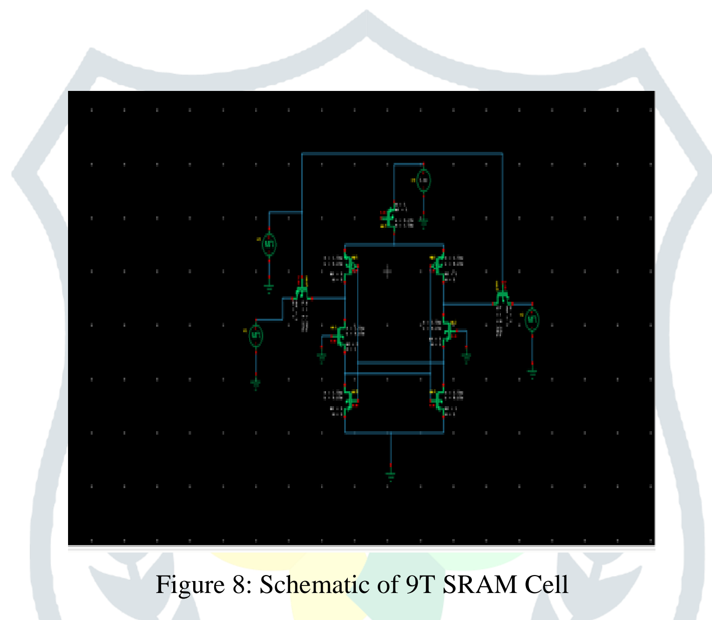

Figure 8: Schematic of 9T SRAM Cell

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Power Results

VV4 from time 1e-009 to 1e-006
Average power consumed -> 1.490347e-010 watts
Max power 1.510652e-009 at time 5e-009
Min power 1.491139e-009 at time 1e-007


Parsing                       0.09 seconds
Setup                         0.03 seconds
DC operating point            0.03 seconds
Transient Analysis            0.52 seconds
Overhead                      0.44 seconds
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Total                         1.11 seconds
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Figure 9: Power Consumption of 9T SRAM Cell

6T SRAM CELL:

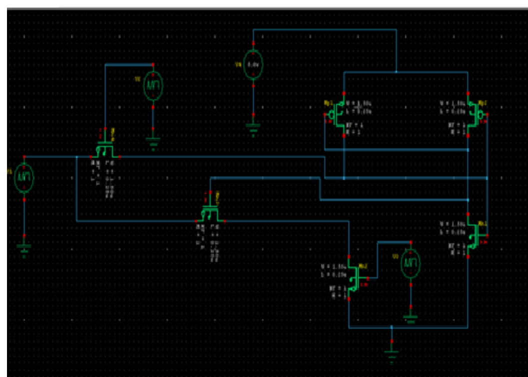

Figure 10: Schematic of 6T SRAM Cell

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Power Results

VV4 from time 1e-009 to 1e-006
Average power consumed -> 8.071395e-011 watts
Max power 1.143830e-009 at time 5.1e-008
Min power 2.507794e-010 at time 4.05e-008


Parsing                          0.11 seconds
Setup                            0.03 seconds
DC operating point               0.00 seconds
Transient Analysis               0.56 seconds
Overhead                         0.84 seconds
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Total                            1.54 seconds

Simulation completed
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Figure 11: Power Consumption of 6T SRAM Cell

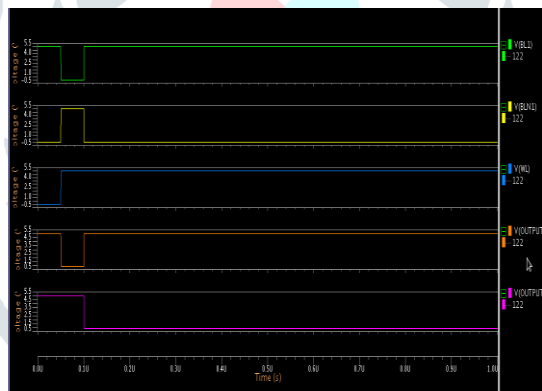

Figure 12:10T-SRAM cell wave forms

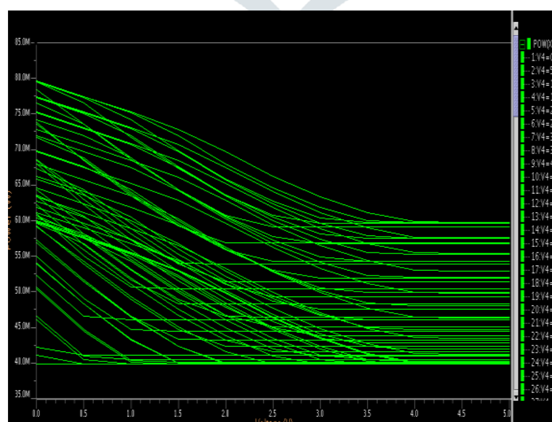

Figure 13: Power consumption of 10T-SRAM cell

CONCLUSION

A novel 10T SRAM CELL is proposed. In this brief compared with previously hardened 9T, 7T, 6T memory cells. The proposed cell can recover an error in any one sensitive mode. The simulation results present that the introduced for the proposed 10T CELL is the decreased time access. However, when the considering the constraints of the target applications, compared with

another hardened memory cell, the proposed 10T static cell can be regarded as a good choice for aerospace application as it provides a good balance among performances and low power consumption and reliability for memories working at radiation environment.

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