An Efficient Design and Analysis of Combinational Circuits Using Reversible Decoder

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Abstract : Digital system implemented by using conventional gates like AND and OR gates dissipates a major amount of energy in the form of bits which gets erased during logical operations. This problem of energy loss can be solving by using reversible logic circuits in place of conventional circuits. This problem of energy loss can be solving by using reversible logic circuits in place of conventional circuits. Reversible logic is widely being considered as the potential logic design style for implementation in modern nanotechnology and quantum computing. Reversibility has become the most promising technology in digital circuits designing. In this paper proposed comparator, decoder and multiplier design methodologies for the reversible realization of reversible 16 bit adder where the designs are based on the Peres gate. The proposed design is implemented on SPARTEN3 FPGA board and is synthesized using Xilinx ISE software.

IndexTerms **- AND, OR, SPARTEN3, FPGA, Xilinx, Reversible, Decoder.**

I. INTRODUCTION

Over the years, growth in the complexity of VLSI design has enable designer to include well over a million transistors on each chip. Designers are faced with the daunting task of packing more functionality into a smaller area and creating a circuit that operates faster than the previous generation. Design Automation (DA) technique play an invaluable role in this complex process. Reversible logic is a very prospective approach of logic synthesis for power reduction in future computing technologies. In a reversible circuit, the number of inputs and outputs are same and there is a one-to-one mapping between input values and output values. Reversible circuits are constructed using reversible gates. Reversible logic plays an extensively important role in low power computing as it recovers from bit loss through unique mapping between input and output vectors. No bit loss property of reversible circuitry results less power dissipation than the conventional one. Moreover, it is viewed as a special case of quantum circuit as quantum evolution must be reversible. Over the last two decades, reversible circuitry gained remarkable interests in the field of DNA-technology, nano-technology, optical computing, program debugging and testing, quantum dot cellular automata, and discrete event simulation and in the development of highly efficient algorithms.

Quantum Cost of the circuit is design by knowing the number of simple reversible gates (gates of which rate is previously identified) required to realize the circuit. The output of the reversible gate that's not used as a main output or as input to other gates is referred as the garbage output. In very little the unexploited output of a reversible gate (or circuit) is that the garbage output (s). These garbage outputs are required within the circuit to retain the reversibility concept.

II. LITERATURE SURVEY

Gopi Chand Naguboina et al.[1]These circuits are designed for minimum quantum cost and minimum garbage outputs. The method proposed for designing the decoder circuit can be generalized. For example, a 3×8 decoder can be designed using a 2×4 decoder followed by 4 fredkin gates, Similarly a 4×16 decoder can be designed using 3×8 decoder followed by 8 fredkin gates .The concept of duplicating the single output to required number of outputs is utilized to overcome the fan-out limitation in reversible logic circuits. This method of designing combinational circuits helps to implement many digital circuits with better performance for minimum quantum cost.

Ritajit Majumdar et al.[2] The number of garbage outputs also increases in the same way since every Fredkin gate has one garbage output for this design. The generalized design cannot be optimized any further by using the basic gates like Peres, TR or Toffli. However, further research interest may be to propose new gates that can be used to replace Fredkin gates in higher dimensional decoders, resulting in decrease of quantum cost.

Jadav Chandra Das et al.[3]The dissipated power shows that QCA is suitable alternative platform to CMOS, for implementing reversible circuits. Truth table based comparison of simulation results established the design accuracy. All the layouts are faster and higher in device density. The proposed circuits can be used to design reversible architecture for nano communication systems.

Payal Garg et al.[4] A Novel Design of Compact Reversible SG Gate and its Applications", In this paper author proposed a new 4*4 reversible gate, which is based on one to one mapping provided by the given encoding and decoding schemes. Since the proposed gate can implement universal gates so it can be used for designing large reversible systems. In a nutshell, the advent of reversible logic will significantly contribute in designing compact circiuits. Thus, the paper provides the initial threshold to make more complex and advance systems which can execute more difficult and complicated operations.

Rangaraju H G et al.[5] The architecture III implementation of Reversible eight-bit Parallel Binary Adder/Subtractor has much better performance as compared to architecture I, architecture II and existing design in terms of variety of gates used, Garbage inputs or outputs and Quantum Cost, thus can be used for low power applications. The full Adder or Subtractor is implemented in a single unit in our architecture as compared to only full Subtractor in the existing architecture. In future, the design can be drawn out to any number of bits for Parallel Binary Adder or Subtractor unit and also for low power Reversible ALUs, Multipliers and Dividers.

Manjinder Pal Singh et al.[6] "Performance Analysis of Low Power Decoders Using Reversible Computing", In this author presented reversible decoders using BVF, F2G and FRG gates. Table 3 demonstrates that the proposed reversible decoders in terms of hardware complexity and quantum cost. Our proposed reversible decoders with active low and active high mode using tracer circuit to avoid fan out, and can be applied to the design of complex systems in nanotechnology.

Md. Shamsujjoha et al.[7] "A Low Power Fault Tolerant Reversible Decoder Using MOS Transistor", In this author presented the design methodologies of an n-to-2n reversible fault tolerant decoder, where n is the number of data bits. In proposed several lower bounds on the numbers of garbage outputs, constant inputs and quantum cost and proved that the proposed circuit has constructed with the optimum garbage outputs, constant inputs and quantum cost. In addition, author presented the designs of the individual gates of the decoder using MOS transistors in order to implement the circuit of the decoder with transistors correctly. The comparative results proved that the proposed designs perform better than its.

Mozammel H. A. Khan et al.[8] "Reversible Realization of Quaternary Decoder, Multiplexer, and Demultiplexer Circuits", Multiple-valued reversible circuits are a promising choice for future computing technology. Quaternary logic has the advantage that classical binary logic functions can be expressed as quaternary logic functions by grouping 2-bits along into quaternary digits. Quaternary encoded reversible realization of binary logic function will be half-times compressed than the reversible realization of original binary logic function in terms of the number of input/output lines needed.

III. PROPOSED DESIGNS AND SIMULATION

1. Comparator

In the 1-bit comparator circuits we have utilized the one Peres reversible gate and two CNOT reversible gate and one not gate. Figure 1 shows the proposed design for the reversible comparator. The quantum cost of the circuit comes out to be
QC = QC of Peres Gate + 2 X QC of CNOT gate +1 X QC of NOT Gate.
QC = 4 + 2 x 1 + 1=7

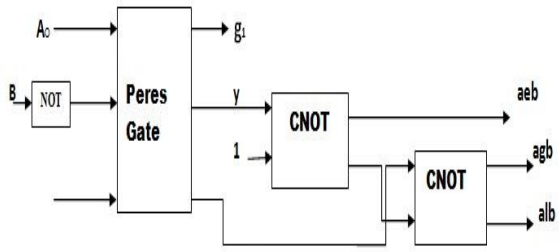

Figure 1: 1-bit reversible Comparator Circuit

Table 1: Truth table of the 1-bit reversible Comparator

INPUT		OUTPUT		
A	B	aeb	agb	alb
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	1

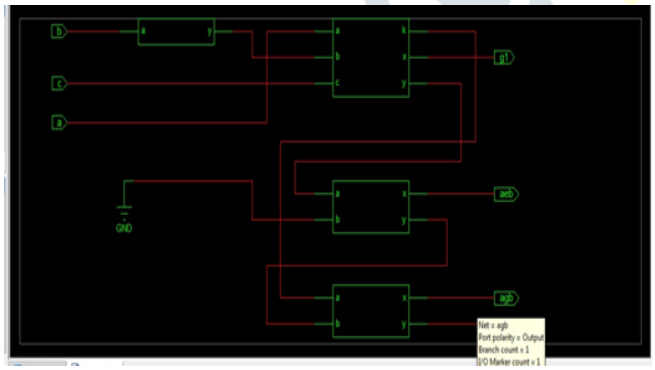

Figure 2: RTL Schematic of Reversible Binary Comparator

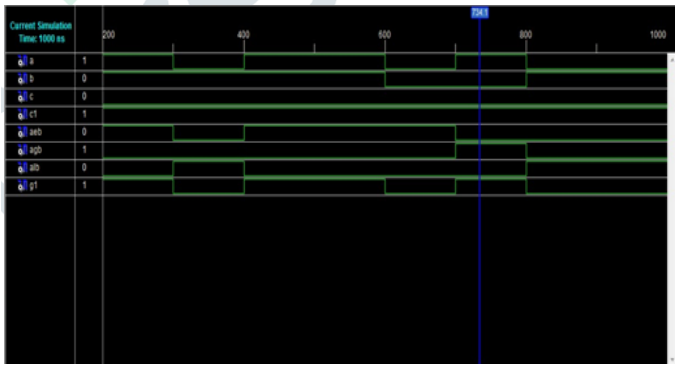

Figure 3: Test bench waveform for Binary Comparator

2. Decoder

3 X 8 Decoder : - Figure 4 shows the proposed 3 x 8 reversible decoder .The Quantum Cost of the Circuit can be calculated as
QC = QC of FG Gate + 6 X QC of MFG
QC => 1 + 6 x 4
QC => 25
As seen from the Figure 4 the Garbage output from the design comes out to be two B output from first 2 MFG and four C output from Last four MFG thus total garbage output comes out to be ,
Garbage Output = 6
The constant input used in the circuit are 7.

Table 2: Truth table of 3 X 8 Reversible Decoder

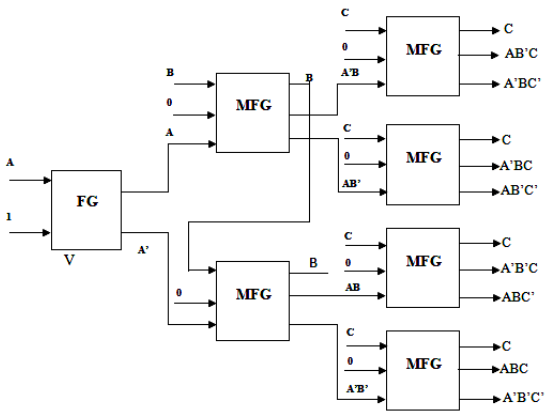

Figure 4: 3 X 8 Reversible Decoder

INPUT			OUTPUT							
A	B	C	p	q	r	s	t	x	y	z
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

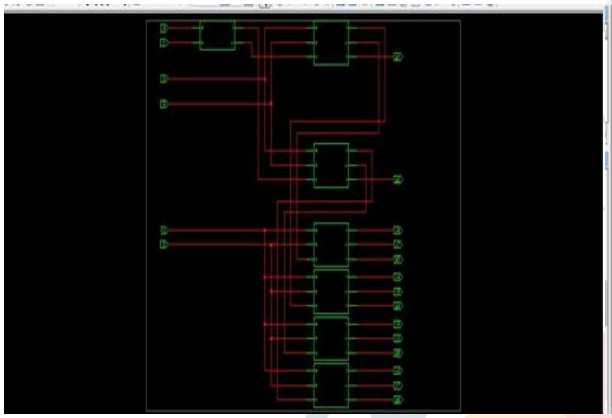

Figure 5: RTL Schematic of Reversible 3x8 decoder

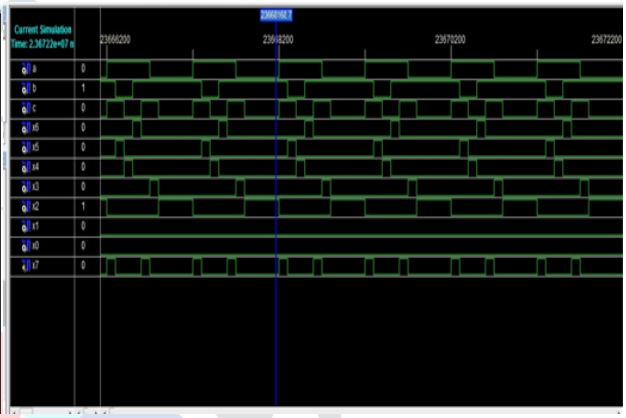

Figure 6: Simulation result of 3x8 decoder

3. Multiplexer

Our Proposed 8x1 Multiplexer is implemented using Fredkin Reversible Gate having Quantum Cost of 5. Figure 7 shows 8 X1 Reversibe Decoder

O1 = S0' A + S0 C
Thus for S0 = 0 => O1 = A
Similarly for S0 = 0 => O2 = C and O3 = E, O4 = G
For S1 = 0
O5 = A and O6 = E
Thus for S2 = 0
Z = A
Quantum Cost of the circuit comes out to be
QC = 7 X QC of Fredkin Gate
QC = 7 X 5
QC = 35

Table 3: Truth table of 8 X 1 Reversible Multiplexer

S_0	S_1	S_2	p
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

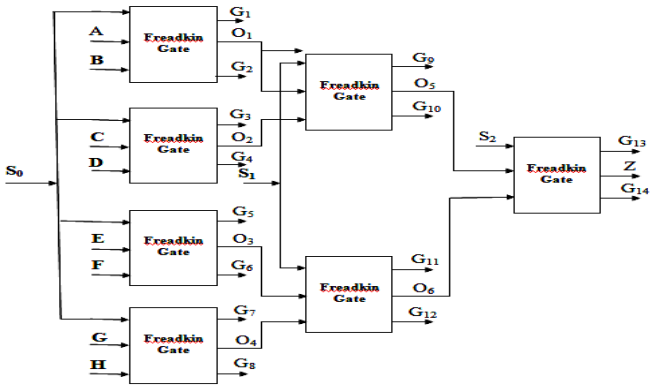

Figure 7: 8 x 1 Reversible Multiplexer Simulation

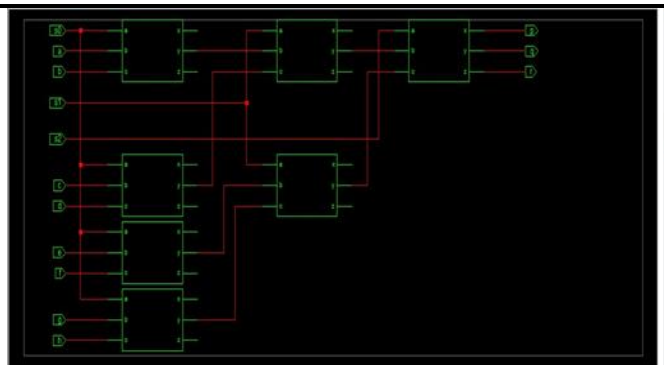

Figure 8: RTL Schematic of Reversible 8x1 Multiplexer

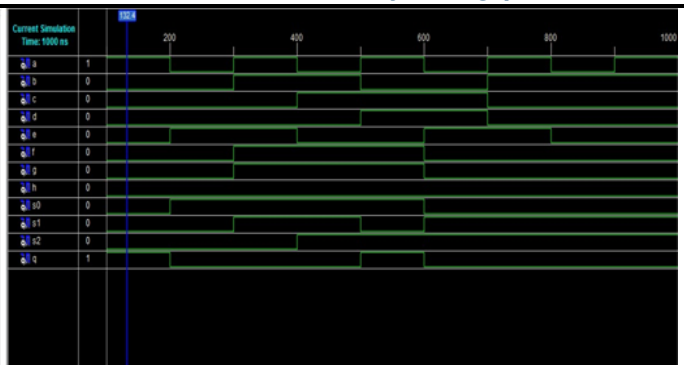

Figure 9: Simulation result of 8x1 Multiplexer

Above figures shows the RTL schematic along with simulation result of different reversible combinational circuits shown in the proposed methodology.

IV. RESULT AND COMPARISON

Proposed work is simulated using Xilinx software, outcome discussion is following-

Table 4: The combinational circuit designed using reversible gates are analyzed in terms of quantum cost and garbage outputs.

Circuit	Quantum cost of Previous Work	Garbage Outputs of Previous Work	Quantum cost Of Proposed Work	Garbage Outputs of Proposed Work
3 to 8 Decoder	31	4	25	2
4to16Decoder	71	5	57	3
Binary Comparator	16	5	7	2
8x1 multiplexer	75	39	35	14

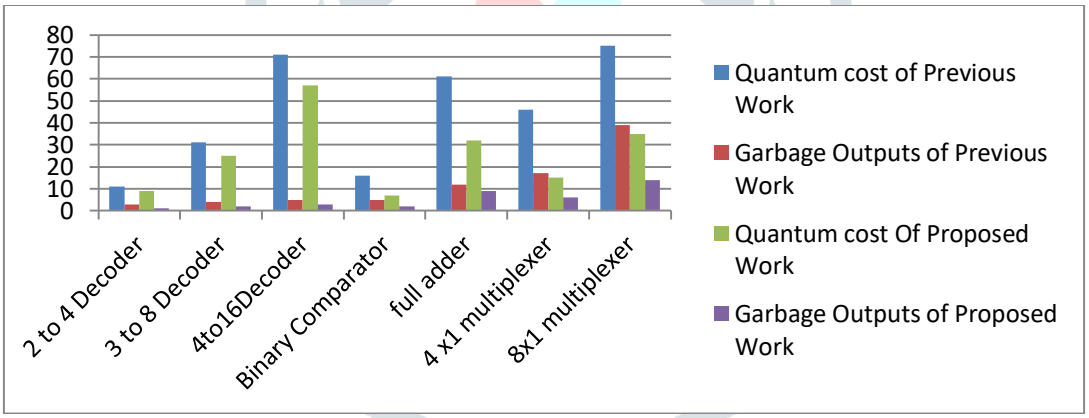

Figure 10: Analyzed in terms of quantum cost and garbage outputs.

Table 5: The combinational circuit designed using reversible gates are analyzed in terms of ancilla input

Circuit	Ancilla Input of Previous Work	Ancilla Input of Proposed Work
3 to 8 Decoder	31	25
4 to 16 Decoder	71	57
Binary Comparator	16	7
8x1	75	35

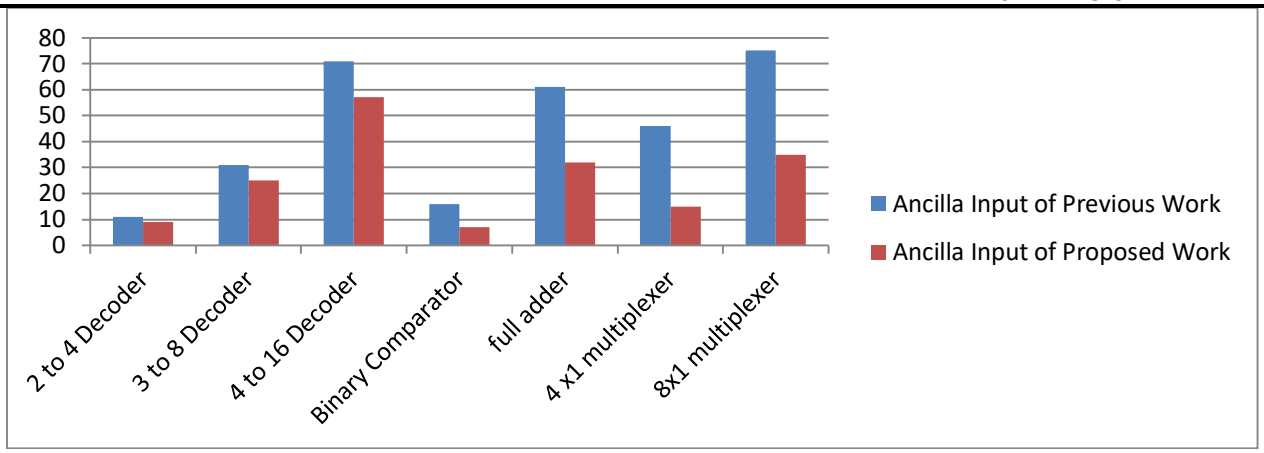

Figure 11: Analyzed in terms of Ancilla input.

Table 6: The combinational circuit designed using reversible gates are analyzed in terms of gate count

Circuit	Gate Count of Previous Work	Gate Count of Proposed Work
3 to 8 Decoder	31	25
4 to 16 Decoder	71	57
Binary Comparator	16	7
8x1 multiplexer	75	35

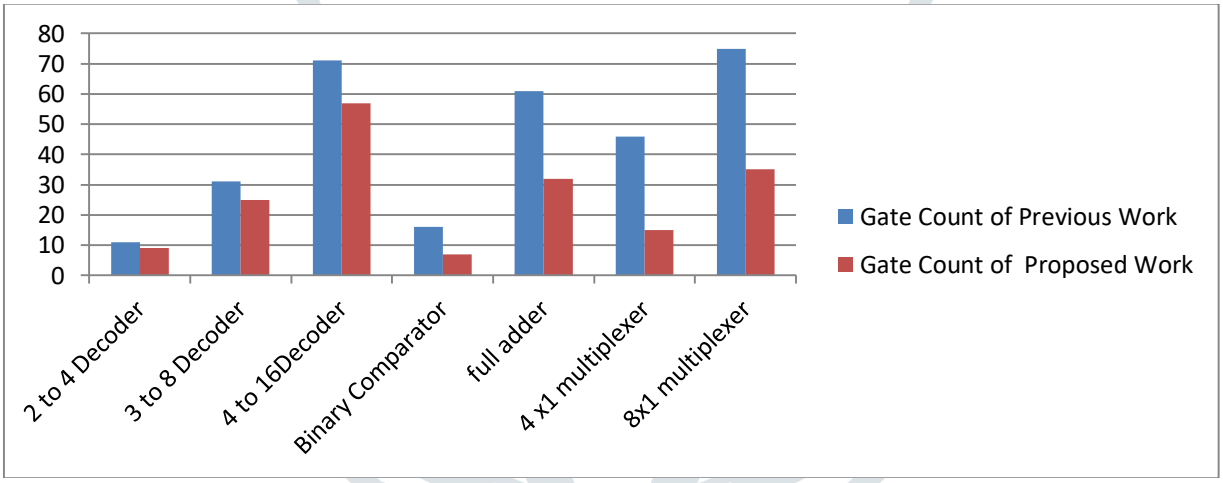

Figure 12: Analyzed in terms of Gate count

The quantum, cost, garbage output and Ancilla input are calculated in the proposed methodology. The blue line in the simulation results shows the output result at particular bit value which validate the simulation results.

V. CONCLUSION

The planned multiplier factors are higher than the present styles because of reducing the quantity of gates, garbage outputs, hardware complexity and variety of transistors needed. The facility dissipation of reversible logic style over irreversible logic style is low. Our planned reversible multiplier factor circuit is applied to the planning of complicated systems in nanotechnology. The planned Wallace reversible multiplier circuit is better than the present designs in terms of hardware complexness, variety of gates, garbage outputs and constant inputs. The implementation of proposed reversible logic multiplier circuit using 8X8 wallace tree Techniques which has two main features: One is implementing the multiplier using reversible logic increases the speed of the multiplication and second is the use of 8X8 wallace tree Techniques reduces the area and the hence the power dissipation. The proposed design is hardware efficient as compared to other traditional methods as well as architectures that is built using partial products, full adder and compressors. The design is implemented on Xilinx XC3S100E-5VQ100, Spartan3E device family.

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