Analysis on integration impacts of Distributed generation on distribution system

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Abstract : ***The generation of power from the convention methods to meet the load demand will experiences lot of disturbance and also it is difficult to meet the load growth. There is a requirement to supply the power at appropriate voltage. Distributed generation (DG) is the solution for these issues. The DG includes both positive and negative impacts on the interconnected system. The impact of DG integration is the point to be considered for the analysis as the total system operation will be depending on the optimal allocation. In this paper DGs are integrated at different nodes of the test system considered based on the possible disturbance of integration. The DG with selected penetration is integrated at sensitive node, Low voltage bus, Tail end node, bus with maximum load and node near to source to analyze the integration impact of DG on the test system. The considered test system is analyzed by analyzing the voltage profiles and power losses at each considered method. IEEE bus system is used for the analysis.***

Index Terms – Distributed generation (DG), impact of DG, Sensitive nodes, Tail end nodes, Voltage profiles.

I. INTRODUCTION

The term "distributed generation" (DG) refers to the production of electricity near the load center at the distribution level. The distributed generation resources are renewable energies and cogeneration (simultaneous production of heat and electricity). Distributed Energy Resources (DER) had changed many features of distribution system operation, design and Execution. With increase in number of decentralized systems with smaller generating units connecting directly to the distribution networks near load center, the distribution companies reduce loss in their networks.

The position and capacity of the DG must be optimized to increase the benefits and minimize their negative impacts on the power system [6]. The technical parameters are voltage profile, system protection, reactive power, power loss, power quality, power control and conditioning, reliability and stability.

Improper placement of DG will leads to the increment in system losses which includes both active and reactive power losses, operating cost and network capital cost. it also lead to injection of harmonics, possibility of reverse power flow, risking the safety issues and complex controlling scheme . In view of these, proper allocation of distributed generation could enhance the network potential in terms of better voltage profile and lower the system power losses, while improving the quality of power supply.

With the above considerations the optimal allocation and sizing of DG is necessary to improve the overall efficiency of the system by reducing the losses and improving voltage profiles and performance of the power system.

II. PROBLEM FORMULATION

A.Power loss calculation

The equation of the real power losses in the system can be given in terms of exact loss formula as state below, The power loss is given by

$$P_L = \sum_{i=1,j=1}^{n} [\alpha_{ij}(P_iP_j + Q_iQ_j) + \beta_{ij}(Q_iP_j - P_iQ_j)] \quad \ldots\ldots\ldots 2.1$$

Where $\alpha_{ij} = \frac{r_{ij}}{V_iV_j} \mathrm{Cos}(\partial_i - \partial_j)$ and $\beta_{ij} = \frac{r_{ij}}{V_iV_j} \mathrm{Sin}(\partial_i - \partial_j)$

$$Q_L = \sum_{i=1,j=1}^{n} \left[¥_{ij}\left(P_iP_j + Q_iQ_j\right) + \lambda_{ij}\left(Q_iP_j - P_iQ_j\right) \right] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots..2.2$$

Where $¥_{ij} = \frac{x_{ij}}{V_iV_j}\,\mathrm{Cos}(\partial_i - \partial_j)$ and $\lambda_{ij} = \frac{x_{ij}}{V_iV_j}\,\mathrm{Sin}(\partial_i - \partial_j)$

The voltage at the nodes should be within the limits

$$V\min \le |Vi| \le V\max$$

Where

Vi - Voltage magnitude at bus i

Vj - Magnitude of voltage at bus j

Vmin and Vmax are the minimum and maximum voltage limits respectively.

P_L and Q_L are active and reactive power losses

P_i and Q_i are the active and reactive powers at bus i

P_j and Q_j are the active and reactive powers at bus j.

a. To find the size of DG

The penetration level of DG is chosen based on the following equation. .

$$PLDG\% = \frac{\text{Size of DG}}{\text{Total demand}} * 100 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots..2.3$$

Where, PLDG% is penetration Level of DG

b. To find the location of DG

Sensitive node: These are the nodes of the test system which are very sensitive towards the fault or disturbance in the system. The maximum variation of voltage and current can be observed at these nodes. These nodes are selected based on the interconnection of the lines and busses which leads to junction. In IEEE 33bus radial distribution system the sensitive nodes can be selected as node 2, node3 and node6.

Low voltage bus: This is the bus chosen after load flow on the selected test system. Integrating DG at this low voltage bus will improve the voltage profiles of the system.

Maximum power losses bus: This is the bus chosen after load flow on the selected test system. Integrating DG at this Maximum power loss bus will reduces the losses of the system.

Tail end node: These are the nodes of the test system which are the buses connected to the end branches. Usually the low voltage at these buses will be low. In IEEE 33bus radial distribution system the sensitive nodes can be selected as node 25, node33, node18 and node22.

Bus with maximum load: This is the bus with maximum load in the considered test system. Usually these busses will be having increased losses and weak voltage profiles.

Node near to source: The bus near to the main source is considered for integration of DG to analyze the impact of integration leads to a chance of reverse power flow as well.

III. Methodology

The steps of execution of the algorithm are given as follows

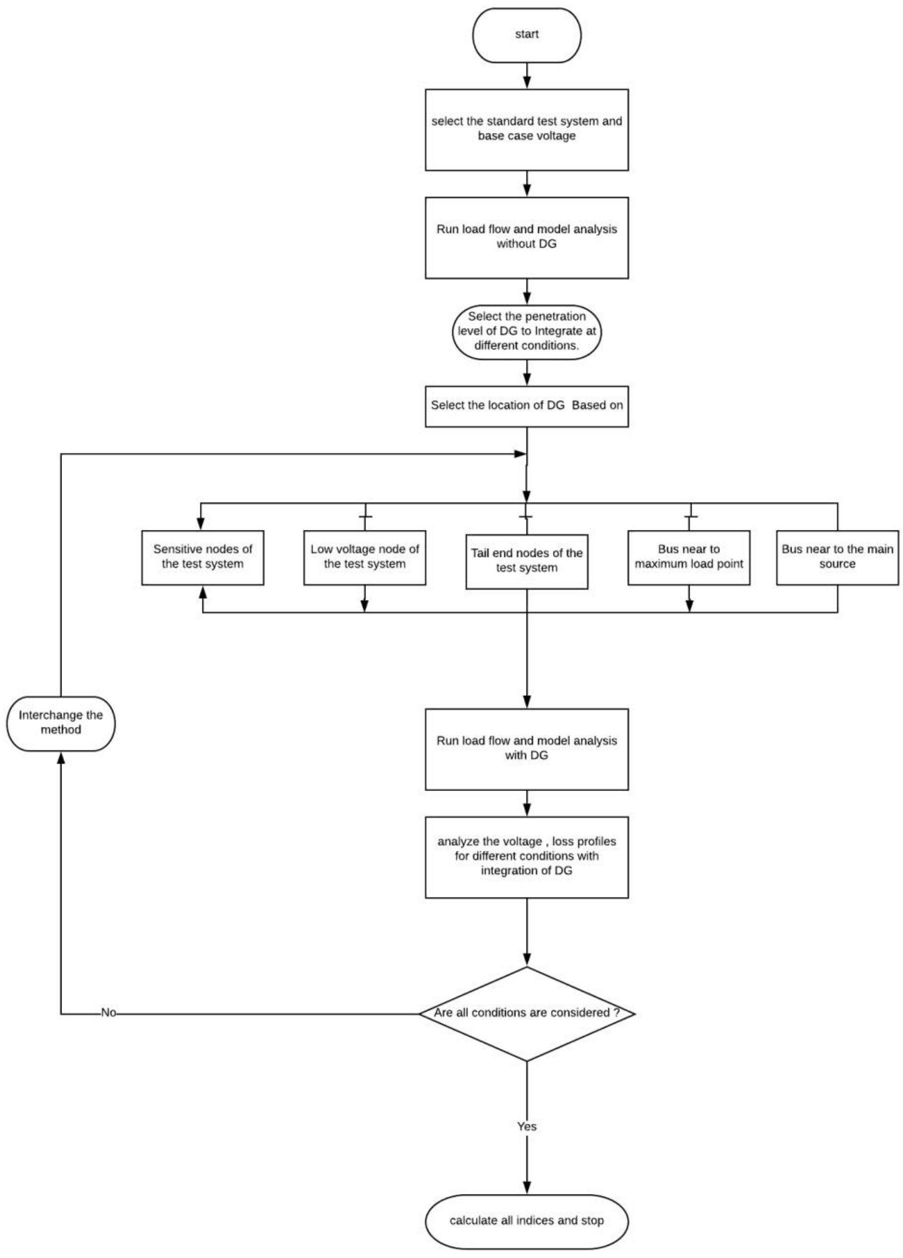

Fig 1: Flowchart for the proposed method

Step1: Select the standard test system with all base case parameters

Step 2: Run load flow on the selected test system and the different parameter values

Step 3: Select the size of DG by using equation

Step 4: Select the location of DG by selecting Sensitive node, Low voltage bus, Tail end node, bus with maximum load, node near to switch (if any) and node near to source.

Step 5: Integrate DG with particular penetration at the above said locations and run load flow.

Step 6: Check for the impact of DG at different locations by considering voltage profile, Active and Reactive power losses and other indices.

Step 7: If Integration of DG is done for all the conditions. Stop the execution and show the impact of DG integration behavior at different nodes based on the selected conditions.

III. RESULTS AND DISCUSSIONS

This method is applied to the standard IEEE 33 bus system operated at 12.66kV level of voltage and consists of 33 busses, 32 branches, with 3715kW and 2300kVar of power respectively as shown in Figure.3.1. The base case load flow is obtained where the power losses without the connection of the DG's are 202.68kW and 143.22kVAr respectively.

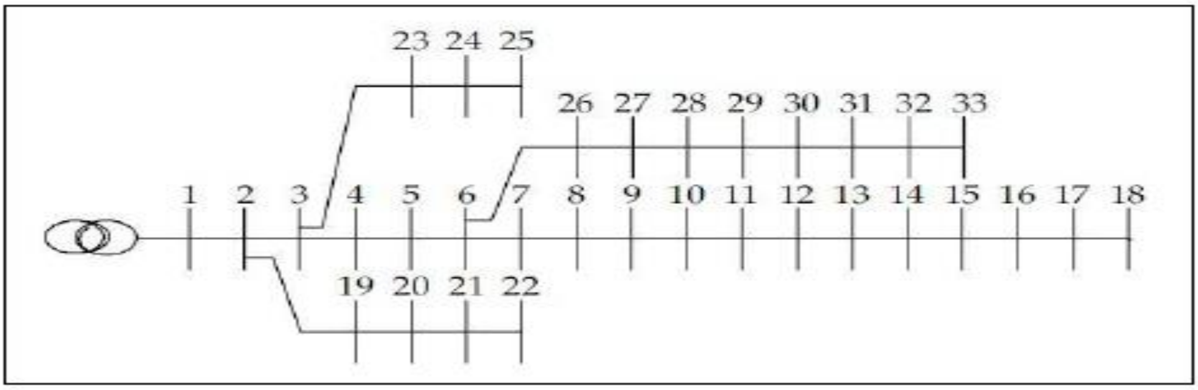

Fig.2: Single diagram of IEEE 33 bus test system

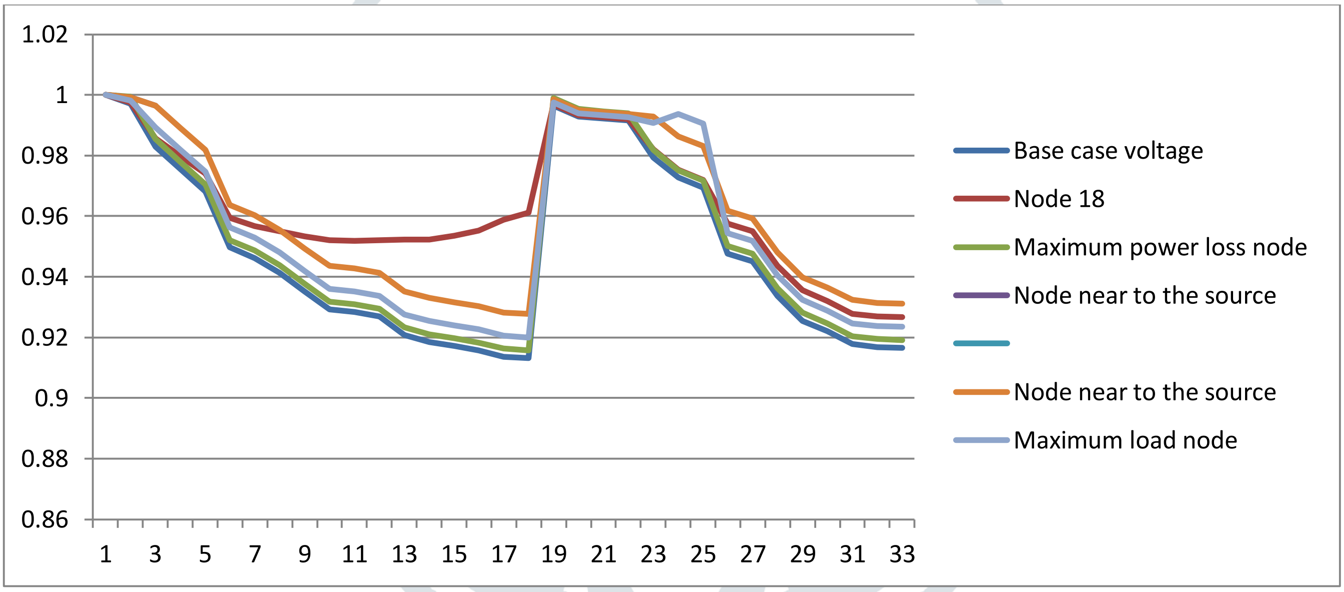

Fig 3: Voltage profiles of DG integration at 50% penetration for different methods

Fig. 3 shows the voltage profiles at 50% DG penetration level for the case of base case, maximum power loss node, low voltage node and maximum load node . the voltage profiles are improved compared to the base case in all the methods, maximum improvement can be observed when the DG is integrated at minimum voltage bus compared to the other methods.

Table 1: power loss profiles for maximum power loss node, low voltage node and maximum load node.

Active power loss variation at different nodes after Integration of DG at 50% Penetration level					
Bus no	Base case Power losses	At Minimum voltage node	At Maximum power loss node	At Node near to the source	At Maximum load bus
1	12.24	9.259	4.1333	3.37	7.2136
2	51.791	37.901	16.147	14.882	28.731
3	19.9	13.07	6.4447	19.3	19.679
4	18.699	12.017	6.2842	18.132	18.49
5	38.249	24.354	13.291	37.086	37.821
6	1.9145	0.58653	1.7695	1.8568	1.8933
7	4.838	1.1205	4.4687	4.6908	4.7838
8	4.1805	0.71987	3.8585	4.0522	4.1333
9	3.5609	0.63672	3.2859	3.4513	3.5206

10	0.5537	0.11331	0.51085	0.53662	0.54742
11	0.88113	0.20029	0.81283	0.8539	0.87111
12	2.6662	0.8177	2.459	2.5836	2.6358
13	0.72916	0.35011	0.67242	0.70653	0.72083
14	0.35697	0.59785	0.32913	0.34587	0.35289
15	0.28147	0.99283	0.25948	0.2727	0.27824
16	0.25163	2.1783	0.23195	0.24378	0.24874
17	0.053136	1.54	0.048978	0.051477	0.052525
18	0.16095	0.16082	0.16045	0.16026	0.1607
19	0.83218	0.83148	0.82956	0.82861	0.83088
20	0.10076	0.10067	0.10044	0.10033	0.1006
21	0.043634	0.043598	0.043497	0.043447	0.043566
22	3.1816	3.1643	3.1171	3.094	0.97762
23	5.1437	5.1156	5.0392	5.0017	2.1202
24	1.2875	1.2804	1.2612	1.2518	4.6153
25	2.6009	2.5454	2.4013	2.5214	2.5716
26	3.329	3.2578	3.073	3.227	3.2915
27	11.301	11.059	10.43	10.954	11.173
28	7.8333	7.6653	7.2291	7.5925	7.7447
29	3.8957	3.812	3.5948	3.7757	3.8515
30	1.5936	1.5592	1.47	1.5443	1.5755
31	0.2132	0.20859	0.19664	0.20659	0.21077
32	0.013169	0.012884	0.012145	0.012761	0.013018

Table 1 Shows power loses for base case, maximum power loss node, low voltage node and maximum load node. The power losses are reduced for maximum power loss method compared to the other methods.

Fig. 4 shows the voltage profiles at 50% DG penetration level for the case of base case and sensitive nodes. The voltage profiles are improved compared to the base case in all the methods, maximum improvement can be observed when the DG is integrated at node 6 compared to the other nodes.

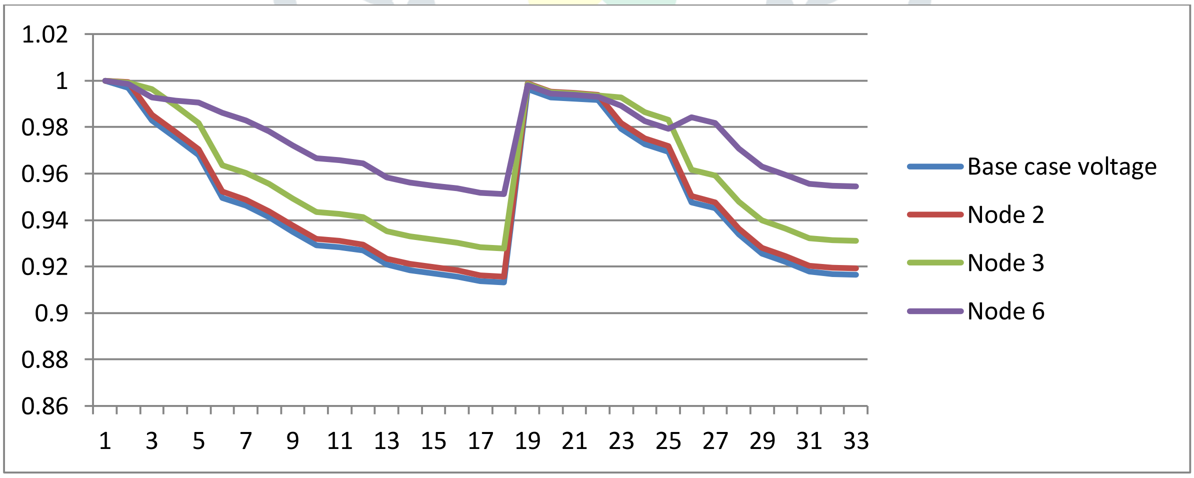

Fig 4: Voltage profiles of DG integration at 50% penetration for sensitive nodes

Table 2: Active power loss variation at different nodes after Integration of DG at 50% Penetration level

		DG integration at Sensitive nodes			DG integration at Tail end nodes			
Bus no	Base case	Ploss at node 2	Ploss at node 3	Ploss at node 6	Ploss at node 25	Ploss at node 33	Ploss at node 18	Ploss at node 22
1	12.24	4.1333	3.37	7.2432	3.4241	6.0781	9.259	7.2136
2	51.791	16.147	14.882	28.829	51.513	23.837	37.901	28.731
3	19.9	6.4447	19.3	9.2204	19.791	19.612	13.07	19.679
4	18.699	6.2842	18.132	8.3622	18.595	18.427	12.017	18.49
5	38.249	13.291	37.086	16.882	38.036	37.69	24.354	37.821
6	1.9145	1.7695	1.8568	1.8418	1.904	1.8868	0.58653	1.8933
7	4.838	4.4687	4.6908	4.6527	4.8111	4.7673	1.1205	4.7838
8	4.1805	3.8585	4.0522	4.0189	4.1571	4.1189	0.71987	4.1333
9	3.5609	3.2859	3.4513	3.4229	3.5409	3.5083	0.63672	3.5206
10	0.5537	0.51085	0.53662	0.53219	0.55058	0.5455	0.11331	0.54742
11	0.88113	0.81283	0.8539	0.84685	0.87616	0.86806	0.20029	0.87111
12	2.6662	2.459	2.5836	2.5622	2.6511	2.6266	0.8177	2.6358
13	0.72916	0.67242	0.70653	0.70068	0.72503	0.71829	0.35011	0.72083
14	0.35697	0.32913	0.34587	0.34299	0.35495	0.35164	0.59785	0.35289
15	0.28147	0.25948	0.2727	0.27043	0.27986	0.27726	0.99283	0.27824
16	0.25163	0.23195	0.24378	0.24175	0.2502	0.24786	2.1783	0.24874
17	0.053136	0.048978	0.051477	0.051048	0.052833	0.052339	1.54	0.052525
18	0.16095	0.16045	0.16026	0.16071	0.16018	0.16063	0.16082	0.1607
19	0.83218	0.82956	0.82861	0.8309	0.82818	0.83048	0.83148	0.83088
20	0.10076	0.10044	0.10033	0.1006	0.10027	0.10055	0.10067	0.1006
21	0.043634	0.043497	0.043447	0.043567	0.043424	0.043545	0.043598	0.043566
22	3.1816	3.1171	3.094	3.1499	3.1657	2.2925	3.1643	0.97762
23	5.1437	5.0392	5.0017	5.0923	5.1178	5.1541	5.1156	2.1202
24	1.2875	1.2612	1.2518	1.2746	1.281	1.2332	1.2804	4.6153
25	2.6009	2.4013	2.5214	1.3923	2.5864	2.5627	2.5454	2.5716
26	3.329	3.073	3.227	1.9278	3.3104	3.28	3.2578	3.2915
27	11.301	10.43	10.954	7.1657	11.237	11.134	11.059	11.173
28	7.8333	7.2291	7.5925	5.5283	7.7894	7.7177	7.6653	7.7447
29	3.8957	3.5948	3.7757	3.5144	3.8738	3.8381	3.812	3.8515
30	1.5936	1.47	1.5443	4.4697	1.5846	1.57	1.5592	1.5755
31	0.2132	0.19664	0.20659	1.9156	0.21199	0.21002	0.20859	0.21077
32	0.013169	0.012145	0.012761	3.0682	0.013094	0.012973	0.012884	0.013018

Table 2 Shows power loses for base case, sensitive nodes and tail end nodes. The power losses are reduced for tail end nodes compared to the sensitive nodes.

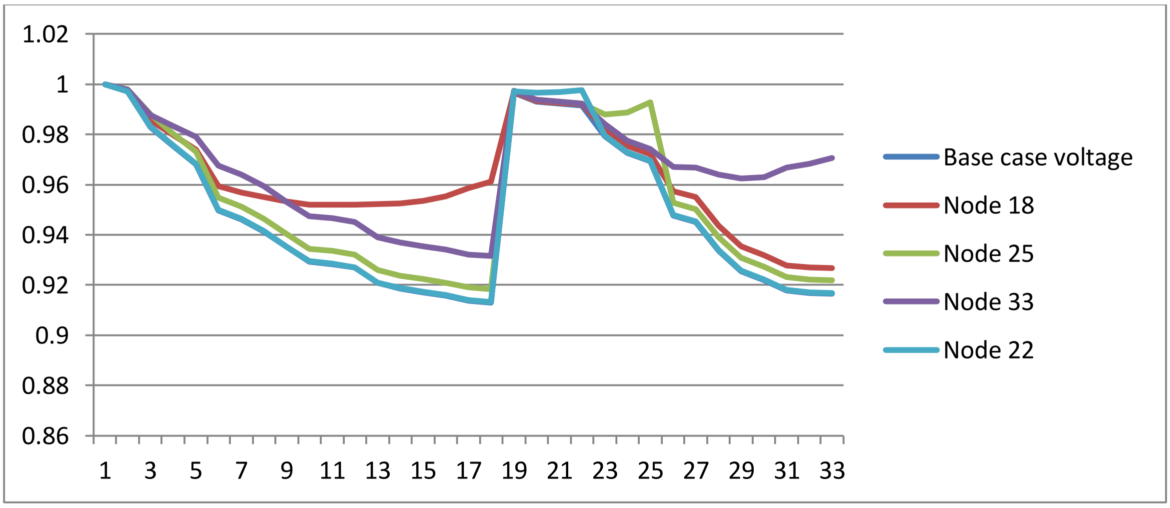

Fig 5: Voltage profiles of DG integration at 50% penetration for tail end nodes

Fig. 5 shows the voltage profiles at 50% DG penetration level for the case of base case and tail end nodes. The voltage profiles are improved compared to the base case in all the methods, maximum variation in the profile can be observed when the DG is integrated at node 18 and node 33 compared to the other nodes.

IV. CONCLUSION

In this paper, The DG with selected penetration level is integrated at sensitive node, Low voltage bus, Tail end node, bus with maximum load and node near to source to analyze the impact of DG integration on the test system(location). Impact of integration of dg includes both positive and negative impacts. In this paper the negative impacts are studied and methods to reduce them are proposed by considering the location of the DG. The DG siting plays a very important role for the reduction of the power losses and improving the voltage profile. In view of this, the methods have been opted for the study, the results of which are shown with improved quality of power. .

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