Voltage Control of Two Bus Power System using CMLI based STATCOM

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Abstract: The following paper, introduces a synchronous compensation (STATCOM) based on a 9-level Cascaded Multilevel Inverter (CMLI) using a phase-shifted PWM technique. The STATCOM used here is controlled such in order to provide the reactive power compensation at the point of common coupling (PCC) for a R-L lagging load. The PS-PWM is used for minimizing the harmonic content of the CMLI terminal voltage. The d-q axis transformation is used for decoupling the active and reactive power components for simplifying the compensating power regulation. Double loop control strategy consisting of PI controllers is employed, for achievement and maintenance of nominal load bus voltage and a faster dynamic response.

Index Terms **- STATCOM, PS-PWM, CMLI, PCC, Phase locked loop (PLL)**

I. INTRODUCTION

Flexible AC Transmission Systems (FACTS) as per IEEE is characterized as a integration of power electronic based system with static equipment's which are capable of controlling multiple parameters of AC transmission system in order to improve the controllability and capable of increasing the power transfer capability. In recent time, FACTS are most preferred in power systems as it is capable of enhancing system utilization capacity as well as power transfer capability. Some other advantage of using FACTS devices are increase in reliability, improving stability, and better power quality of system interconnections. STATCOM, a member of shunt device family of FACTS is capable of providing reactive power compensation, damping of active power oscillation, improving voltage regulation, etc. The two important types of the VSI for power systems involving bulk power and higher voltage levels are - multi-pulse inverter (MPI) and multilevel inverter (MLI) [2-4]. As there is no need of bulky zig-zag transformers in MLI, therefore MLI scheme is far more enticing for its utilization in STATCOM [6-7]. There are three basic topologies of MLI namely- Diode-Clamped (DC-MLI), Flying-Capacitor (FC-MLI) and Cascaded H-bridge (CMLI). The CMLI has several advantages in comparison to other basic topologies of MLI like modular structure, no need of clamping diodes and voltage balancing capacitors as used in other topologies, ease of designing etc [10]. In addition to these advantages, several modulation schemes like staircase scheme, Space Vector Modulation (SVM) and carrier-based sinusoidal pulse width modulation (SPWM) have been developed for control of switching devices.

In this paper, a double loop control strategy used for a nine-level CMLI based STATCOM is proposed. PS-PWM is used for generating firing pulses for inverter devices and to eliminate lower-order harmonics of inverter terminal voltage. The abc to d-q transformation is used for decoupling the active and reactive components of the current and voltage in order to regulate load bus voltage or for reactive power compensation.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

The basic unit of CMLI is the H-bridge inverter cell. Fig. 1 shows the structure of a H-bridge inverter cell. The different voltage levels: $+V_{dc}$,0 and $-V_{dc}$ are obtained by using different combinations of switching state. When S_{A11} and S_{A14} conducts at

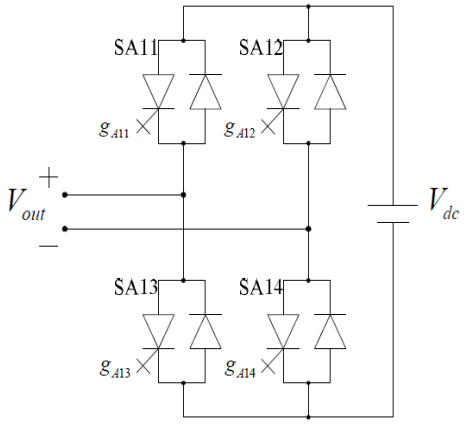

Fig.1 Single phase H-bridge cell

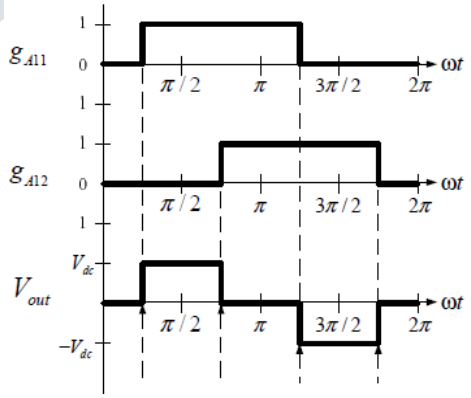

Fig.2 Gate signals with output voltage

the same time ,then $V_{out} = +V_{dc}$, and when S_{A12} and S_{A13} conducts at the same time, then $V_{out} = -V_{dc}$. At other switching states, $V_{out} = 0$, but there is a condition that the upper switch and lower switch of same inverter leg must have to operate in such a manner that only one switch must turn on at a time and while the other switch is turned off.

In CMLI multiple H-bridge cells are connected in series for producing high-voltage with low harmonic AC output. For a three-phase CMLI, in order to obtain output phase voltage of n number of levels, the number of isolated dc supplies and active switches required in each phase are (n-1)/2 and 2(n-1) respectively[2].

III. Phase Shifted SPWM (PS-SPWM)

The scheme used to switch of the active switches of the STATCOM voltage source converter should utilize the topology selected and the type of active switches for producing VAr to be supplied to the system. In multi-pulse STATCOM, GTOs are used which are capable of switching at higher frequency. Therefore high frequency PWM pattern is implemented. As multi- level inverter type of voltage source converter are capable of switching with fundamental frequency and unnecessity of the coupling transformer for connection when voltage is not exceptionally high ,therefore it becomes helpful in reducing the total switching losses[10]. This provides the basis for the selection of PWM scheme.

In this paper, PS-SPWM is implemented for generating firing pulses and to eliminate lower order harmonics from the inverter output voltage. MLI with 'n' number of voltage levels requires(n-1) number of triangular carriers having equal peak-to-peak amplitude and frequency and one sinusoidal modulating wave is used as a reference signal for each phase leg. In Phase-shifted SPWM, all the triangular carriers are phase shifted with an angle, which is given by:

$$\text{Angle between each adjacent carriers} = \frac{360}{n-1} \qquad (1)$$

As the CMLI implemented in this paper is of 9 –level, therefore number of carriers is 8 and angle between each adjacent carrier is 45^{o}. Fig.3 shows the arrangement of carriers for generating firing pulses for devices of CMLI and Table 1 shows the parameters used for PWM scheme. The output phase and line voltage are shown in Fig. 4 and Fig. 5 respectively. Fig.6 and Fig. 7 shows the THD analysis of CMLI phase and line output voltages.

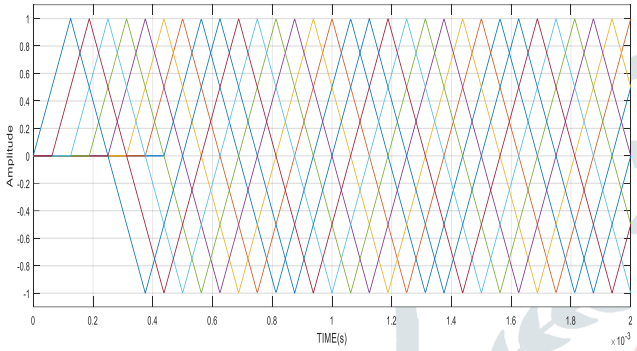

Fig. 3 Carrier arrangement for PS-SPWM

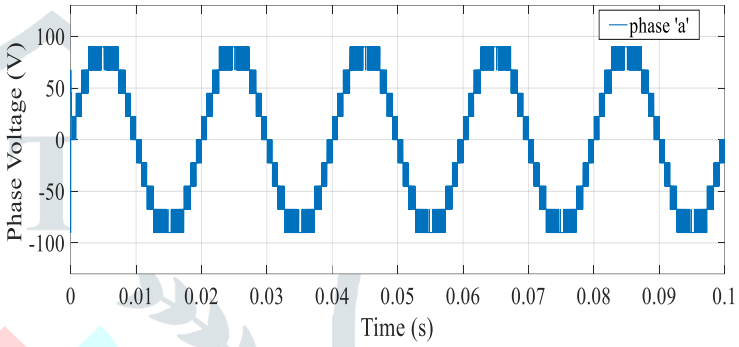

Fig.4 Phase output voltage of 9-level CMLI

Table 1 Parameters of PS-SPWM

Parameter	Value
Reference Frequency	50Hz
Carrier Frequency	2000Hz
Frequency Modulation Index	40

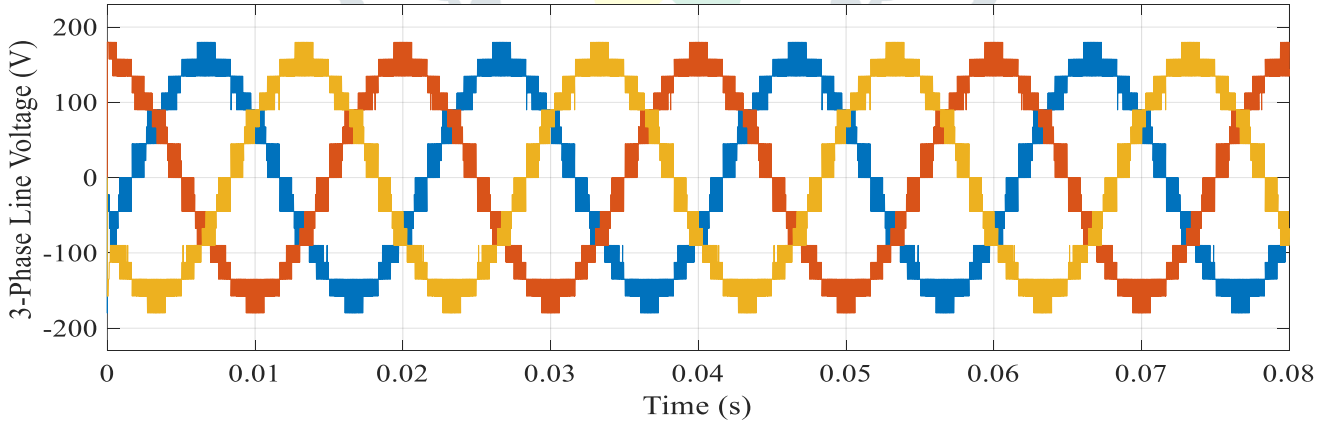

Fig.5 Line output voltage of 9-level CMLI

The major disadvantage of power electronics based compensating devices is that when integrated, it injects harmonics in the AC power system. The pulse width modulation used reduces the lower order harmonics but in order to eliminate the higher order harmonics present in the output of the CMLI, an L-C tuned filter is required. The parameters obtained after tuning the L-C filter used here, are as follows:

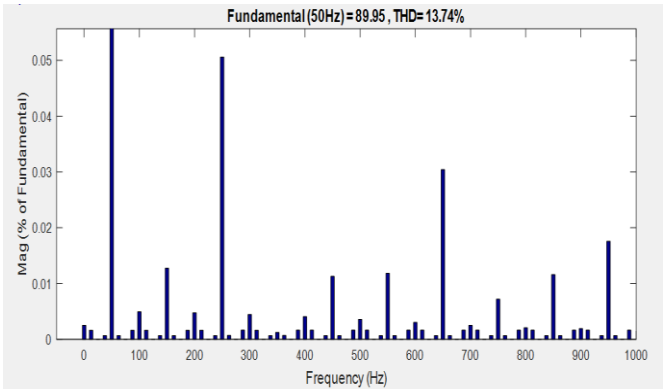

Fig.6 FFT analysis of Output Phase voltage of 9- level CMLI

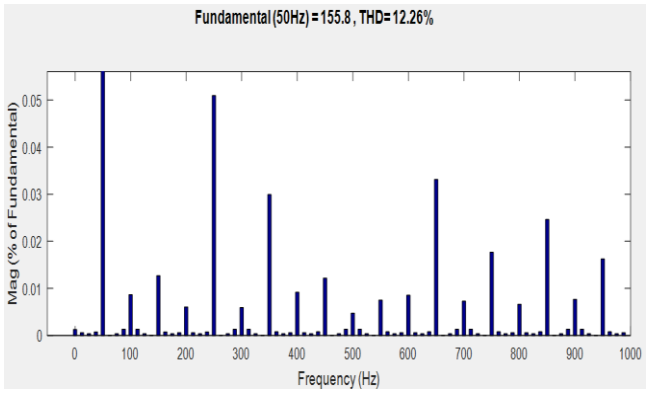

Fig.7 FFT analysis of Output Line voltage of 9- level CMLI

Table 2. Parameters of L-C tuned filter

Parameters	Tuned Values
R_1 – L	R_1 = 2 Ω , L = 6.5 mH
R_2 – C	R_2 = 0.2 Ω , C = 100 μF

The FFT analysis of the Output line voltage of CMLI with an L-C tuned filter is shown in Fig. 8. With the elimination of higher order harmonics, the THD of CMLI output line voltage is reduced to 0.4 %. Thereby, meeting our purpose of maintaining power quality of AC power system when STATCOM is integrated for voltage control.

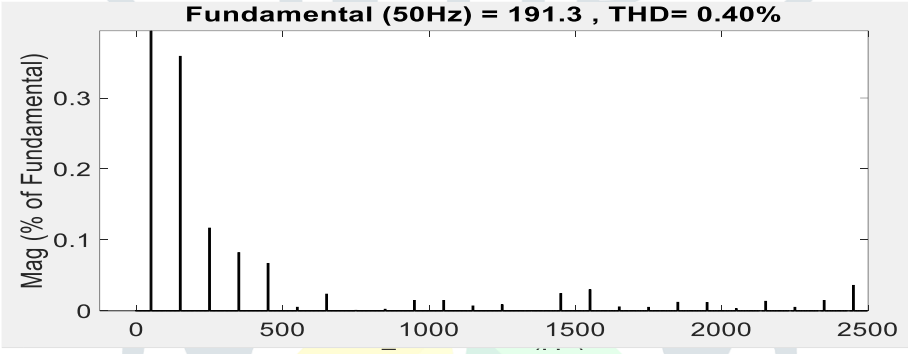

Fig.8 FFT analysis of the Output line voltage of CMLI with an L-C tuned filter

IV. CASCADED MULTILEVEL INVERTER BASED STATCOM

Fig. 9 shows the proposed circuit of 9-level CMLI based STATCOM. The STATCOM consist of a generic CMLI, which is connected to power system bus through coupling reactors. The output voltage of the STATCOM must maintain synchronism with the bus voltage to which it is connected, which is achieved by using three- phase PLL. The voltage phasor angle and magnitude of STATCOM and system bus decide the exchange of active and reactive power between them [9]. In Fig.9, if E_1 represents the

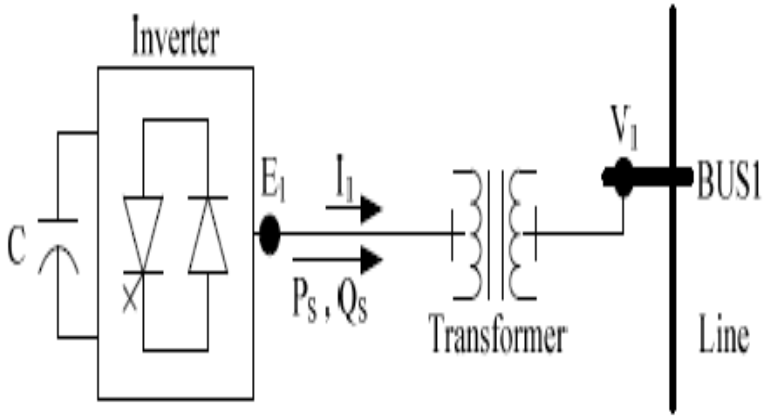

Fig.9 STATCOM schematic diagram

STATCOM terminal output voltage phasor, and V_1 represents the system bus voltage phasor to which the STATCOM is coupled. When E_1 higher than the system bus voltage V_1 , then the STATCOM injects lagging VARs to the AC power system and vice-versa.

V. DESIGN OF CONTROLLER

In this paper, a direct control strategy is implemented. In this control technique, output voltage of the STATCOM is varied by changing the modulation index i.e. by changing the angles of the voltage levels at the output keeping the dc source voltage constant.

The mathematical model of CMLI is transformed to the stationary rotating reference frame. Fig. 10 shows proposed block diagram for the control of CMLI based STATCOM. The d - q axis reference voltage components of STATCOM, e_d and e_q are controlled as:

$$e_d = x_1 + v_d - \omega L i_q \quad (2)$$

$$e_q = x_2 + \omega L i_d \quad (3)$$

where, v_d is the d – axis component of the ac load bus voltage and i_d and i_q are d-axis and q-axis current components of the CMLI line current respectively. The load bus voltage vector is aligned with synchronously rotating frame, therefore the q – axis component of the load bus voltage v_q is made equal to zero. The control parameters x_1 and x_2 are controlled as

$$x_1 = \left(K_{p1} + \frac{K_{i1}}{s} \right) (i_d^* - i_d) \quad (4)$$

$$x_2 = \left(K_{p2} + \frac{K_{i2}}{s} \right) (i_q^* - i_q) \quad (5)$$

$$i_q^* = \left(K_{p3} + \frac{K_{i3}}{s} \right) (V_{load(rms)}^* - V_{load}^{actual}) \quad (6)$$

$$\text{M.I.} = \frac{\sqrt{e_d^2 + e_q^2}}{V_{dc}} \quad (7)$$

Where, V_{dc} represents the total dc link voltage.

The control model used forms a double loop, in which the outer loop gives reference active and reactive currents for controlling or maintaining the voltage at PCC. The inner loop controls the line current of the STATCOM to achieve the desired reference values of active and reactive current with zero steady state error.

Fig. 10 shows functional block diagram of CMLI based STATCOM. The instantaneous load bus voltage, V_{load}^{actual} is compared with its reference voltage, V_{ref} (=110V). The error is fed to PI-controller of ac voltage controller to generate q-axis reference current i_q^* which is compared with STATCOM line current q-axis for generating STATCOM q-axis reference voltage, e_q. Similarly, STATCOM d-axis reference voltage, e_d and therefore e_q and e_d are used calculation of amplitude modulation index of STATCOM PS-PWM. Three phase PLL is used for synchronizing the STATCOM output voltage with that of load bus voltage. Fig.10 shows the waveforms of STATCOM output voltage and load bus voltage.

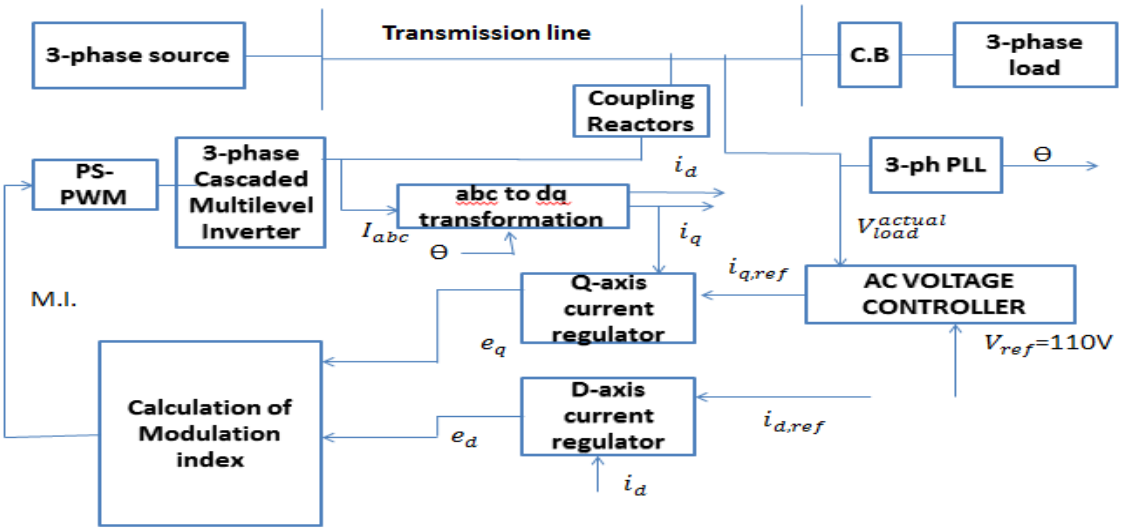

Fig.10 Block diagram of CMLI based STATCOM

VI. SIMULATION RESULTS

The Cascaded Multilevel STATCOM is considered for simulation. The simulation study is carried out using MATLAB/SIMULINK. The system parameters are shown In Table 3.

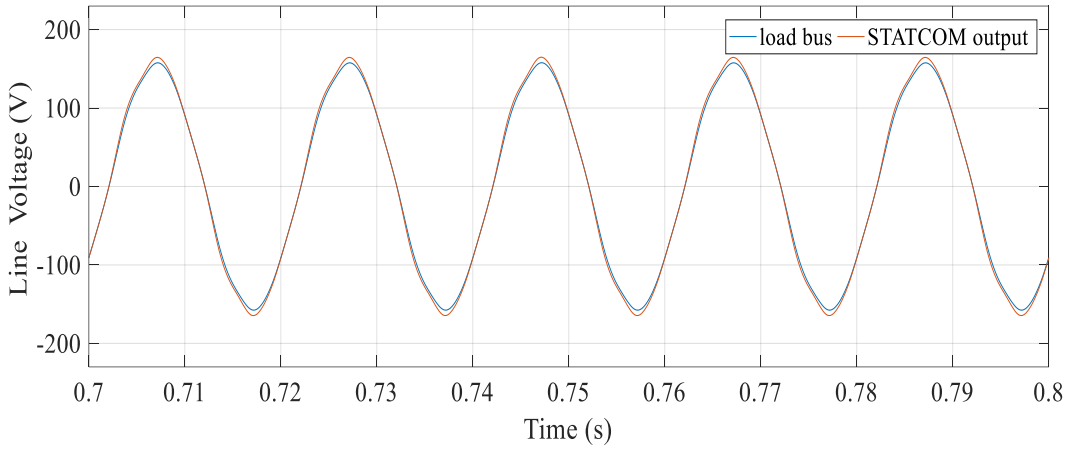

Fig. 11 Synchronised STATCOM output and load bus voltage

Initially the system is operating at no load and the load bus is operating at voltage of 1 pu . If a load of 1.1 kVA load of 0.707 pf lag is connected to the load bus at t=0.08 sec, the voltage dips (sags) to 0.846 pu. STATCOM with double loop control strategy is connected to the AC system load bus at the point of common coupling (PCC) at time, t = 0.2 s. The load bus voltage overshoots to 1.022 pu but the voltage is soon restored to 0.997 pu at t= 0.534 s. Fig.12 shows the three- phase load bus line voltage under load variation with CMLI based STATCOM using double loop control strategy connected at the PCC. Fig. 13 shows the magnitude for load bus voltage for load variation.

Table 3. System parameters

Supply Voltage	110 V (RMS)
Nominal load voltage	110 V (RMS)
DC link voltage	23.2 V
Coupling Reactors	R = 0.04Ω , L = 0.1 mH
AC Voltage controller gains	K_p=5 , K_i=22.5
Current regulator gains	Kp=1.4 , Ki=0.35

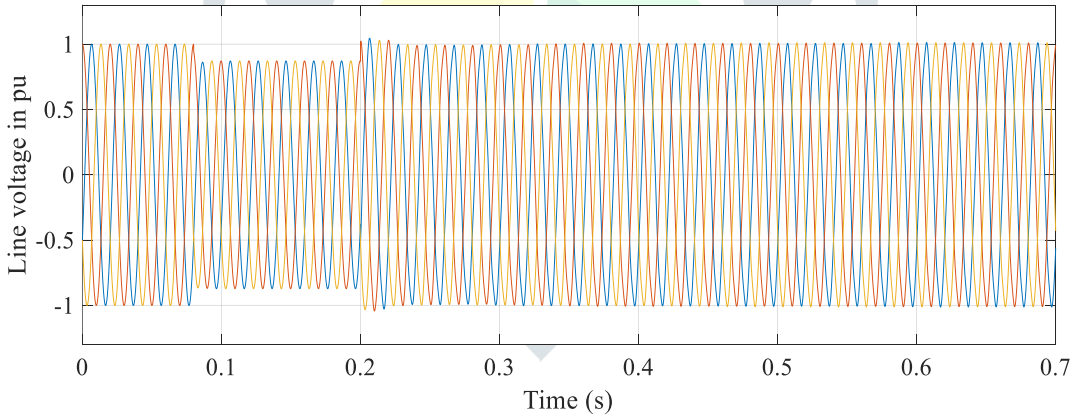

Fig. 12 Load bus voltage using double loop control strategy

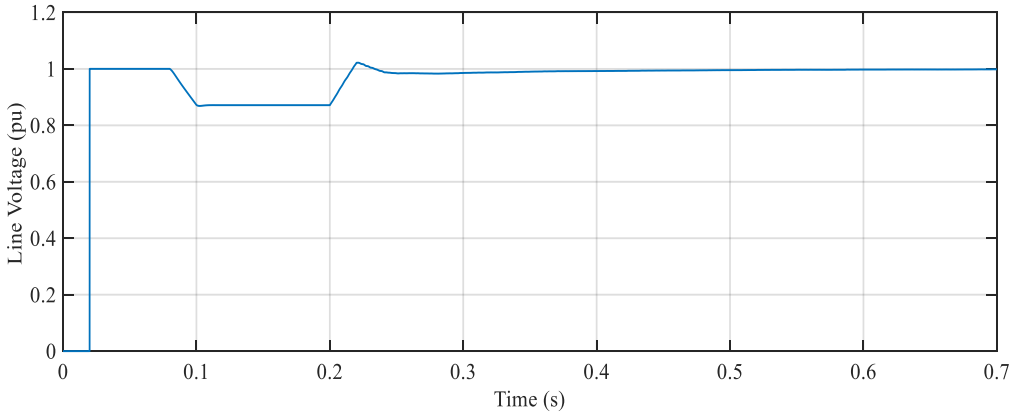

Fig. 13 Line voltage in per unit using double loop control strategy

For maintaining the voltage of the load bus to nominal , STATCOM injects the lagging VARs to the AC power system in order to fulfill the reactive power demand of load and the transmission line. Fig. 14 shows the reactive power exchange between STATCOM and AC power system.

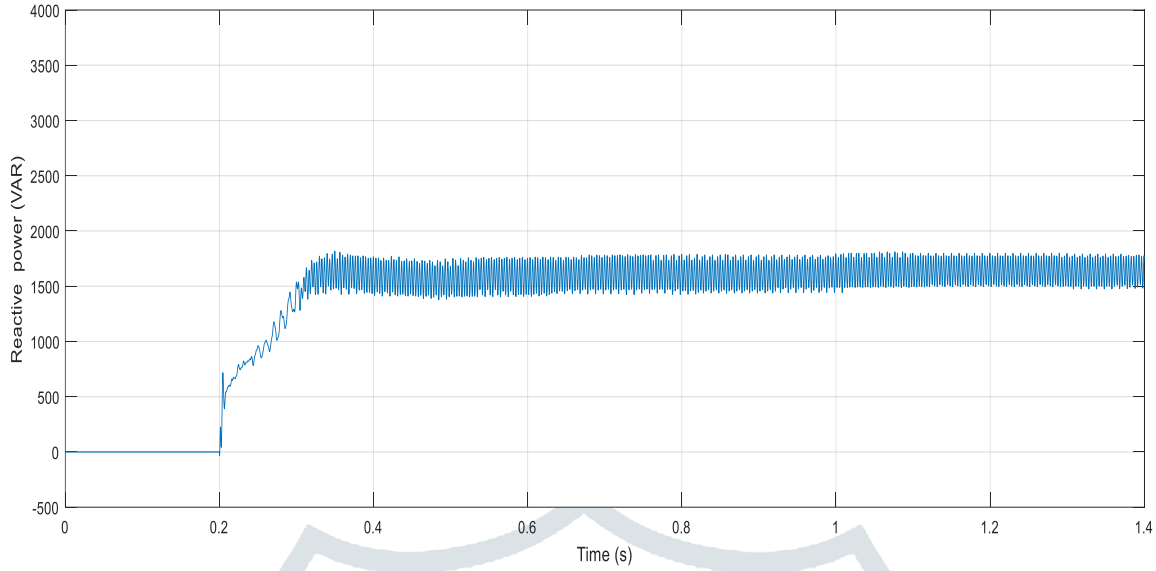

Fig. 14 Reactive power exchange between STATCOM and AC power system.

When CMLI based STATCOM is connected at PCC for voltage regulation of load bus, then the combined effect of Phase – Shifted PWM and L-C tuned filter reduces harmonic content injected in the AC power system, hence improving the power quality. Fig. 15 shows the FFT analysis of the load bus line voltage at steady state.

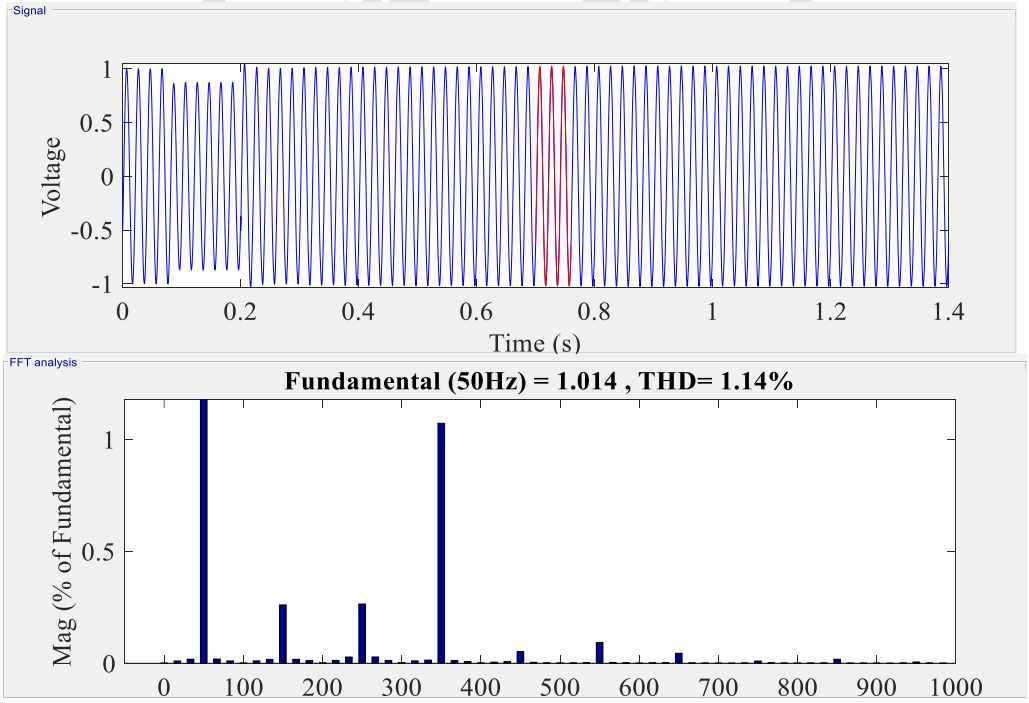

Fig. 15 FFT analysis for line voltage of load bus using double loop control strategy

VII. CONCLUSION

In this paper, a 9- level CMLI along with a phase–shifted PWM switching scheme and a direct control used as a STATCOM. The direct control strategy is used for voltage control which is faster in comparison to the indirect voltage control technique. The control strategy used here consists of double loops in which inner current loop helps in faster dynamic response, hence achieving and maintaining the nominal voltage within 0.3secs. Also the receiving end voltage is maintained approximately equal to the sending end voltage by providing local reactive power support. Therefore reducing losses in the transmission line, better system utilization and higher stability.

This paper also highlights the THD improvement of the load bus voltage to be 1.4%, by using the novel 9-level CMLI based STATCOM within 5%, as per IEEE standards 519. Hence, improving the Power quality immensely by reducing the effect of harmonics to a minimal.

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