FPGA BASED MOTION CONTROLLER FOR ROTATING PLATFORM

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ABSTRACT: The project is to design a controller for positioning a mechanical rotating platform based on position commands. The mechanical platform can be moved in both azimuth and elevation angles. The platform consists of DC motors, associated drive circuitry, encoders and brake for the motors. In this mechanism, the command is received through the serial communication channel from the external system. In the platform, after disabling the brake and applying some control voltage, the platform starts rotating for positioning. Simultaneously the counter starts counting the pulses. After some degrees of rotation, the speed is increased to maximum by increasing the control voltage and the speed is decreased when the platform seems to attain its desired position. And then, when current position equals to the desired position, the brake is enabled by removing the applied voltage signal. Then the position feedback is sent through the serial channel.

Index Terms: Field Programmable Gate Array, UART, DC Motor, Motor Driver, DAC etc

I. INTRODUCTION

Importance Of Defense Against Anti-Ship Missiles:

The maritime combat scenario of today is filled with complex multidimensional threats for a man of war. Conflicts in the past quarter century or so have shown that warships have grown more vulnerable to aerial threats, in particular to anti-ship missiles.

II. EARLIER WORKS

MICRO CONTROLLER

The Existing System consist of Micro controller ,the draw back in the system is sampling is limited only at the run time .The micro controller cannot interface high power devices directly .It has more complex structure .It only perform limited number of executions simultaneously .It is generally used in micro equipment .The Micro controller has increased computational time and high computational delays.

The Micro controllers cannot be reprogrammed, they have a fixed architecture which makes them more costly. Micro controllers can execute on many cores with out-of-order instructions, not all functions are well-suited to this approach, like massive image or digital signal processing applications. A micro controller like an application-specific integrated circuit in a prototype or in limited production designs.

III. Proposed System

A. FPGA (Field Programmable Gate Array)

The Proposed system consist of FPGA there are advantages of using an FPGA, the benefits are that they are very flexible, reusable, and quicker to acquire. An FPGA likely has a quicker time-to-market because they are not pre-designed to perform certain tasks.

The FPGA has a simpler design cycle to manage and requires less manual intervention. The software will handle much of the routing, placement, and timing automatically to match the programmed specification. Because FPGA's are re programmable, they are reusable, making them flexible for faster prototyping and mistakes are not so costly.

B. OPTO Mechanical design:

To overcome the limitations, here H-Bridge has been replaced by Optocoupler. Advantage of this is interfacing with logical circuits by preventing FPGA, motor from noise and other defective damages.

Control circuits are well protected due to electrical isolation. As it is unidirectional, signal transfer noise from the output side does not coupled to the input side of the circuit. Hence it is a small and light weight device so; it doesn't make the circuit bulkier. It transfers data at incredibly high speed.

IV. BLOCK DIAGRAM DESCRIPTION

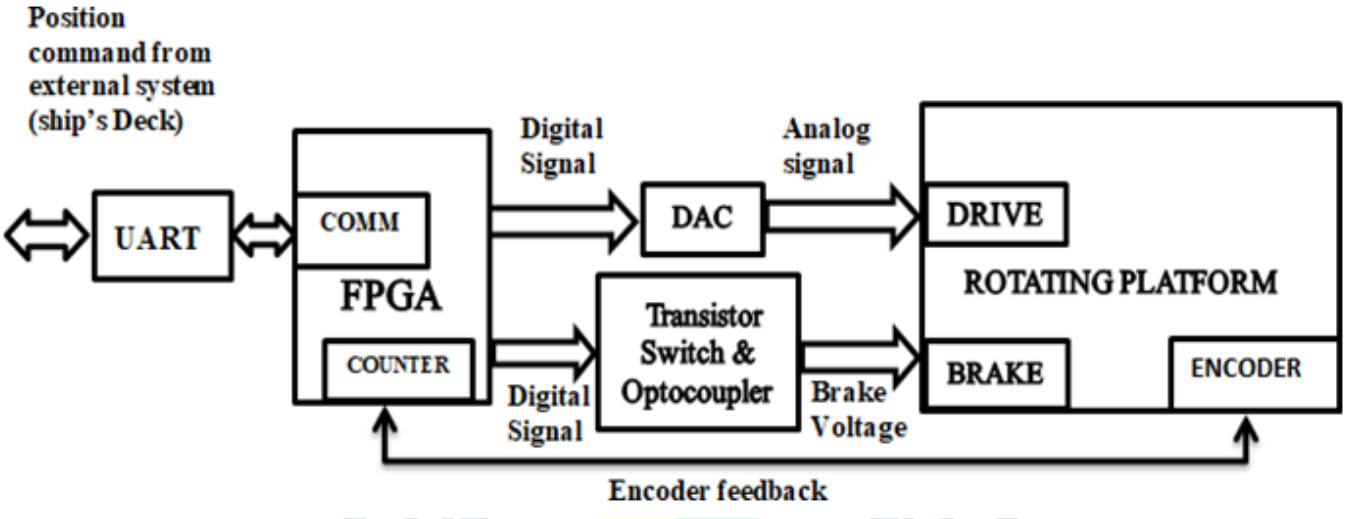

Figure 1: Block Diagram

Communication interface: A serial communication channel has to be provided to receive position commands from external system/PC. Serial Communication through RS422 protocol is suitable for this. Implementation of RS422 protocol requires addition circuitry using UART ICs.

Drive Interface: The platform is capable of rotating at a maximum speed of 60 rpm. It has got inbuilt circuitry for driving the motors. It requires an analog control voltage of -10V to +10V to control the speed and direction of motors. Motor moves at maximum speed when maximum voltage of 10V is applied and speed changes proportional to the applied voltage. Positive voltage moves the motor in clockwise direction and negative voltage moves it in the anticlockwise direction. Considering the effect of inertia on large mechanical systems, the platform motion has to be Started at slow speed. Similarly, at the time of stopping, speed should be slowed down for accurate positioning. A Digital to Analog Convertor (DAC) IC is required to generate this analog voltage from digital output of FPGA.

Brake Interface: The mechanical platform has an electromechanical braking system which has to be applied/ released when at the start/stop of the motion, using a 15V brake disable/enable signal. Application of this signal has to done using a transistor as switch. The brake signal circuitry has to be isolated from the FPGA circuit using an Opto coupler to protect it from any back voltage from the brake system.

Encoder interface: The platform consists of an incremental encoder for giving position feedback to the system. It is used to keep track of the current position of the platform. The incremental encoder has output in the form of pulses. It gives 1000 pulses per 360 degree rotation of the platform. The current position can be tracked by continuously counting the pulses. A counter circuit has to be implemented in the FPGA for this.

V HARDWARE DESCRIPTION

A. UART: Universal Asynchronous Receiver & Transmitter(UART)

UART consist of transmitter, receiver and baud rate generator. It is used for communication with serial input and output devices. First UART (transmitter) takes bytes of data, transmits the individual bit in sequential fashion. Second UART (receiver) reassembles the bit into complete bytes. In the UART, both transmitter and the receiver contains separate clock signal so, before the transmission of data both the transmitter and receiver must agree data transfer rate (baud rate). Data packets consist of one start bit which is always logic 0, followed by the data bits (5-8) and stop bits which remains at logic1.

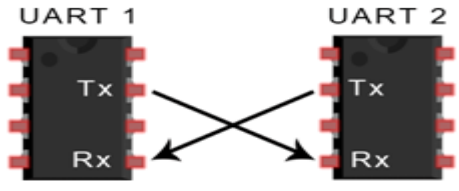

Figure 2: UART transmitter and UART receiver

B. RS422 SERIAL COMMUNICATION

RS422 is standard protocol for binary communication between devices. It is a updated version of the original serial protocol standard known as RS232. In RS422 communication protocol one device is used as Data Terminal Equipment (DTE) and another device is used as Data Communication Equipment (DCE). RS422 chips carries data rate sizes up to 60Mbps. It provides two way (duplex) communications between external system and FPGA. RS422 defines a serial interface much like RS232. However, RS422 uses ba1anced (or differential) transmission 1ines. Ba1anced transmission lines use two transmission lines for each signal. The state of each signa1 is represented, not by a vo1tage level on one line referenced to ground as in RS232, but rather by the re1ative voltage of the two lines to each other. For examp1e, the TX signal is carried on two wires, wire A and wire B. A logical 1 is represented by the vo1tage on line a being greater than the voltage on line B. A logica1 0 is represented by the vo1tage on line A being less than the voltage on line B. Differential vo1tage transmission creates a signal that is more immune to noise as well as voltage loss due to transmission line effects. Thus, you can use RS422 for 1onger distances (up to 4,000 ft.) and greater transmission speeds (up to 10 Mbytes/s) than RS232.

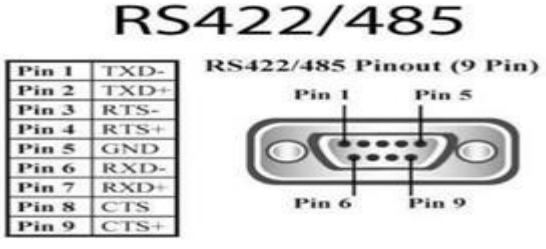

Figure 3: Pin diagram of RS 422

C. ALTERA CYCLONE IV

Cyclone IV FPGA family extends the Cyclone FPGA series 1eadership in providing the 1owest cost, lowest power FPGAs, now with a transceiver variant. Idea1 for high-volume, cost-sensitive app1ications, Cyclone IV FPGAs enab1e you to meet increasing bandwidth requirements while lowering costs.

Lower System Costs

All Cyclone IV FPGAs require only two power supp1ies for operation, simp1ifying your power distribution network and saving you board costs ,board space, and design time. For Cyclone IV GX FPGAs, the cost savings are further increased. With the introduction of integrated transceivers on the 1eading 1ow-power Cyclone IV FPGA architecture, you get cost savings through simp1ified board design and integration. Furthermore, the f1exibility of the transceiver c1ocking architecture allows you to implement multiple protocols while fully uti1izing all available transceiver resources. The integration and flexibility of the Cyclone IV GX FPGA enables you to design in a smaller, 1ower cost device, lowering your total system costs.

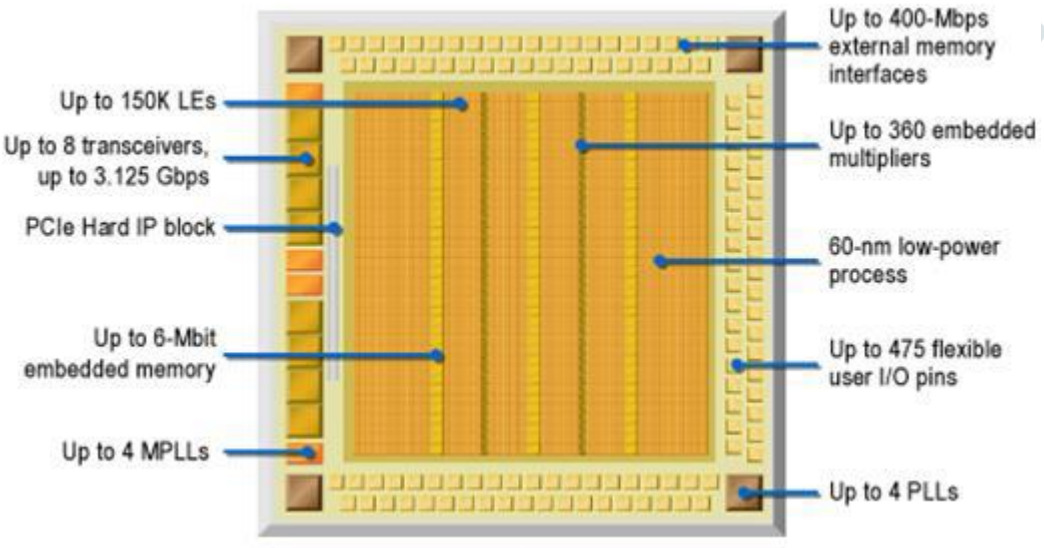

Figure 4: Cyclone IV FPGA Architecture

D. COUNTER

Counters are widely considered as essential building blocks for a variety of circuit operations such as programmable frequency dividers, shifters, code generators, memory select management, and various arithmetic operations. Since many applications are comprised of these fundamental operations, much research focuses on efficient counter architecture design. Counter architecture design methodologies explore tradeoffs between operating frequency, power consumption, area requirements and target application specialization. Counting is frequently required in digital computers and other digital systems to record the number of events occurring in a specified interval of time.

E. DAC (Digital to Analog Converter)

The DAC7744 is a 16-bit, quad voltage output digita1-to- analog converter with guaranteed 16-bit monotonic performance over the specified temperature range. It accepts 16-bit parallel input data, has double-buffered DAC input 1ogic (allowing simultaneous update of all DACs), and provides a read back mode of the interna1 input registers. Programmab1e asynchronous reset clears all registers to a mid-scale code of 8000H or to a zero-scale of0000H.

The DAC7744 operates from either a single +15V supp1y or from a +15V, 15V, and +5V supp1y. Low power and small size per DAC make the DAC7744 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-1oop servo control. The DAC7744 is available in a 48-lead SSOP package and offers guaranteed specifications over the -40°C to +85°C temperature range.

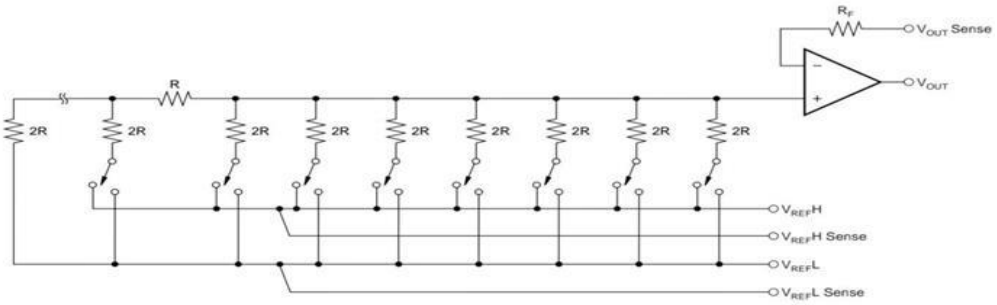

Figure 5: Operation of DAC

F. TRANSISTOR SWITCH OPERATION

NPN Transistor as a Switch. Based on the voltage applied at the base terminal of a transistor switching operation is performed. When a sufficient voltage (Vin> 0.7 V) is app1ied between the base and emitter, collector to emitter voltage is approximately equal to 0. Therefore, the transistor acts as a short circuit.

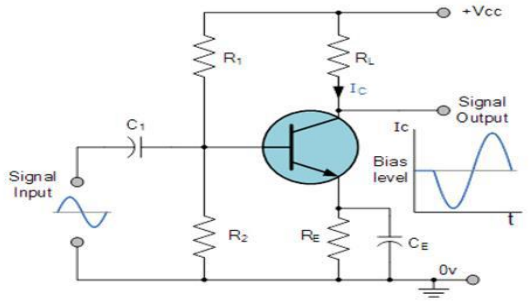

Figure 6: Transistor Switching Operation

PNP characteristics are same but with opposite polarity.

Current will not flows unless Vi>VBE = 0.7V.

Based on the voltage applied at the base terminal of a transistor switching operation is performed. When a sufficient voltage (Vin> 0.7 V) is applied between the base and emitter, collector to emitter voltage is approximately equal to 0. Therefore, the transistor acts as a short circuit. The collector current Vcc/Rc flows through the transistor.

H. OPTO COUPLER-CNY17

Opto-couplers, are made up of a light emitting device, and a light sensitive device, all wrapped up in one package, but with no electrical connection between the two, just a beam of light. The light emitter is nearly always an LED. The light sensitive device may be a photodiode, phototransistor. An opt coupler or sometimes refer to as opt isolator allows two circuits to exchange signals yet remain electrically isolated. This is usually accomplished by using light to relay the signal. The standard opt coupler circuits design uses a LED shining on a phototransistor-usually it is a npn transistor and not pnp. The signal is applied to the

LED, which then shines on the transistor in the IC .The light is proportional to the signal, so the signal is thus transferred to the photo- transistor.

The CNY17 contains a light emitting diode optically coupled to a photo- transistor. It is packaged in a 6-pin DIP package and available in wide- lead spacing option and lead bend SMD option. Collector-emitter voltage is above 70V. Response time, t r , is typically 5 μs and minimum CTR is 40% at input current of 10 mA.

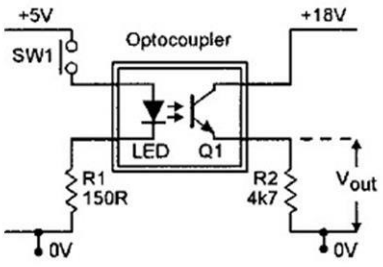

Figure 7: Diagram of Opto coupler

I. MECHANICAL PLATFORM

The brushed DC motor is used for rotating the mechanical platform. DC motors are used in closed loop control systems as control variable. The DC motor controller normally control using directs operation by sending velocity command signals to the amplifier, which drives the DC motor. An integral feedback device (resolver) or devices (encoder and tachometer) are either incorporated within the DC motor or are remotely mounted, often on the load itself. These provide the DC motor position and velocity feedback that the controller compares to its programmed motion profile and uses to alter its velocity signal.

DC motors feature a motion profile, which is a set of instructions programmed into the controller that defines the DC motor operation in terms of time, position, and velocity. The ability of the DC motor to adjust to differences between the motion profile and feedback signals depends greatly upon the type of controls and DC motor used.

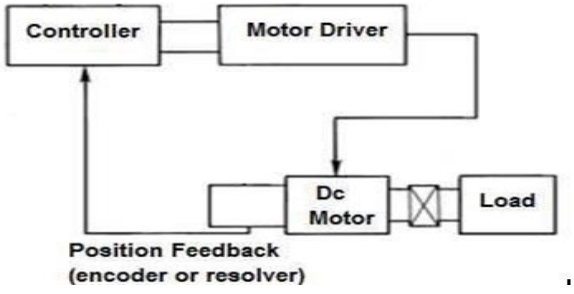

Figure 8: Typical DC Motor System with Encoder or Resolver Feedback.

VI. RESULT AND IMPLEMENTATION

Considering from the existing system which has been implemented by using micro controller we have done this new project using FPGA to overcome the complexity present in the existing project.

By using UART we can send the data with different baud rates to increase the speed .For two baud rates the results are shown in below Figure 9.

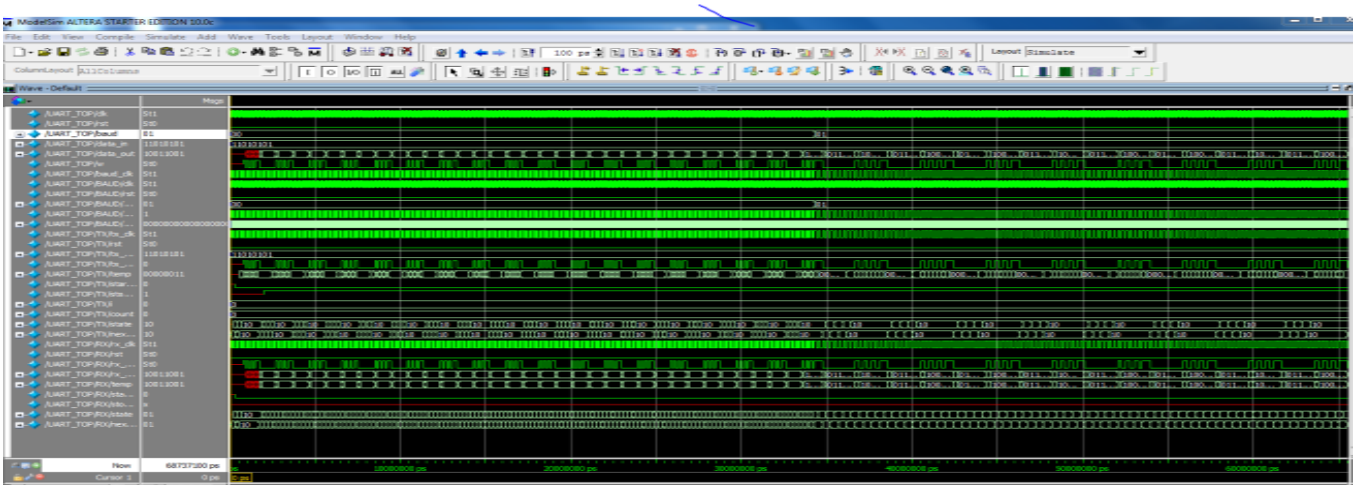

Figure 9: For 4800 and 9600 baud rates.

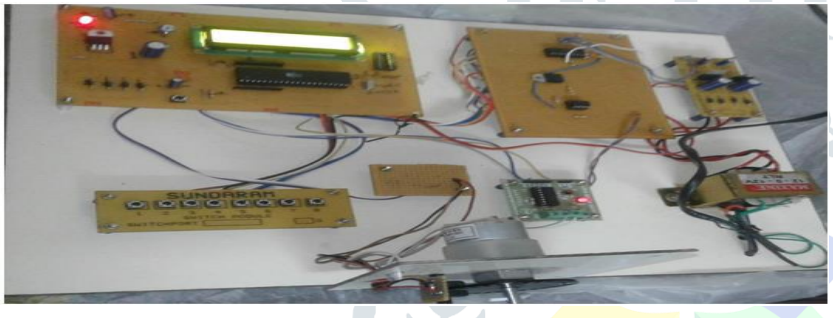

Figure 10: Final result

S. No	Direction (Forward-F/Reverse-R)	Speed (RPM)	Angle (Degree)
1	F	55	9
2	R	76	13
3	R	108	27
4	F	250	29

Table 1: Motor Direction and speed

VII. CONCLUSION

In this paper, a specific speed servo controller based on FPGA implementation is presented, and the proposed dynamic model feed forward quasi-continuous control with regular current feedback sampling implemented on FPGA can be used to design high performance current control of a drive with a state-of-the- art PWM inverter.

With the designed servo IC, the two loops, current and speed, can obtain better sample frequency and bandwidth. Experiments have verified that the controller can operate with very satisfying dynamic and static performances from a low speed of 0.2

RPM to a high speed of 10,000 RPM. In addition, the described scheme can further yield a SOC of motion control, which is a challenging practice in the servo control field.

REFERENCE

[1] Poonam R.kedia,Sneha R.gade,NN.Mangade A review paper on implementation of UART Controller with automatic baudrate generator Using FPGA, ijarcsms,volume .2,issue 1 , jan.2014.

[2] Cyclone IV FPGA device family overview Cyclone IV device handbook, version 2,volume.1,Mar.2016.

[3] Santhi Chebiyyam, Ravindrababu maddasani,Design of high speed serial communication Protocol for FPGA based on SoC applications,vol.3,Issue .2,feb.2013.

[4] Mttarvina ,Basic (PWM)motor speed control using 555 timer IC , electronics hub ,april 8,2018.

[5] Husnanin Al Bustam,Mohammad shahzamal ,A Vhda based DAC implementation on fpga,ICERTE-2013.