Performance Analysis of FTISEN in Faulty and Non-Faulty Conditions

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Abstract : Multistage Interconnection Networks (MINs) are most proficient interconnection networks (INs); they are broadly used in broadband switching technology and for multiprocessor systems. With the development of parallel processing, the MIN has turned into a hotspot of this field. The irregular MINs are more reliable and fault-tolerant networks which provide more disjoint paths, rerouting capabilities against faults. Fault tolerance is the critical issue of MINs. In this paper, a new fault-tolerant irregular MIN named Fault Tolerant Irregular Shuffle Exchange Network (FTISEN) is proposed. The FTISEN has full access capability and dynamic rerouting property under any switch failure. It provides better fault-tolerance by providing more paths between any source-destination pair as compared to existing MIN (Irregular Augmented Shuffle Exchange Network-4).

Keywords - **Multistage Interconnection Networks (MIN); rerouting; fault tolerance;**

I. INTRODUCTION

Fault-tolerance is the most dominant issue in the design of MINs for large-scale multiprocessor systems [2]. It is the ability to perform in presence of failure of components [3]. The proficiency of MINs is it organizes communication in connecting processors and memory modules. The MINs are a noteworthy class of indirect switching networks. The example of interconnection might be uniform or non-uniform that classifies the MINs to be regular, irregular and hybrid individually[12]. Full access property of MINs enables the request or data from any input to be transmitted to any output in one pass through the network.

The greater part of the dialog in MIN configuration is focused towards fault-tolerant capacity of the network. The essential thought for the adaptation to the internal failure of the MIN [4],[5],[6] is to make alternate paths between all source-destination pairs, with the goal that alternate paths can be utilized, when any switch gets failed/occupied.

The switch or link faults may cause the failure of MINs that ends in an unbalanced traffic load. To avoid this, high fault-tolerance and reliable MIN is needed. Several research works have been done to enhance the fault-tolerant ability of MIN with the sole objective of increasing the redundant (or alternate) and disjoint paths. Different MIN topologies and their structure, exchanging topology, and downsides are depicted in [8]. Disjoint paths [9] are repetitive ways that don't have any node (or switching element) in common other than the source and destination. Disjoint paths enhance the performance and reliability of MINs. While redundant (or alternate) paths are multiple paths between any source-destination pair [9].

To avoid performance degradation and to route multiple communication tasks together, a network designer has to choose a suitable fault-tolerant and highly reliable MIN architecture [8]. To design a high fault-tolerant dynamic MIN, it is necessary to:
   (i) provide more disjoint paths
   (ii) provide an effective dynamic rerouting algorithm
   (iii) have fault tolerance towards switching elements (SEs) failures
   (iv) decrease collision rate with the help of routing and rerouting strategy
   (v) have effective use of accessibility paths.
   (vi) have an architecture that is highly reliable and fault tolerant [8]
According to the reported researches and literature there is very limited fault tolerance comparison works of irregular MINs architecture [1][8][9][10][11][12][13].

In this paper, we are focusing on existing irregular MIN named as Irregular Augmented Shuffle Exchange Network-4 (IASEN-4). The main drawback of IASEN-4 is less alternate paths between any source-destination pair with less accessibility [1] in non-faulty (when there is no faulty node in each stage) and faulty (when a faulty node exists in one or more stages) cases. Therefore, we proposed Fault Tolerant Irregular Shuffle Exchange Network (FTISEN) to resolve this issue. FTISEN is more fault tolerant and it provides more alternate paths in faulty and non-faulty cases.

This paper addresses the issue of fault-tolerance and improves the performance of the proposed network by reducing the count of stages and appending direct links in the proposed new irregular fault-tolerant FTISEN. The structure of the existing Irregular Augmented Shuffle Exchange Network-4 (IASEN-4) [1] is mentioned in Section 2. Section 3 exhibits the structure, redundancy graph and routing scheme of the proposed MIN. Performance evaluation parameters of existing and proposed MINs are discussed in section 4. Results and comparison analysis of the proposed MIN with existing MIN is presented in section 5. Finally, section 6 summarizes the conclusion of the paper.

II. STRUCTURE OF THE EXISTING NETWORK

In this paper, the structure of existing IASEN-4 is discussed below.

Irregular Augmented Shuffle Exchange Network-4 (IASEN-4)

The IASEN-4 [1] is an irregular multistage interconnection with N×N size and ($\log_2 N/2$) number of stages. The stage 0 and last stages consist of N/2 switching elements (SE) while each middle stage consists of the (N/4) number of SEs. The IASEN-4 has N sources and N destinations, which are associated, with N multiplexers (MUX) and N demultiplexers (DEMUX) respectively. The

size of each SE of stage 0, middle stage and last stage is 2×3, 4×2, and 2×2 respectively. The size of each multiplexer (MUX) and demultiplexer (DEMUX) is 4×1 and 1×4 respectively. In the first stage, each switching element (SE) is attached with two multiplexers of size 4x1 and in the last stage; two demultiplexers of size 1x4 are connected with each SE. The 16x16 network size IASEN-4 is mentioned in Figure 1[1].
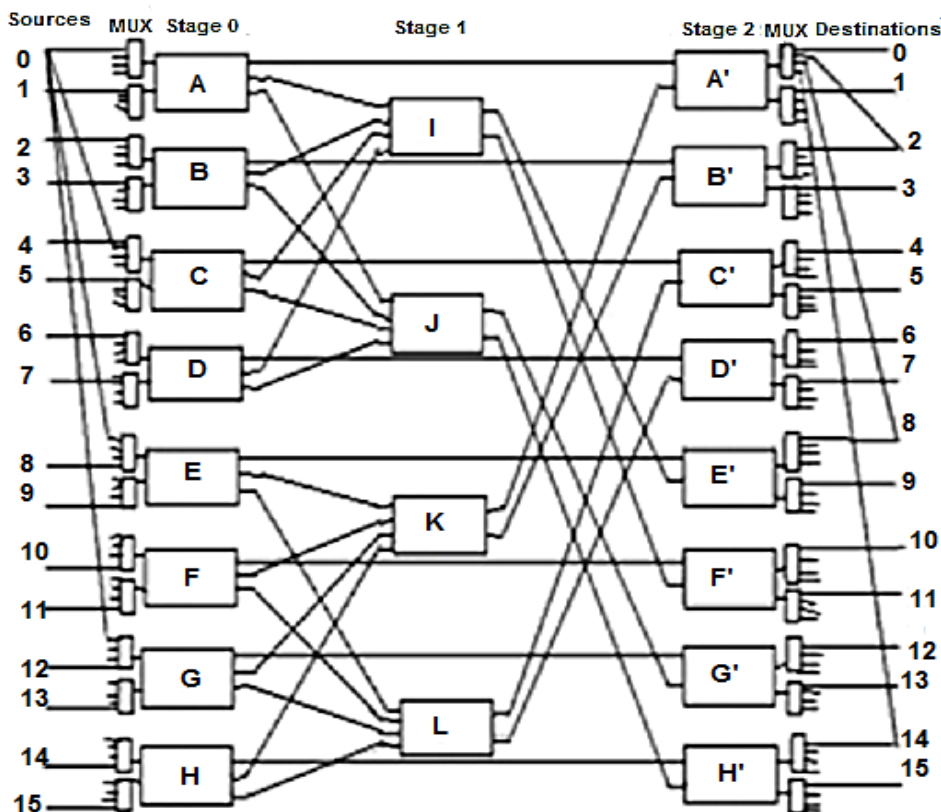

Figure 1. Irregular Augmented Shuffle Exchange Network-4 (IASEN-4) [1]

Before moving to next section, let us have a look on the symbols which are used throughout the paper. Table I demonstrates the different symbols and their significance which are used in the paper.

Table I: Symbols with their meanings

Symbol	Meaning	Symbol	Meaning
PSE_0	Primary SE of stage 0	D_n	Number of destinations
FSE_0	First alternate SE of stage 0	S_t	Number of stages
SSE_0	Second alternate SE of stage 0	$BW_{IASEN-4}$	Bandwidth of IASEN-4
TSE_0	Third alternate SE of stage 0	BW_{FTISEN}	Bandwidth of FTISEN
PSE_1	Primary SE of stage 1	$PA_{IASEN-4}$	Probability of acceptance of IASEN-4
FSE_1	First alternate SE of stage 1	PA_{FTISEN}	Probability of acceptance of FTISEN
SSE_1	Second alternate SE of stage 1	$TP_{IASEN-4}$	Throughput of IASEN-4 in non-faulty condition
TSE_1	Third alternate SE of stage 1	$TP_{IASEN-4\_SF}$	Throughput of IASEN-4 in single fault condition
PSE_2	Primary SE of stage 2	TP_{FTISEN}	Throughput of FTISEN in non-faulty condition
FSE_2	First alternate SE of stage 2	TP_{FTISEN_SF}	Throughput of FTISEN in single fault condition
PSE_k	Primary SE of stage k where k=2 to (n-3), when n>4	$PU_{IASEN-4}$	Processor Utilization of IASEN-4 in non-faulty condition
FSE_k	First alternate SE of stage k where k=2 to (n-3), when n>4	$PU_{IASEN-4\_SF}$	Processor Utilization of IASEN-4 in single fault condition
$PSE_{(n-2)}$	Primary SE of stage (n-2)	PU_{FTISEN}	Processor Utilization of FTISEN in non-faulty condition
$FSE_{(n-2)}$	First alternate SE of stage (n-2)	PU_{FTISEN_SF}	Processor Utilization of FTISEN in single fault condition
T_{NF}	Data Transmission Time in non-faulty	$PP_{IASEN-4}$	Processing Power of IASEN-4 in non-faulty

	condition		condition
T_{SF}	Data Transmission Time in faulty condition	$PP_{IASEN-4\_SF}$	Processing Power of IASEN-4 in single fault condition
N_n	Number of nodes including source and destination	PP_{FTISEN}	Processing Power of FTISEN in non-faulty condition
T_r	Routing Time between two nodes (either SE or source or destination)	PP_{FTISEN_SF}	Processing Power of FTISEN in single fault condition
N_{dp}	Total number of generated data packets on a source node		

III. PROPOSED MULTISTAGE INTERCONNECTION NETWORK: FTISEN

3.1 Structure of Proposed Multistage Interconnection Network

The Fault Tolerant Irregular Shuffle Exchange Network (FTISEN) is a modified IASEN-4 with N×N network size. FTISEN has N sources and N destinations, which are connected, with N MUX and N DEMUX respectively. It is an irregular MIN having [(log$_2$N)-1] number of stages. These stages have range from 0 to (n-2), where n= log$_2$N. Stage 0 and last stage consist of (N/2) number of SEs. The number of middle stages (m) is (n-3). Each middle stage (m) consists of N/4 number of switching elements. A 16x16 network size FTISEN is mentioned in Figure 2.
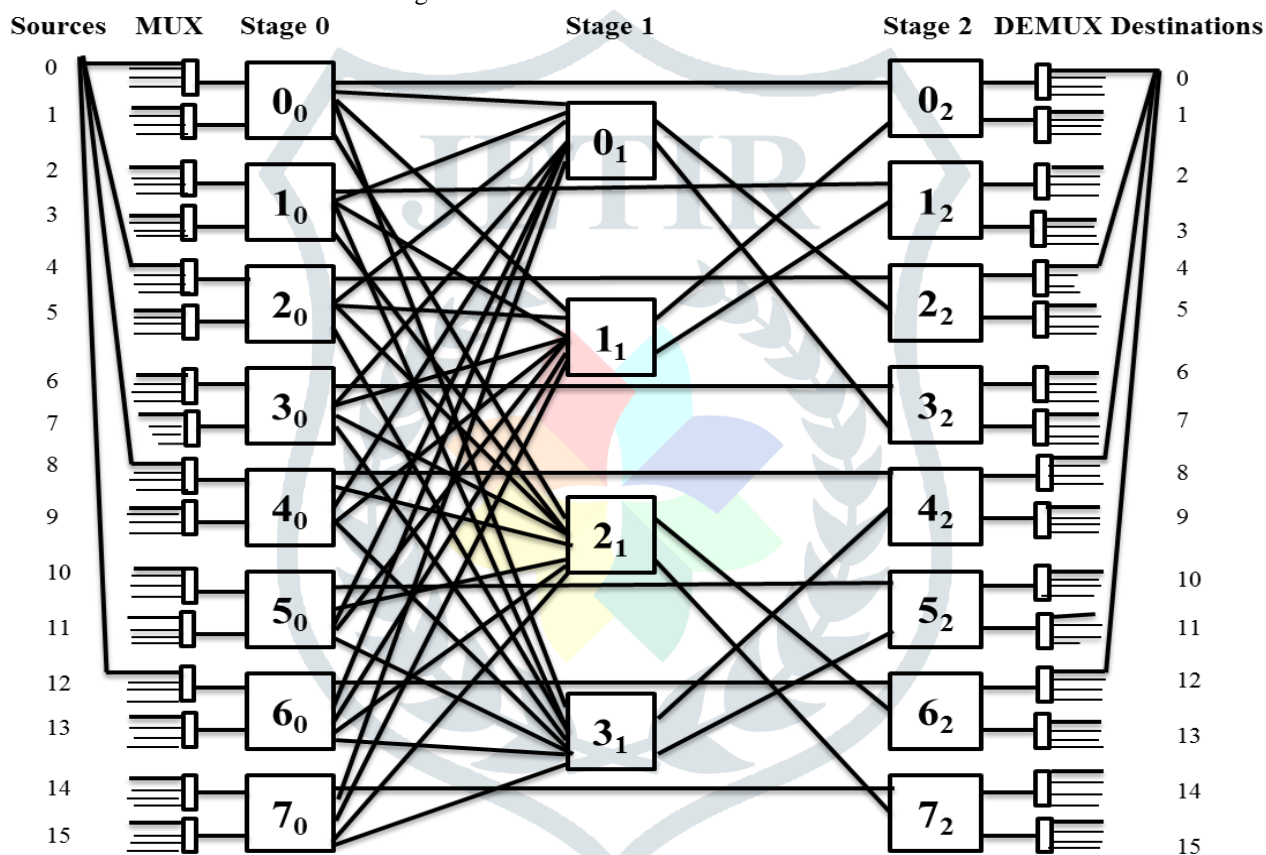

Figure 2. Fault Tolerant Irregular Shuffle Exchange Network (FTISEN)

The SE of first and last stage is represented as j_0 and $j_{(n-2)}$ respectively where, j=0,2,..(N/2-1). The SEs of middle stages (m) are represented as k_m, where k=0 to ((N/4)-1). The size of each SE in the stage 0, stage 1 and stages (2 to (n-2)) is 2×5, 8×2, and 2×2 respectively.

Each MUX and DEMUX has size 4×1 and 1×4 respectively. Each SE of first stage is associated with two multiplexers while the two demultiplexers are associated with each SE in last stage.

FTISEN is a dynamically re-routable irregular MIN, which provides multiple paths of varying lengths between a given source to given destination. The Link connection pattern from source to destination is as follows:

(1) Link Connections at Source:

Each source is connected with four multiplexers (MUX) as follows:
    (i) For each source S_i, where i=0 to ((N/4)-1)
(a) First link connects to MUX (i)
(b) Second link connects to MUX (i+(N/4))
(c) Third link connects to MUX (i+(N/2))
(d) Fourth link connects to MUX (i+(3N/4))

    (ii) For each source S_i where i=(N/4) to((N/2)-1)
(a) First link connects to MUX (i)
(b) Second link connects to MUX (i+(N/4))
(c) Third link connects to MUX (i+(N/2))

(d) Fourth link connects to MUX $(i-(N/4))$

(iii) For each source S_i where $i=N/2$ to $((3N/4)-1)$
(a) First link connects to MUX (i)
(b) Second link connects to MUX $(i+(N/4))$
(c) Third link connects to MUX $(i-(N/2))$
(d) Fourth link connects to MUX $(i-(N/4))$

(iv) For each source S_i where $i=(3N/4)$ to $(N-1)$
(a) First link connects to MUX (i)
(b) Second link connects to MUX $(i-(3N/4))$
(c) Third link connects to MUX $(i-(N/2))$
(d) Fourth link connects to MUX $(i-(N/4))$

(2) Link Connections at Multiplexers:
The FTISEN consists of N number of multiplexers (MUX) with size 4×1, range from 0 to $(N-1)$. Each switch j_0, where $j=0$ to $N/2-1$, in stage 0 is connected with two MUX with following steps:
(a) First link connects to MUX $(2j)$
(b) Second link connects to MUX $(2j+1)$

(3) Link Connections at stage 0:
Each SE in the stage 0 is connected with four SEs of stage 1. We assume that the total number SEs in stage 0 are divided into $N/16$ groups (P_q), where $q=0$ to $(N/16)-1$. Each group (P_q) consists of 8 SEs. Each SE of group (P_q) has 5 output links. Their output connection links are as follows:
The SE j_0 of stage 0 is connected with 5 output links:
(a) First link connects to SE j_{n-2} of last stage
(b) Second link connects to SE $(4q)_1$ of stage 1
(c) Third link connects to SE $(4q+1)_1$ of stage 1
(d) Fourth link connects to SE $(4q+2)_1$ of stage 1
(e) Fifth link connects to SE $(4q+3)_1$ of stage 1

(4) Link Connections from Middle stages:
On the basis of network size, we considered two cases for output link connections of middle stages:
(1) When Network size $N=16$, and
(2) When Network size $N > 16$
 Case 1 In first case when network size $N=16$, then there is only one middle stage (m). There are $N/4$ switches in stage 1. It is assumed that there are $N/8$ groups (P_r) in the stage 1, where $r=0$ to $(N/8-1)$. Each group consists of two switching elements. Each switching element (SE) of group (P_r) has two output links. These output connection links are as follows:

(i) The SE $(k=2r)_1$ of stage 1 has 2 output links:
(a) First link connects to SE $(4r+2)_{m+1}$ of last stage
(b) Second link connects to switch $(4r+3)_{m+1}$ of last stage

(ii) Switch $(k=2r+1)_1$ of stage 1 has 2 output links:
(a) First link connects to switch $(4r)_{m+1}$ of last stage
(b) Second link connects to switch $(4r+1)_{m+1}$ of last stage

 Case 2 In second case when network size $N>16$, then there are $(n-3)$ number of middle stages (m), ranges from $m=1$ to $(n-3)$. It is assumed that there are $N/8$ number of groups (P_r) of switches in each middle stage, where $r=0$ to $(N/8-1)$. In addition, each group (P_r) consists of two switches named as $2r$ and $(2r+1)$, where $r=0$ to $(N/8-1)$. There are two steps for the link connections of switches in stages $(m=1$ to $(n-4))$ are as follows:

A. In first step, there are $m=1$ to $(n-4)$ number of middle stages are considered except last middle stage. There are $N/8$ groups (P_r) in the stage 2, where $r=0$ to $(N/8-1)$. Each group consists of two switching elements. Each switching element (SE) of each group (P_r) has two output links. So the output link connections for SE k_m in stage m can be determined as:

(i) The SE $(k=2r)_m$ of stage 1 has 2 output links:

(a) First link connects to SE $(2r)_{m+1}$ of stage 2
(b) Second link connects to SE $(2r+1)_{m+1}$ of stage 2
(ii) The SE $(k=2r+1)_1$ of stage 1 has 2 output links:

(a) First link connects to switch $(2r)_{m+1}$ of stage $(m+1)$
(b) Second link connects to switch $(2r+1)_{m+1}$ of stage $(m+1)$

B. In second step, only last middle stage $(m=n-3)$ is considered. There are $N/4$ switching elements (SE) in the stage $(n-3)$. It is assumed that there are $N/8$ groups (P_r) in the stage $(n-3)$, where $r=0$ to $(N/8-1)$. Each group consists of two switching elements. Each switching element (SE) of group (P_r) has two output links. These output connection links are as follows:

(i) The SE $(k=2r)_m$ of stage 1 has 2 output links:
(a) First link connects to SE $(4r+2)_{m+1}$ of last stage
(b) Second link connects to switch $(4r+3)_{m+1}$ of last stage

(ii) Switch $(k=2r+1)_m$ of stage 1 has 2 output links:
(a) First link connects to switch $(4r)_{m+1}$ of last stage
(b) Second link connects to switch $(4r+1)_{m+1}$ of last stage

(5) Link Connections at last stage (n-1):
The last stage (n-1) consists of N/2 number of SEs. Each SE j_{n-1} has 2 output links, where the range of j=0 to (N/2-1). Therefore, the output link connections of each SE j_{n-1} of last stage are as follows:
(a) First link connects to DEMUX (2j)
(b) Second link connects to DEMUX (2j+1)

(6) Link Connections at Demultiplexer:
The link connections at DEMUX consist of following steps:

(i) Each destination D_i is connected with four DEMUX, where i=0 to ((N/4)-1)
(a) First link connects to DEMUX (i)
(b)Second link connects to DEMUX(i+(N/4))
(c)Third link connects to DEMUX(i+(N/2))
(d)Fourth link connects to DEMUX (i+(3N/4))

(ii) Each destination D_i is connected with four DEMUX, where i=(N/4) to ((N/2)-1)
(a) First link connects to DEMUX (i)
(b)Second link connects to DEMUX (i+(N/4))
(c) Third link connects to DEMUX(i+(N/2))
(d) Fourth link connects to DEMUX (i-(N/4))

(iii) Each destination D_i is connected with four DEMUX, where i=N/2 to ((3N/4)-1)
(a) First link connects to DEMUX (i)
(b)Second link connects to DEMUX (i+(N/4))
(c)Third link connects to DEMUX(i-(N/2))
(d) Fourth link connects to DEMUX (i-(N/4))

(iv) Each destination D_i is connected with four DEMUX, where i=(3N/4) to (N-1)
(a)First link connects to DEMUX (i)
(b)Second link connects to DEMUX (i-(3N/4))
(c) Third link connects to DEMUX (i-(N/2))
(d) Fourth link connects to DEMUX (i-(N/4))

3.2 Redundancy Graph

A redundancy graph gives a helpful approach to consider the properties of multipath MIN, for example, the number of faults tolerated or the sort of rerouting conceivable. A redundancy graph describes all the accessible paths between a source and a destination in a MIN. It includes two recognized nodes– the source S_i and the destination D_i and whatever remains of nodes related to the switches that lie along the paths amongst S_i and D_i. In FTISEN, the redundancy graph shows multipath between source and destination, as shown in Figure 3.
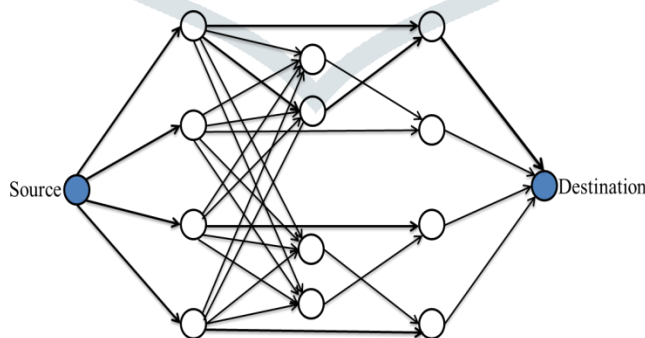

Figure 3. Redundancy graph of FTISEN

Example: The all possible paths between source 0 and destination 5 are as follows:

$$0 \rightarrow MUX(0) \rightarrow 0_0 \rightarrow 0_2 \rightarrow DEMUX(1) \rightarrow 5$$
$$0 \rightarrow MUX(0) \rightarrow 0_0 \rightarrow 0_1 \rightarrow 2_2 \rightarrow DEMUX(5) \rightarrow 5$$
$$0 \rightarrow MUX(0) \rightarrow 0_0 \rightarrow 1_1 \rightarrow 0_2 \rightarrow DEMUX(1) \rightarrow 5$$
$$0 \rightarrow MUX(0) \rightarrow 0_0 \rightarrow 2_1 \rightarrow 6_2 \rightarrow DEMUX(13) \rightarrow 5$$
$$0 \rightarrow MUX(0) \rightarrow 0_0 \rightarrow 3_1 \rightarrow 4_2 \rightarrow DEMUX(9) \rightarrow 5$$
$$0 \rightarrow MUX(4) \rightarrow 2_0 \rightarrow 2_2 \rightarrow DEMUX(5) \rightarrow 5$$
$$0 \rightarrow MUX(4) \rightarrow 2_0 \rightarrow 0_1 \rightarrow 2_2 \rightarrow DEMUX(5) \rightarrow 5$$
$$0 \rightarrow MUX(4) \rightarrow 2_0 \rightarrow 1_1 \rightarrow 0_2 \rightarrow DEMUX(1) \rightarrow 5$$

$0 \rightarrow MUX(4) \rightarrow 2_0 \rightarrow 2_1 \rightarrow 6_2 \rightarrow DEMUX(13) \rightarrow 5$
$0 \rightarrow MUX(4) \rightarrow 2_0 \rightarrow 3_1 \rightarrow 4_2 \rightarrow DEMUX(9) \rightarrow 5$
$0 \rightarrow MUX(8) \rightarrow 4_0 \rightarrow 4_2 \rightarrow DEMUX(9) \rightarrow 5$
$0 \rightarrow MUX(8) \rightarrow 4_0 \rightarrow 0_1 \rightarrow 2_2 \rightarrow DEMUX(5) \rightarrow 5$
$0 \rightarrow MUX(8) \rightarrow 4_0 \rightarrow 1_1 \rightarrow 0_2 \rightarrow DEMUX(1) \rightarrow 5$
$0 \rightarrow MUX(8) \rightarrow 4_0 \rightarrow 2_1 \rightarrow 6_2 \rightarrow DEMUX(13) \rightarrow 5$
$0 \rightarrow MUX(8) \rightarrow 4_0 \rightarrow 3_1 \rightarrow 4_2 \rightarrow DEMUX(9) \rightarrow 5$
$0 \rightarrow MUX(12) \rightarrow 6_0 \rightarrow 6_2 \rightarrow DEMUX(13) \rightarrow 5$
$0 \rightarrow MUX(12) \rightarrow 6_0 \rightarrow 0_1 \rightarrow 2_2 \rightarrow DEMUX(5) \rightarrow 5$
$0 \rightarrow MUX(12) \rightarrow 6_0 \rightarrow 1_1 \rightarrow 0_2 \rightarrow DEMUX(1) \rightarrow 5$
$0 \rightarrow MUX(12) \rightarrow 6_0 \rightarrow 2_1 \rightarrow 6_2 \rightarrow DEMUX(13) \rightarrow 5$
$0 \rightarrow MUX(12) \rightarrow 6_0 \rightarrow 3_1 \rightarrow 4_2 \rightarrow DEMUX(9) \rightarrow 5$

There are twenty possible paths between source 0 and destination 5 in FTISEN when there is no faulty switch in each stage but in IASEN-4 only ten paths are possible.

3.3 Routing Algorithm

The routing scheme of FTISEN for the situation is that each source-destination pair tries to use just a single path at any given time. The dynamic rerouting scheme given beneath is simple to execute and performs quite well. This scheme expect that sources and switches can identify faults in the switches to which they are associated. In case of any fault, instead of reinitializing request, dynamic re-routing scheme has been used to find an alternate path from the current stage. In routing of FTISEN, first step is to obtain the source address and its corresponding destination address. Let S_i and D_i are the source and destination addresses respectively. Let binary representation of the source S_i and destination D_i is as follows:

$S_i = s_0, s_1, \ldots, s_{n-2}, s_{n-1}$,
$D_i = d_0, d_1, \ldots, d_{n-2}, d_{n-1}$,   where i=0 to N-1

Each source is associated to two switches (primary and secondary) in a subnetwork (G_a). A source selects a particular subnetwork (G_a) based upon the MSB (most significant bit) of destination address D (i.e. $a=d_0$) and attempts an entry into the FTISEN via its primary path. If primary path is faulty (i.e. MUX or switch or both are faulty), then request is routed via secondary path. For example, switch 0_0 is the primary SE (PSE_0) and 2_0 is first alternate SE (FSE_0) in subnetwork G_0 via its primary and secondary path respectively for source 0. Switches 4_0 is the second alternate SE (SSE_0) via its primary path and switch 6_0 is the third alternate SE (TSE_0) via its secondary path in subnetwork G_1 for source 0. If both paths (primary and secondary) are faulty then request is routed to other subnetwork. If both (primary and secondary) paths of other subnetwork are still faulty. Then drop the request otherwise forward the request to the SE of next stage.

Two algorithms are proposed in FTISEN. Algorithm 2 is part of algorithm 1. In algorithm 1, if the binary bits of source and destination address are same and if the applicable SE of stage 0 (SE_0) and SE of last stage (SE_L) are not faulty. Then request is directly forwarded to the given destination via DEMUX from given source.

Algorithm 1:Routing_ FTISEN

```
BEGIN
If (Si and Di are same)
{
        if (SE0 and SEL are not faulty)
        {
            Send request from SE0 to SEL;
        }
        else
        {
            Algorithm 2;
        }
}
else
{
        Algorithm 2;
}
End
```

Algorithm 2: Routing_ FTISEN

```
At Stage 0:
if PSE0==FB          //FB means busy or faulty node
        then FSE0
        else if FSE0==FB
            then SSE0
        else if SSE0==FB
           then TSE0
        else if  TSE0==FB
```

```
                    then drop the request
else Send Request to PSE₁


At Stage 1:
if PSE₁== FB
            then FSE₁
            else if FSE₁== FB
            then SSE₁
            else if SSE₁ == FB
            then Send Request to TSE₁
            else if TSE₁== FB
            then Drop the Request
else Send Request to PSE₂


for (Stage k=2 to (n-3)     // Execute only when n> 4, where n=log₂N
    At Stage k:
    if PSEₖ== FB
            then FSEₖ
            else if FSEₖ== FB
            then Drop the Request
    else Send Request to PSEₖ₊₁ of Stage k+1


At Stage (n-2):
if PSE₍ₙ₋₂₎== FB
            then Drop the Request
Send Request to the given destination
```

IV. PERFORMANCE EVALUATION PARAMETERS OF FTISEN AND IASEN-4

This performance analysis [13] of existing MIN IASEN-4 [1] and proposed MIN FTISEN for network size 16×16 is calculated with the help of different performance evaluation parameters such as the probability of acceptance, bandwidth, throughput, processor utilization and processing power [13] and their comparison is also performed in faulty (or single switch fault) and non-faulty conditions. The simulation is performed in MATLAB version 8.5.0.197613. The performance evaluation parameters which are used in order to measure the performance of network are as follows:

4.1 Request Generation Probability

Request Generation Probability (p) or Load Factor is the quantity of data packets created on a source node and these packets can be transmitted to the destinations over MINs[9-11].The estimation of p is thought to be 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, and 1.

Let the request generation probability for each $\alpha \times \beta$ SE is p, where 'α' and 'β' are inputs and outputs of a SE respectively. Thus, general probability equation is as follows:

"Probability [9-11] of one output receiving the request from "α' inputs is:

$$1 - (1 - (p/\beta))^{\alpha} \qquad (1)$$

The probability equations of IASEN-4:

$$p_0 = 1 - (1 - (p/3))^2 \qquad (2)$$
$$p_1 = 1 - (1 - (p_0/2))^4 \qquad (3)$$
$$p_2 = 1 - \{(1-p_1)\times(1-(p_0/2))\}^2 \qquad (4)$$

The probability equations of FTISEN:

$$p_0 = 1 - (1 - (p/5))^2 \qquad (5)$$
$$p_1 = 1 - (1 - (p_0/2))^8 \qquad (6)$$
$$p_2 = 1 - \{(1-p_1)\times(1-(p_0/2))\}^2 \qquad (7)$$

4.2 Data Transmission Time

It is time that all produced data packets (or requests) take from source to the given number of destinations [12]. It can be measured in faulty and non-faulty network environments. Let the representation of data transmission time in non-faulty and faulty network conditions is T_{NF} and T_{SF} respectively.

If network is non-faulty, then it is given as follows:

$$T_{NF} = (N_n - 1) \times T_r \times N_{dp} \times D_n \qquad (8)$$

If network has single switch fault, then it is given as follows:

$$T_{SF} = T_{NF} + (S_t \times T_r) \qquad (9)$$

Where,

N_n = Number of nodes including source and destination

T_r = Routing Time between two nodes (either SE or source or destination)

D_n = Number of destinations

S_t = Number of stages

N_{dp} = Total number of generated data packets on a source node

In non-faulty case, the data packets (or requests) takes the shortest path from source to destination and let the routing time (T_r) between two nodes is 0.01ms. In faulty case, the data packets are dynamically rerouted from faulty to most suitable non-faulty node. Subsequently, these data packets (or requests) can be transmitted to the given destination. In faulty cases, we have expected that a data packet (or request) takes 0.02 ms routing time (T_r) in its rerouting method.

4.3 Bandwidth (BW)

The mean number of active memory module in a transfer cycle is known as bandwidth of network [9-11].

For S_n sources and D_n destinations, the bandwidth is calculated as follows:

$$BW = D_n \times p_{n-1} \qquad (10)$$

Now, BW of IASEN-4 and FTISEN are given by the following formulas:

$$BW_{IASEN-4} = (D_n \times p_{n-1}) \qquad (11)$$
$$BW_{FTISEN} = (D_n \times p_{n-1}) \qquad (12)$$

Where, p_{n-1} is the expected of requests on $\alpha \times \beta$ output line SE at $(n-1)^{th}$ stage

4.4 Probability of Acceptance(PA)

In data transmission, the switch failure, link failure or any other cause can block some data packets (or request) from source to destination node. That's why the total number of requests accepted by the destination and total number of requests sent by the source in a transfer cycle will not be same [9][10][11]. Therefore, "the number of requests accepted by the destination node which are sent by source node in a transfer cycle is known as probability of acceptance".

It is calculated as follows:

$$PA = BW/(D_n \times p) \qquad (13)$$

Now, PA of IASEN-4 and FTISEN are given by the following formulas:

$$PA_{IASEN-4} = BW_{IASEN-4}/(D_n \times p) \qquad (14)$$
$$PA_{FTISEN} = BW_{FTISEN}/(D_n \times p) \qquad (15)$$

4.5 Throughput (TP)

The average number of data packets (or request) delivered to a destination in a transfer cycle is called throughput [9-11].

$$TP = (BW/N \times T) \qquad (16)$$

Where, T is the data transmission time in ms.

In non-faulty case, the TP of IASEN-4 and FTISEN are given by the following formulas:

$$TP_{IASEN-4} = BW_{IASEN-4}/(N \times T_{NF}) \qquad (17)$$

$$TP_{FTISEN} = BW_{FTISEN}/(N \times T_{NF}) \qquad (18)$$

In single switch fault case, the TP of IASEN-4 and FTISEN are given by the following formulas:

$$TP_{IASEN-4-SF} = BW_{IASEN-4}/(N \times T_{SF}) \qquad (19)$$

$$TP_{FTISEN-SF} = BW_{FTISEN}/(N \times T_{SF}) \qquad (20)$$

4.6 Processor Utilization (PU)

When data packets are transmitted from a given source to destination, then the processor takes a specific amount of time to make this computation fast and efficient for each transfer cycle [9][10][11][12][13]. So the time taken by the processor for each transfer cycle is known as utilization time of the processor.

In other words, the percentage of time the processor is active doing computation without accessing the global memory is called processor utilization [9-11].

$$PU = BW/(N \times p \times T) \qquad (21)$$

In non-faulty case, the PU of IASEN-4 and FTISEN are given by the following formulas:

$$PU_{IASEN-4} = BW_{IASEN-4}/(N \times p \times T_{NF}) \qquad (22)$$
$$PU_{FTISEN} = BW_{FTISEN}/(N \times p \times T_{NF}) \qquad (23)$$

In single switch fault case, the PU of IASEN-4 and FTISEN are given by the following formulas:

$$PU_{IASEN-4-SF} = BW_{IASEN-4}/(N \times p \times T_{SF}) \qquad (24)$$
$$PU_{FTISEN-SF} = BW_{FTISEN}/(N \times p \times T_{SF}) \qquad (25)$$

4.7 Processing Power (PP)

The sum of processor utilization over the number of processors is called processing power [9-11].

$$PP = (N \times PU) \qquad (26)$$

In non-faulty case, the PP of IASEN-4 and FTISEN is given by the following formulas:

$$PP_{IASEN-4} = (N \times PU_{IASEN-4}) \qquad\qquad (27)$$
$$PP_{FTISEN} = (N \times PU_{FTISEN}) \qquad\qquad (28)$$

In single switch fault case, the PP of IASEN-4 and FTISEN is given by the following formulas:

$$PP_{IASEN-4-SF} = (N \times PU_{IASEN-4-SF}) \qquad\qquad (29)$$

$$PP_{FTISEN-SF} = (N \times PU_{FTISEN-SF}) \qquad\qquad (30)$$

V. PERFORMANCE ANALYSIS AND RESULT

To evaluate the performance of FTISEN and IASEN-4, the we have simulated the above formulas in MATLAB 8.5.0.197613. The performance parameters (bandwidth, probability of acceptance, throughput, processor utilization and processing power) of FTISEN and IASEN-4 are compared and analyzed here. In non-faulty case, the data packets (or requests) takes minimum path from source to destination and let the routing time (T_r) between two nodes (either source or destination or SE) is 0.01ms. In faulty (single switch fault) case, the data packets are dynamically rerouted from faulty to most suitable non-faulty node. Subsequently, these data packets (or requests) can be transmitted to the given destination. In faulty cases, we have expected that a data packet (or request) takes 0.02 ms routing time (T_r) in its rerouting method. The values of performance parameters for FTISEN and IASEN-4 have been shown in following table II and table III.

Table 2 Performance Parameters of FTISEN

p	BW_{FTISEN}	PA_{FTISEN}	TP_{FTISEN}	TP_{FTISEN_SF}	PU_{FTISEN}	PU_{FTISEN_SF}	PP_{FTISEN}	PP_{FTISEN_SF}
0.1	4.8369	3.0231	0.47235	0.45120	4.72354	4.51204	75.5767	72.1926
0.2	8.2104	2.5658	0.80179	0.76589	4.00899	3.829488	64.1439	61.2718
0.3	10.5628	2.2006	1.03152	0.98534	3.43841	3.284449	55.0145	52.5512
0.4	12.2029	1.9067	1.19169	1.13834	2.97924	2.845841	47.6678	45.5335
0.5	13.3467	1.6683	1.30338	1.24502	2.60677	2.490047	41.7083	39.8408
0.6	14.1443	1.4734	1.38128	1.31943	2.30213	2.199052	36.8341	35.1848
0.7	14.7008	1.3126	1.43563	1.37135	2.05089	1.959065	32.8143	31.3450
0.8	15.0893	1.1789	1.47357	1.40759	1.84196	1.759481	29.4713	28.1517
0.9	15.3607	1.0667	1.50007	1.43290	1.66674	1.592113	26.6679	25.4738
1	15.5505	0.9719	1.5186	1.45060	1.5186	1.450603	24.2976	23.2096

Table 3 Performance Parameters of IASEN-4

| p	BW_{FTISEN}	PA_{FTISEN}	TP_{FTISEN}	TP_{FTISEN_SF}	PU_{FTISEN}	PU_{FTISEN_SF}	PP_{FTISEN}	PP_{FTISEN_SF}
0.1	4.53477	2.83423	0.4428	0.42302	4.4285	4.230199	70.8558	67.68318
0.2	7.78106	2.43158	0.7599	0.725845	3.79935	3.629226	60.7895	58.06761
0.3	10.10334	2.10486	0.9867	0.942476	3.28885	3.141587	52.6216	50.26539
0.4	11.76399	1.83812	1.1488	1.097387	2.8721	2.743468	45.9531	43.89548
0.5	12.95145	1.61893	1.2648	1.208158	2.5296	2.416315	40.4733	38.66104
0.6	13.8008	1.4376	1.3477	1.287391	2.2462	2.145652	35.9397	34.33043
0.7	14.4088	1.2865	1.4071	1.344107	2.0101	1.920153	32.1626	30.72245
0.8	14.8445	1.1597	1.4497	1.384752	1.8121	1.73094	28.9932	27.69503
0.9	15.1573	1.0526	1.4802	1.413925	1.6447	1.571028	26.3147	25.13645
1	15.3822	0.9614	1.5022	1.434909	1.5022	1.434909	24.0347	22.95855
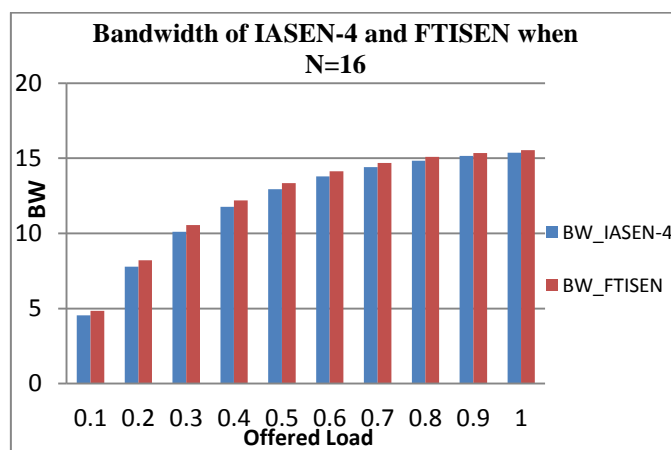
Figure 4. Bandwidth Comparison of IASEN-4 and FTISEN

Figure 4 shows that bandwidth of IASEN-4 is less as compared to FTISEN when the network size (N) is 16 in both (faulty and non-faulty) cases.
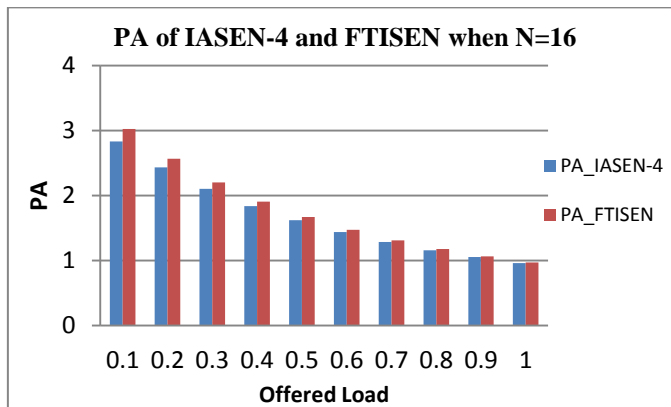

Figure 5. PA Comparison of IASEN-4 and FTISEN

Switch fault, link fault or any other causes are responsible for blockage of data packets during data transmission. That's why the total number of data packets accepted by a destination will not be equal to the total number of data packets generated at a source node in a transfer cycle [10]. Therefore, Figure 5 shows that probability of acceptance of FTISEN is greater than IASEN-4.
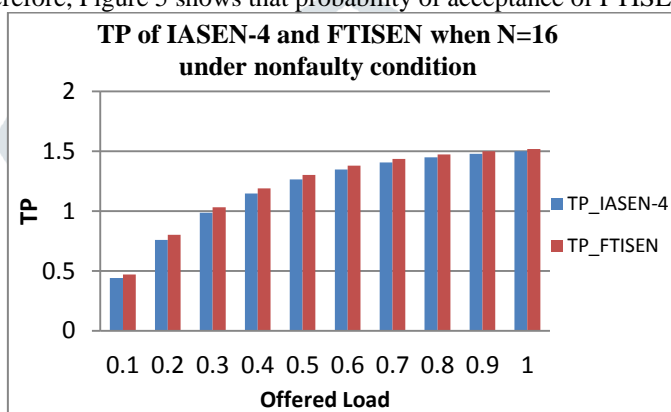
Figure 6. Throughput Comparison of IASEN-4 and FTISEN in Non-Faulty Condition
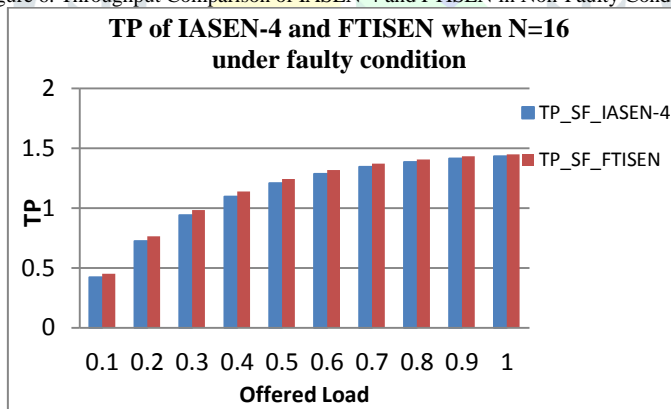
Figure 7. Throughput Comparison of IASEN-4 and FTISEN in Faulty Condition

Figure 6 and Figure 7 show that throughput of FTISEN is greater than IASEN-4 in faulty and non-faulty cases respectively.
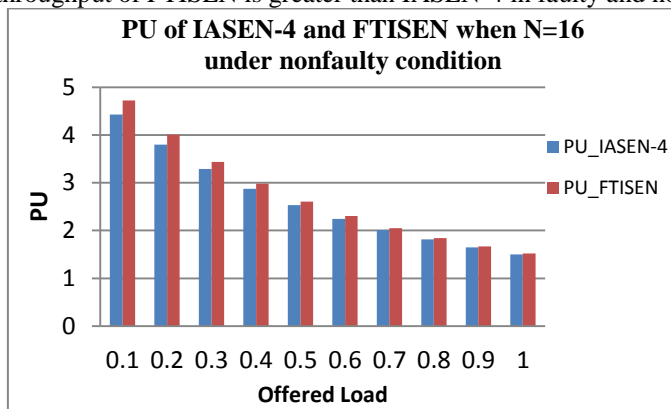

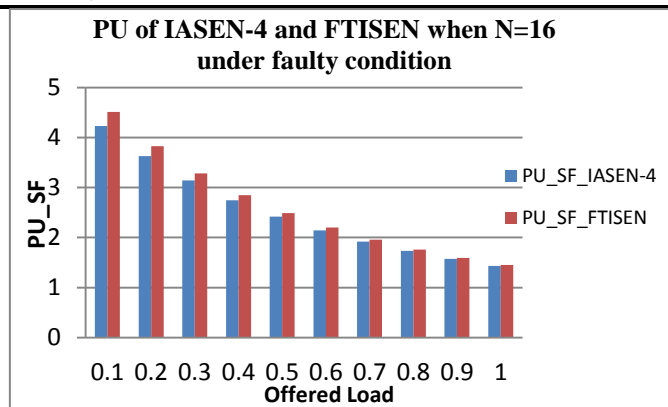Figure 8. PU Comparison of IASEN-4 and FTISEN in Non-Faulty Condition

Figure 9. PU Comparison of IASEN-4 and FTISEN in Faulty Condition

The processor utilization of FTISEN is greater than IASEN-4 in Figure 8 and Figure 9 for non-faulty and faulty cases respectively.
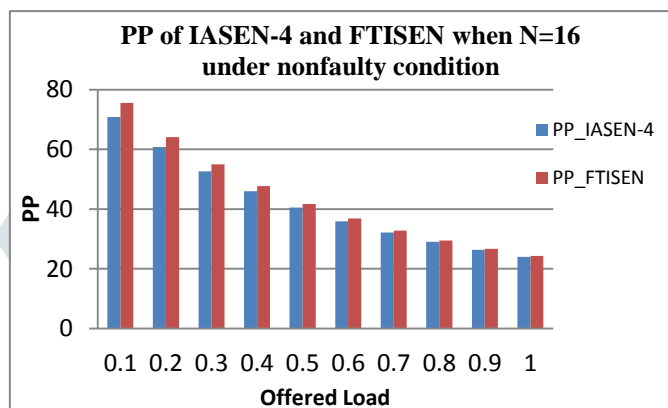

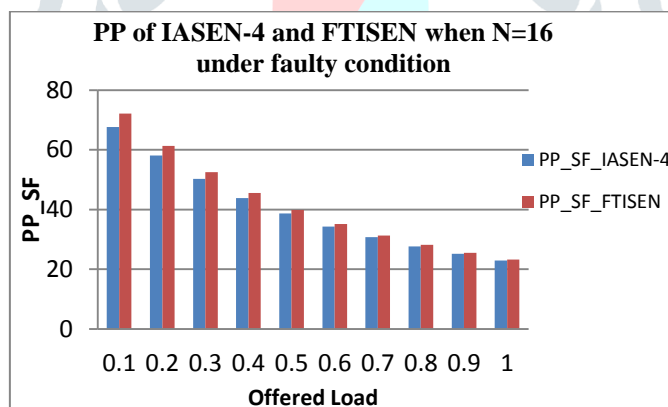Figure 10. PP Comparison of IASEN-4 and FTISEN in Non-Faulty Condition

Figure 11. PP Comparison of IASEN-4 and FTISEN in Faulty Condition

Processing power of FTISEN is greater than IASEN-4 in Figure 10 and Figure 11 for non-faulty and faulty cases respectively.

VI. CONCLUSION

In this paper, we proposed a class of fault tolerant multistage interconnection network, named as FTISEN, which can accomplish huge resilience to faults and great performance. We provide a generalized structure (link connection formula for each stage) of FTISEN which is rarely discussed in any irregular MINs. In our analysis we assume that any node (switch/MUX/DEMUX) in FTISEN have a possibility to fail. It has been observed that the proposed FTISEN provides better fault-tolerance by providing more paths between any pair of source-destination as compared to existing IASEN-4. From tables II and table III, on comparing the results with the IASEN-4 it is evident that the proposed FTISEN provides higher bandwidth, throughput, processor utilization, and processing power in faulty (single switch fault) and non-faulty conditions.

VII. ACKNOWLEDGMENT

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