16T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage

P. Bhavya [1]

Student, Department of ECE, JNTUA College of Engineering, Ananthapuramu,India[1] ,

ABSTRACT:A Novel 16-transistor static random access memory cell with improved data stability in subthreshold operation is designed. The proposed single ended with dynamic feedback control SRAM cell enhances the Static Noise Margin for ultra low power supply an equalized bit line scheme to eliminate the leakage dependent on data pattern and thus improves RBL sensing . The design is to reduce the circuit complexity level and strom consumption level. The architecture contains sleep transistor which is used to reduce outflow power when these operate in "stand by mode " due to inefficient passing of the voltage.

Index Terms – Ooze reduction, Semiconductor Memory

I INTRODUCTION

Reduction of the supply voltage is the most straightforward technique to reduce the active power dissipation. Read Bit Line is charged and discharged through the read port according to the state of stored bit.RBL is powered by virtual power rails that run horizontal and are shared by the cells of a word. The dynamic control of read port power rails reduces the RBL leakage substantially. We Precharge RBL at VDD/2, while the previous 16T design eliminated the Precharge phase, and used INV to fully charge or discharge the RBL.

The low energie consumptions of CMOS linear chips is advantageous in a number of different ways. Many devices can operate at supply voltages as low as 1V with ultralow leakage current which facilitates battery operation. This not only means less power decay, but for operational amplifiers and comparators it results in a least offset voltage caused by thermal drift and for timers it results in higher accuracy and stability.

II RELATED WORK

Fast access non-volatile memories rest under intense investigation facing integrated in Flip-Flops or computing memories to allow system power-off faddy standby state and save power.They conducted electrical simulations to validate its functional behavior.NVM technologies such as PCRAM, MRAM together RRAM will possibly enable memory chips that inhabit permanently, require low-energy including density and latency closer to current DRAM chips.

Even though most of these technologies abide still in early prototyping stages, their expected properties in terms of density, latency, energy moreover endurance are already estimated. Based on these estimations, several papers have been published proposing practical applications for these new NVM technologies.

Caches are used to store frequently used information close to who needs it. They are used at several layers of computer architecture, but probably the most important are mainframe caches. In order to explore lo cality of reference, we need to place memory with very fast access close to the pro cessor. The result is that pro cessor caches reside between the CPU and main memory, as depicted Centralprocessor caches usually are transparent caches , meaning that the same addressing space is shared between the cache and the backing storage.

- ✓ B. Wang, T. Q. Nguyen, A. T. Do, J. Zhou, M. Je, and T. T. H. Kim, Design of an ultra-low voltage 9T SRAM with equalized bit line leakage and CAM-assisted energy efficiency improvement.
- ✓ Ultra-low power VLSI circuit design demystified and explained: A tutorial M. Alioto, -2012 The analysis ranges from the circuit to the micro-architectural level, and reference is given to process, physical and system levels when necessary. Among the main goals

of this paper, it is shown that many paradigms and approaches borrowed from traditional above-threshold low-power VLSI design.

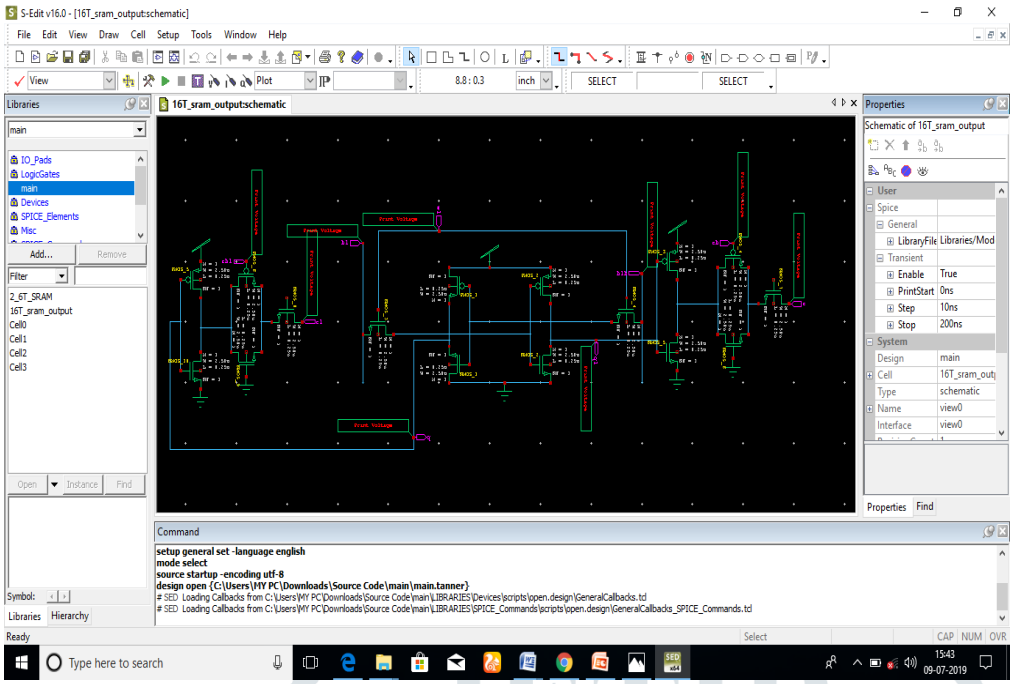
- ✓ Prashant Upadhyay, Rajib Kar, Durbadal MandaI,Sakti P Ghoshal A novel 10T SRAM cell for low power circuits.
- ✓ Single-ended Schmitt-trigger-based robust low-power SRAM cellS. Ahmad, M. K. Gupta, N. Alam, and M. Hasan, -2016 A new figure of merit that comprehensively captures stability, delay, power dissipation, and area of an SRAM cell is also proposed. Based on the proposed metric, we observe that the proposed cell outperforms all, but one of the SRAM cells considered here.To increase the fast writing operation level.
- ✓ The GreenDroid mobile application processor: An architecture for silicon's dark future, N. Goulding-Hotta et al., -2011 The Greendroid mobile application processor demonstrates an approach that uses dark silicon to execute general-purpose smart phone applications with less energy than today's most energy efficient designs. To reduce the power consumption level.

III PROPOSED SYSTEM

The architecture consumes less energy due to the internal memory placement. For a read-0 operation, RBL discharges through TG and NMOS transistor, and for the next precharge, Read Bit Line is supplied current by VP. For a read-1 operation, RBL is charged from vdd/2 to vdd by virtual read port.RBL leakage is reduced by more than 3 orders of magnitude, and thus a higher number of cell could be integrated on a single column.

The modified design for the SRAM CMOS architecture and to optimize the placement for the SRAM Row Cache function.The proposed system is to modify the Heterogeneous SRAM Architecture and to use the manufacture process in any memory architecture.This technique is to reduce the energy consumption level and to optimize the writing in the SRAM memory functions.

- ✓ The proposed 16T SRAM bit cell and the layout. The read port consists of three NMOS LVT transistors (M7, M8 and M9) for realizing the equalized bit line leakage.
- ✓ The write access paths and the data storage latch are implemented with HVT devices for leakage reduction.
- ✓ A read operation starts by enabling the read word line (RWL) and is followed by RBL conditional discharging when the read data is '0'.
- ✓ When a write operation is enabled, current from WBL/WBLB charges node Q/QB to form data '1' or '0'.
- ✓ In the future, we will investigate an optimized sensing scheme for the proposed SRAM over a wide VDD range.



16T SRAM CMOS DESIGN

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- ✓ The Static Random Access Memory architecture is mainly used to the single cell storage process in any type of memory architecture. Domicile requires less power consumption for the storage of 1-bit.
- ✓ The address selection process is to identify the correct data in overall memory array cell function, then to select the read data process using the 3:8 decoding architecture design.
- ✓ This design is to implement the Semiconductor memory array architecture and to enhance the read performance level in overall SRAM memory design.
- ✓ The decoder architecture is to consist of basic logical gate structure and to apply the input bit in decoder architecture. Then to activate the read line bit
- ✓ The proposed 16T SRAM bit cell and the layout. The read port consists of three NMOS LVT transistors (M7, M8 and M9) for realizing the equalized bit line leakage.
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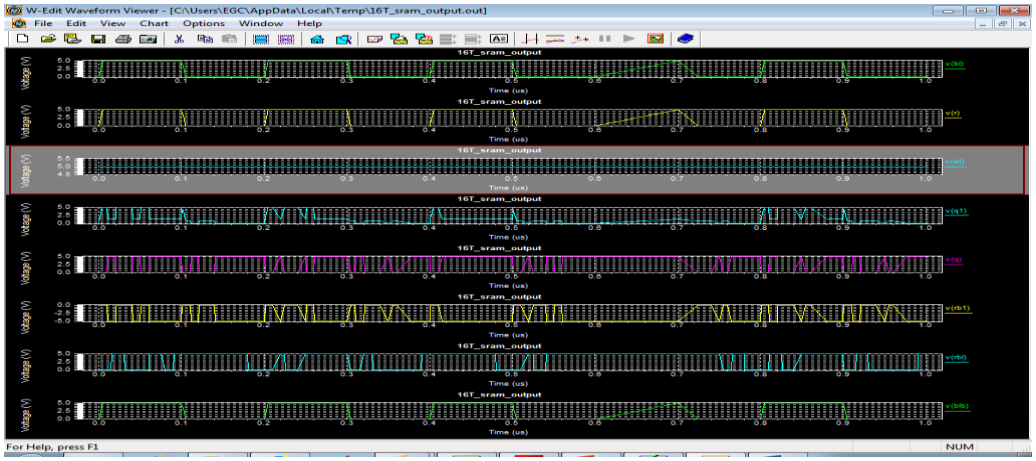
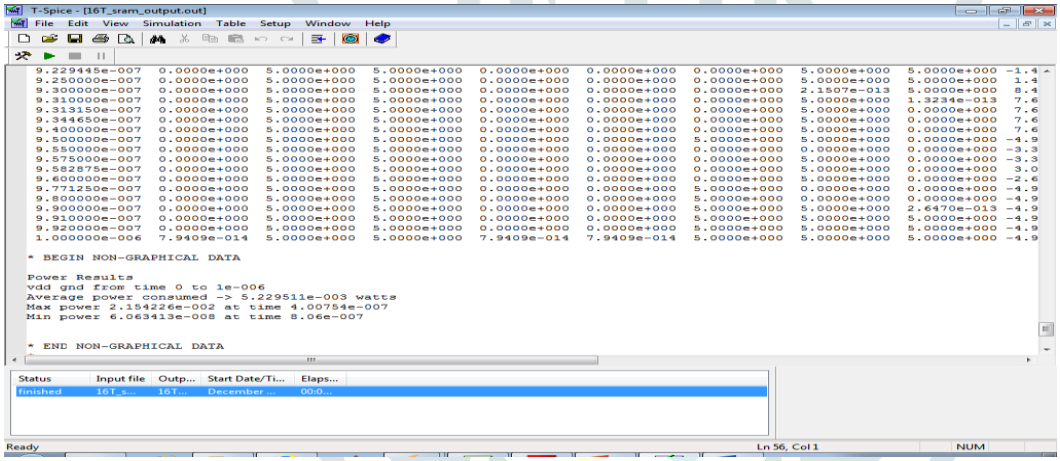
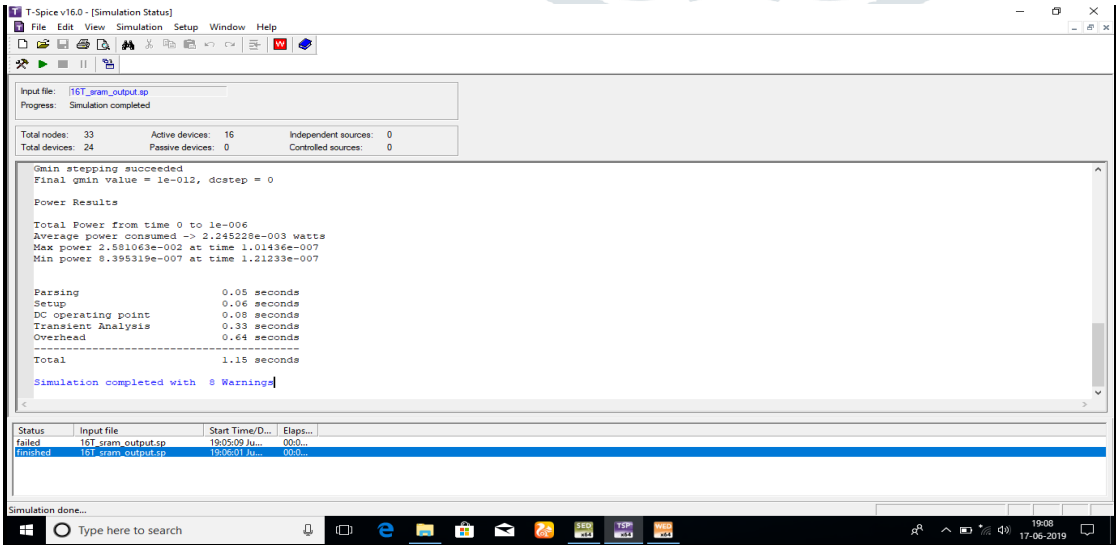
IV EXPERIMENTAL RESULTS



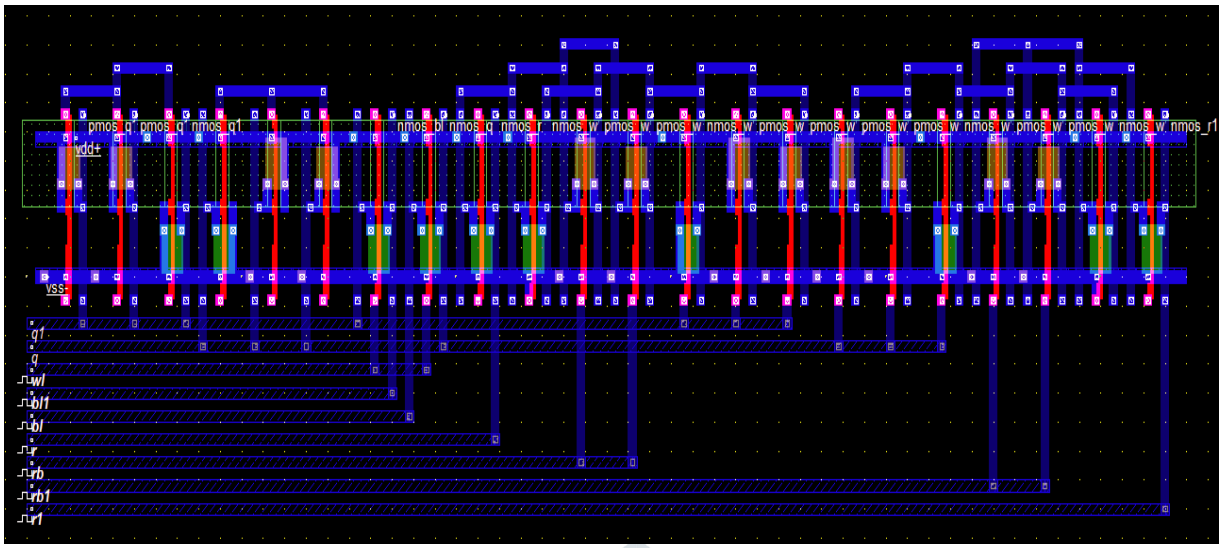
1. SIMULATION OUTPUT



2. POWER ANALYSIS



3.TIMING ANALYSIS



4 . SRAM LAYOUT

VII. CONCLUSION

16T SRAM specially type-II with sleep model is the best technique and it yields more than 98% leakage power reduction as compared to the basic SRAM cell and almost 99% leakage power as over the basic Sixteen Transistor cell. This work is operated with analog input voltage of 0 to 1.8v, supply voltage 1.8v, and consumes 49.94mW power. The schematic is designed for storage capacity of 256 bits i.e. 16x16 Memory array. The complete array which includes peripheral components such as memory bit cell, write driver circuit.

VIII REFERENCES

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BIOGRAPHY

P. Bhavya Currently pursuing M. Tech in Software Engineering at JNTUA College of Engineering, Anathapuramu, A.P,India , during 2017 to 2019 . Her area of interest is Verilog, Tanner and System Verilog.