# Implementation of double fault tolerant full adder using fault localization with pipelining

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***Abstract :*** In the era of microelectronics, rate of chip disappointment is expanded with expanded in chip thickness. A framework must be fault tolerant to diminish the disappointment rate. The nearness of various faults can obliterate the usefulness of a full adder and there is an exchange off between number of fault endured and zone overhead. This paper displays a territory productive fault tolerant full adder plan that can fix single and twofold fault without intruding on the normal task of a framework. RTL amalgamation has been finished by utilizing Xilinx 14.7 and recreation is finished by utilizing Xilinx Isim. In this work we used to identify the fault dependent on interior usefulness by utilizing oneself checking full adder and pipeline idea. By the proposed work of fault endured we can get compelling outcomes as far as Region, Delay, Power utilization angles and number of fault endured when contrasted with the current designs.

***IndexTerms*** **-Single fault, double fault, self checking adder, self repairing, fault tolerant, Adder.**

## I. INTRODUCTION

Fault tolerant structures are mostly utilized for assortment of tasks such guard framework, Satellite and wellbeing measures e.t.c. An error happened in a framework may cost a few Harm or influence human life too. Be that as it may, a few frameworks are reconfigurable, which fix it. These framework can't be disassemble and fix that error consequently. In the present situation, VLSI circuits become more mind boggling as the CMOS highlight size is scaling in nanometer routine. This downscaling makes the circuit more conservative and touchy to the transient faults. Transient fault happened in the incorporated circuit because of electromagnetic clamors, infinite beams, cross-talk and power supply commotion. What's more, innovation scaling further expands the odds of the nearness of perpetual fault too. The idea of self checking and fault tolerant is acquainted with arrangement with the issue of fault. Self checking shows the discovery of faults and ignores the overhead connected with fault recuperation. The vast majority of oneself checking approaches re-execute the guidance for the fault recuperation. Be that as it may, this procedure diminishes the performance of the framework since every faulty hub are reelected. Nonetheless, this procedure does not ensure the fault recuperation if the fault is changeless.

Adder performs an assortment of uses in digital framework and has extraordinary importance DSP activities. There are two sorts of faults happen in full adder plan for example single fault and twofold fault. Single fault makes just one output faulty at once. Be that as it may, twofold fault makes both the outputs faulty at once. It is extremely hard to distinguish and fix the twofold fault. This makes the plan more mind boggling and requires more territory overheads. It makes the fault tolerant full adder structure a matter of extraordinary importance. Previously, numerous methodologies are acquainted with structure oneself checking full adder utilizing equipment redundancy or time redundancy. These methodologies become fruitful in distinguishing the fault however bombs in demonstrating the definite area of that fault. Thus, it makes the other module faulty because of the proliferation of the carry. In this paper, we propose another fault tolerant structure which demonstrates the single and twofold fault with its and programmed fault fixing is likewise conceivable in this design.

## II. PREVIOUS DESIGN APPROACHES

A. Time Redundancy

Redundancy is required in self checking framework. Time redundancy is a self checking approach and is utilized to identify the transient fault. This methodology utilized the copy equipment notwithstanding the original equipment to perform a similar task at various interim of time . The delayed clock is given to the copy equipment. The fault is recognized by contrasting the outputs of both original and copy equipment. On the off chance that the outputs of both the equipment are observed to be same, it speaks to sans fault condition. In any case, if the outputs of both the equipment are unique, it speaks to the faulty condition. The fundamental confinement of this methodology is that it does ensuing calculation to lessen the proliferation delay before contrasting the outputs. Thus, if the main calculation result is faulty and it is utilized for different calculations, additionally makes the ensuing modules faulty.

B. Hardware Redundancy:

The normally utilized equipment redundancy methodologies are Triple modular redundancy (TMR) and Twofold modular redundancy (DMR) Triple modular redundancy approach is utilized to identify the single fault. As demonstrates by its name, it requires three indistinguishable modules in parallel to distinguish the fault. A fault is identified in the event that anybody output of the modules are unique. In any case, this methodology isn't proficient in demonstrating the careful area of the fault. Therefore, this methodology gives the faulty outputs if two single full adder cells become faulty at once. This issue can be evacuated by expanding the equipment yet the subsequent structure requires more than 500 % equipment.

Twofold modular redundancy approach is utilized to identify the single fault at once by looking at the outputs of activity performed by the original equipment and copy equipment in parallel. This methodology requires 200 % equipment cost though the equipment prerequisite of TMR is 300%. Thus, this methodology ends up fruitful to expands the dependability of the plan at the base expense. Be that as it may, fault correction is unimaginable in this methodology in light of the fact that the casting a ballot circuit cannot recognize the area of the faulty module. The major disadvantages of the equipment redundancy approach are that it

requires more than 200% zone overhead and can-not distinguish twofold fault at once . The subsequent issue is that fault recuperation is beyond the realm of imagination since it can't identify the faulty module. What's more, stuck-at faults are not detectable in this methodology and an issue is makes when both the modules experience the fault.

C. Self -checking CSA

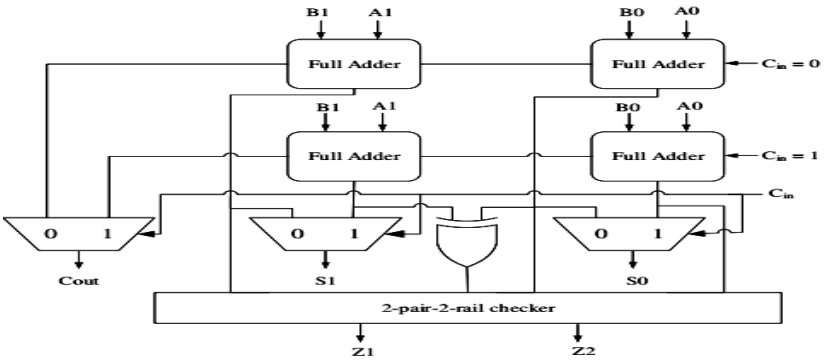


Fig.1. 2-bit self checking carry select adder

In self checking CSA, any single fault and single stuck-at fault can be identified successfully by 2 sets 2-rail checker during the web based testing. Moreover, self-checking multiplexers and XOR gates are additionally used to distinguish these faults. This self checking adder is proposed by Vasudevan et al and appeared in Fig. 1. The full adder utilized in Fig.1 is structured with 28 transistors. Faults are recognized at the essential outputs by oneself checking multiplexers. The checker has two outputs mixes 01 and 10 and shown by Z1 and Z2. The blend of the two outputs demonstrates the nearness of faults. 00 and 11 shows the fault in the full adder cells. Be that as it may, 01 and 10 shows that the full adder cells are sans fault the impediments of this structure are that it can identify single net fault without demonstrating its definite area and additionally the issue of fault engendering through carry. Therefore, fault recuperation is preposterous in this methodology.

D. Self repairing adder

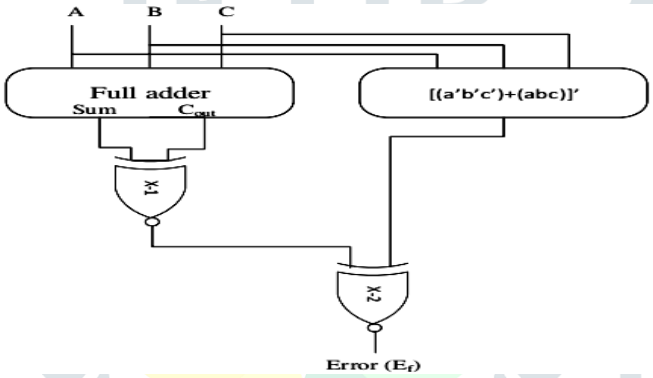


Fig 2. Self checking full adder

Self repairing adder expels the issue of fault engendering through carry happened in the past self checking configuration by showing the precise area of fault. This adder is proposed by Mohammad ali akbar et at and the plan of self checking full adder is appeared in Fig. 2. The equipment prerequisites of self checking adder are full adder cell, equal analyzer and two XOR gates for self testing the fault.

$$Sum = A \oplus B \oplus C_{in}$$

$$Cout = AB + C_{in}(A + B)$$

$$Eqt = NOT((A.B.Cin) + (ABCin))$$

The XOR gate (X-1) is utilized for contrasting the whole and carry outputs produced by the full adder cell. It works on the rule that whole and carry outputs will be equivalent when all the input connected are equivalent and the total and carry outputs will be supplement to one another when any of the three inputs connected is unique in relation to residual inputs. The XOR gate (X-2) is utilized to think about the outputs of XOR gate (X-1) and practical unit [(A'B'C') + (ABC)]'.The fault is spoken to as Ef. In the event that Ef is 0, it demonstrates that there is a fault and if Ef is 1 it demonstrates the fault free condition. The fundamental issue of this plan is that it falls flat, if twofold fault happen in both aggregate and carry outputs at once. For this situation, Ef demonstrates the fault free condition and faulty output propagates to the following unit through carry and makes them faulty.

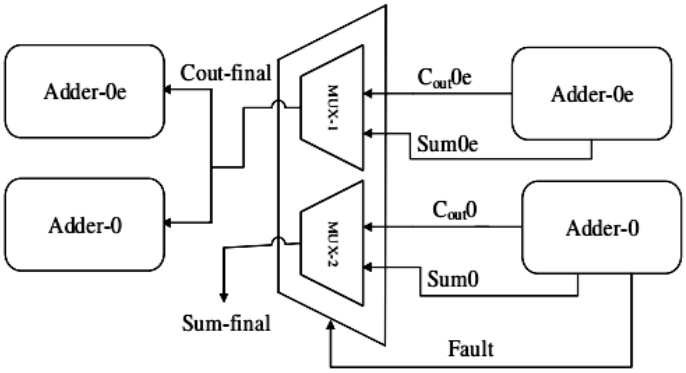


Fig.3. Self repairing adder

The faults recognized in self checking procedure are fixed by supplanting the faulty full adder cell with another excess full adder as appeared in Fig.3. The working behavior is that one adder is work as a normal adder while the another adder is work as excess adder. The equipment prerequisites of this structure are two self checking full adders and two multiplexers. The confinement of this plan is that it bombs when twofold faults happen at once. For this situation, the fault sign output (Ef) of this structure demonstrates that there is no fault and self fixing configuration won't work in this on a fundamental level. Therefore, fault isn't fixed by oneself fixing adder and full adder demonstrates the faulty output.

## III. PROPOSED SELF CHECKING ADDER

The output expressions for the sum and carry outputs of the full adder is shown in equations 1 and 2.

$$Sum = A \oplus B \oplus C_{in}$$

$$Cout = AB + BC_{in} + C_{in}A$$

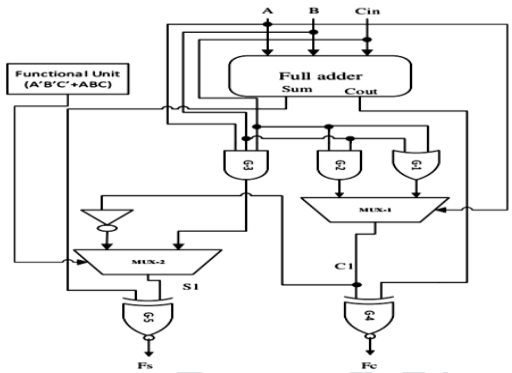


Fig.4. Proposed self checking full adder design

Table 1: Self checking full adder design

| A | B | C | Sum | Carry | G1 | G2 | G3 | Eqt | Fc | Fs |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The proposed self checking full adder is based on the principal given below.

(1) The sum (1) The whole output is inverse to the carry output when vectors of inputs A, B and C are not approach for example (010,100). It demonstrates that aside from (000) and (111) input blends of A, B and C total output is inverse to the carry outputs as appeared Table 1.

(2) The entirety output is equivalent to the carry output when input vectors A, B and C is equivalent for example (000, 111). It demonstrates that for initial (000) and last (111) input blends of A, B and C, whole output is equivalent to the carry outputs as appeared Table 1.

The total structure of oneself checking full adder is appeared in Fig. 4. The gates G1 and G2 are utilized to produce the and OR activity of the input bits B and C as given in 3 and 4. And OR gates are planned utilizing CMOS logic. At that point the outputs gates G1 and G2 are selected by the multiplexer under the control of input A to create the output C1. The output C1 creates the vectors identical to the carry outputs. At that point C1 and Carryout are thought about utilizing XNOR gate G4 as given in condition 5. XNOR gate is planned utilizing DPL logic. On the off chance that both are same, it demonstrates the fault free condition and Fc will be 1. In the event that both are unique, it demonstrates that carry output is faulty and Fc will be 0. Multiplexers are planned through transmission gates. To identify the fault in the whole output C1 is rearranged utilizing an inverter. This output alongside the output (ABC) is bolstered to multiplexer under the control of (A'B'C' +ABC) to create the S1. This output S1 produces the vectors proportionate to the total outputs. At that point S1 and Entirety output are thought about utilizing XNOR gate G5 as given in condition 6. On the off chance that both are same, it demonstrates the fault free condition and Fs will be 1. On the off chance that both are extraordinary, it demonstrates that carry output is faulty and Fs will be 0.

## IV. PROPOSED SELF REPAIRING FULL ADDER DESIGN

The proposed self fixing full adder requires insignificant region overhead than the current structures. The task of the proposed plan is performed utilizing multiplexers under the control of Fs and Fc. The output Fs and Fc are produced by the proposed self checking full adder. The proposed self fixing configuration does not require any stand by adder cell that are utilized to supplant the faulty adder as utilized in the past self fixing full adder. In this methodology, faults are fixed by utilizing inverter instead of the standby full adder cell as appeared in Fig. 5.

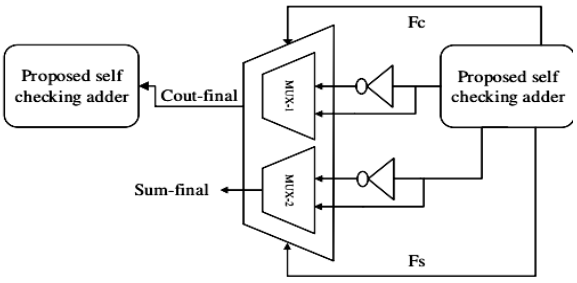


Fig.5. Proposed self repairing full adder design

## V. SIMULATION RESULTS AND COMPARISON

The proposed fault tolerant full adder and some prevalently known self check and self fixing full adder models have been actualized utilizing UMC 55-nm standard cell library in rhythm virtuoso apparatus. Phantom simulator is utilized to perform the reproduction. The equipment overhead and fault location ability of the proposed plan is discovered better in The equipment overhead is figured based on the transistor tally. The proposed fault tolerant full adder requires just one full adder cell with an

inverter and no excess full adder is required which are utilized in the past plans. The equipment cost of the proposed and self fixing adder can be determined and looked at utilizing the condition 7. 100%Area

A. Fault Coverage and Repairing:

In the proposed fault tolerant plan, faults in whole and carry outputs are demonstrated as Fs and Fc individually. The logic high of Fs will demonstrate a fault in the whole output while logic high of Fc will demonstrate a fault in the carry output as appeared in the output waveform of Figs. 6 and 7. The proposed plan has ensured to distinguish and fix the faults (transient and changeless) online regardless of whether the twofold fault happens in the meantime. The fault free output of the proposed fault tolerant full adder is appeared in Fig. 6. In this output Fc and Fs is at logic 1. The faulty output waveform of the proposed fault tolerant full adder is appeared in Fig. 7. In this output Fc and Fs is at logic 0 at specific occurrence, it demonstrates that the output is faulty. This faulty output is fixed by the proposed structure and last aggregate and carry outputs are appeared as SumF and CarryF

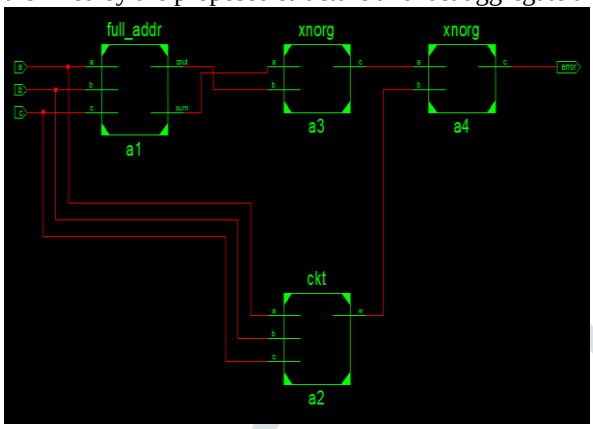


Figure 6: RTL view of Self Checking Full Adder

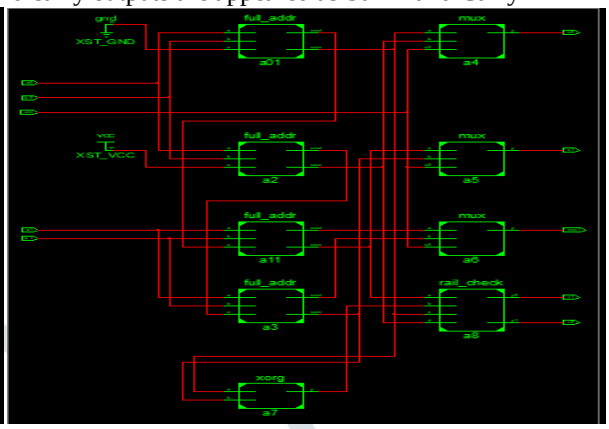


Figure 7: RTL view of 2 bit self checking

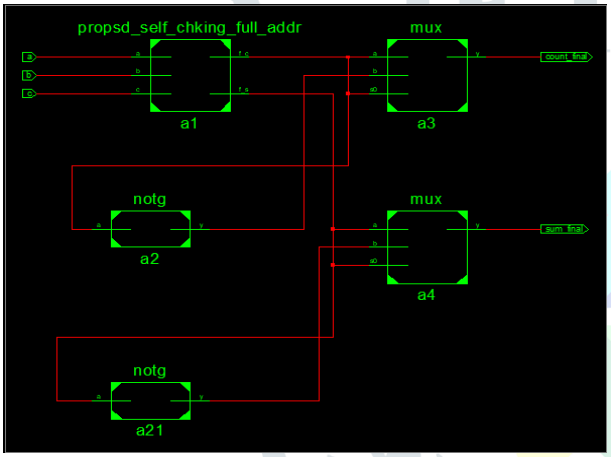


Figure 8: RTL view of proposed self checking

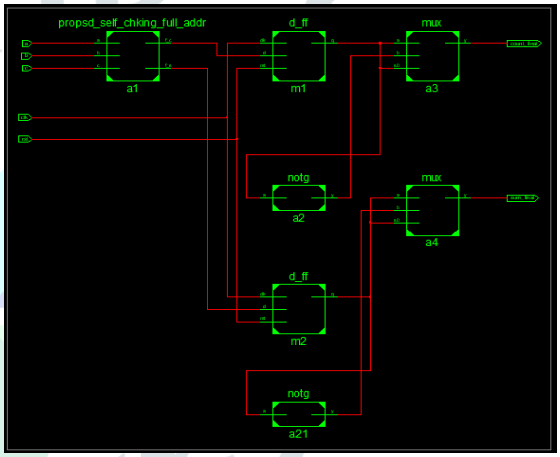


Figure 9: RTL view of extended proposed self checking

The activity of the proposed plan depends on the control signals (Fs and Fc) given by oneself checking full adder. In the event that the control signal Fs is 0, it demonstrates that there is no fault in the total output and the entirety output originating from the full adder cell will be selected by the multiplexer to create the last total. Multiplexers are structured utilizing transmission gates. Then again, If the control sign is Fs 1, it demonstrates that there is a fault in the total output. The faulty aggregate output originating from the full adder cell is fixed by utilizing the inverter. The reversed whole output is additionally selected by the multiplexer to produce the last aggregate. So also, if the control signal Fc is 0, it demonstrates that there is no fault in the carry output, and the carry output originating from the full adder cell will be selected by the multiplexer to produce the last carry.


Figure 10: Proposed self checking

In figure 10, If the control signal Fs is 0, it demonstrates that there is no fault in the total output and the entirety output originating from the full adder cell will be selected by the multiplexer to create the last total. On the off chance that the control signal Fs is 0, it demonstrates that there is no fault in the whole output and the aggregate output originating from the full adder cell will be selected by the multiplexer to produce the last total. In the event that the control signal Fs is 0, it demonstrates that there is no fault in the aggregate output and the entirety output originating from the full adder cell will be selected by the multiplexer to produce the last total. In the event that the control signal Fs is 0, it demonstrates that there is no fault in the total output and the entirety output originating from the full adder cell will be selected by the multiplexer to produce the final sum.

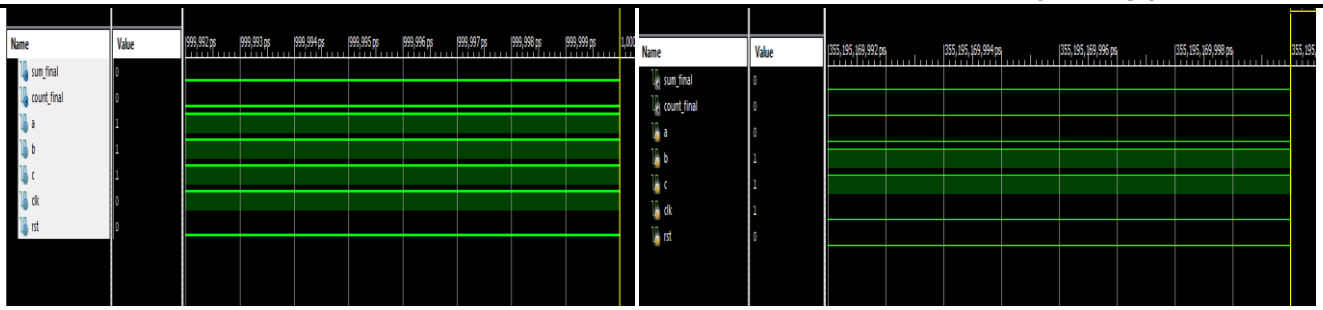


Figure 11: Proposed extended self checking

In figure 11, showing sum and carry result as previous. It's a extended form so it detect fault fast and applicable for double fault tolerant full adder circuit.

Table 5.2 Comparasion of proposed work with revious work

| Sr. no. | Parameter | Previous Work | Proposed work |
|---|---|---|---|
| 1 | Area | 242.85 % | 121% |
| 2 | Delay | 101ns | 60.40ns |

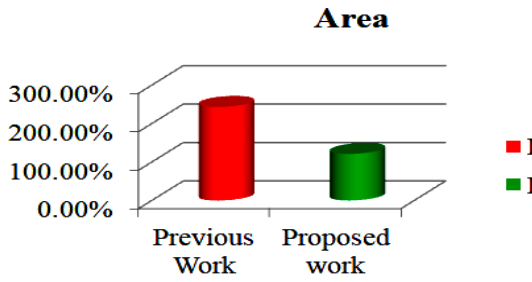


Figure 12: Comparison of area

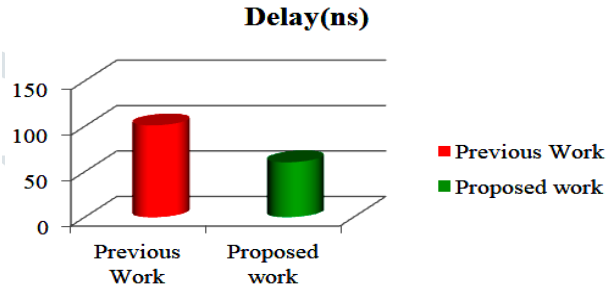


Figure 13: Comparison of delay

The proposed fault tolerant full adder can identify single and twofold fault at once. Henceforth, the proposed structure is free from the issue of fault engendering through carry. Anyway the TMR, DMR, self checking and self fixing full adders have the issue of fault proliferation through carry. Therefore after examination all outcome, it very well may be seen that proposed broadened configuration satisfy all impediment of past work.

## VI. CONCLUSION

In our design, A Carry select adder architecture is presented aiming the multiple fault detection and correction capability. The proposed design consume lesser area because instead of replacing the faulty adder with redundant adder, faulty sum and carry output is inverted using an inverter and multiplexer. Hence, proposed fault tolerant design consumes 19.5 % lesser area than the self repairing full adder. This design is capable in tolerating the double fault in addition to the single fault whereas self repairing full adder can't detect the double fault. The comparison results of the proposed pipe line concept technique are found better that ensure their superior performance capability when compared to the existing designs. We obtained more effective results in proposed design of double fault tolerant full adder in terms of Area, Delay, and power and speed factors.

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