# HIGH SPEED CONFIGURABLE ADDER FOR APPROXIMATE COMPUTING

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**ABSTRACT**

Approximate computing is an effective method for applications with error-tolerance because it can trade off accuracy for power. Addition or expansion may be a key crucial work for applications. In this paper, a high-speed accuracy-configurable adder is proposed, it is based on the conventional carry look-ahead adder, and its configurability of exactness is accomplished by masking the carry propagation at runtime. The proposed 16-bit Accuracy configurable adder reduced critical path delay and area compared with CLA. In addition,the Experimental Results show that the proposed adder accomplished the original purpose of simultaneously optimizing both critical path delay and area without reducing accuracy. Compared to other adders previously studied, the proposed adder delivers significant delay of 4.936ns and speedup with a small area overhead than those of the conventional CLA with delay of 9.169ns.

**Keywords—Accuracy-configurable adder; low-power adder; approximate computing; high-speedadder.**

## I. INTRODUCTION

Recently emerging applications (such as image recognition & synthesis, computationally demanding digital signal processing, and wearable devices requiring battery power) have developed power consumption difficulties. For these applications, Addition is a basic [1][2] Arithmetic function. Most of these applications are tolerated by insignificant inaccuracies approximate computing can be implemented for a tradeoff between power and precision (accuracy) by exploiting the intrinsic tolerancefunction.

This trade off currently plays an important role in such application domains [3]. As a necessity for computational quality so that fan application can differ considerably during Runtime, it is preferable to design quality configurable system that can trade Quality and computational effort according to the demandsof the application criteria [4][5]. The previous configurability suggestions endure the price of increase in power [5] or in delay [12].

A Low power & high speed adder for configurable approximation is highly needed to benefit such an application. In this paper, approximate adder is proposed that can be configured, consuming less power than [5] with a comparable area and critical path delay. Moreover, a critical path delay observed with the proposed Accuracy Configurable adder is much smaller than that of [12] with comparable power consumption. A primary contribution is that, the optimization of critical path delay and area is accomplished simultaneously and without any bias toward either. In order to obtain accuracy configurability of the proposed adder has been introduced, the conventional CLA & Ripple Carry Adder using 45nm library in

Verilog HDL. Then for each of these applications we assessed the power consumption, Design Area and Critical Path Delay. A comparison critical path delay and design area of proposed and existing Technique is provided.

The Accuracy Configurable Adder (ACA) adder has feature of runtime accuracy configurability for better tradeoff between accuracy, performance, and power. In ACA adder, the carry chain is cut to reduce critical-path delay, and sub-adders generate results of partial summations to increase accuracy. Obtain power reductions or performance improvements in return. In some applications, however, more accurate or totally accurate results are required under certain conditions – e.g., image processing in security cameras would require cleaner images after detecting a motion. In contexts where the required accuracy changes during runtime, the accuracy of results should be configurable to maximize the benefit of approximate operations. An Accurate half adder (CMHA) illustrates how power benefits can be achieved with an accuracy-configurable design.

## II. RELATEDWORK

Gupta et al.[6] elaborate the complexity of transistor level conventional mirror adder cell in well manner. Mahdianiet al.[7] suggested a lower-part OR adders that uses OR gates to add lower bits and accurate upper bits adders.Venkatesan et al. [8] discussed an approximate circuit behavior represents that to construct an equivalent untimed circuit. The above static approximate designs [6-8] to meet the quality requirements of applications may fail with fixed accuracy or when high quality is not required, which result in wastage of power. Kahng et al. [4] suggested an ACA (accuracy-configurable adder).The Accuracy configurable adder depends on a pipelinestructure.

Serial Addition: Locally Connected Architectures by Valeriu Beiu, Snorre Aunet, Jabulani Nyathi, Robert R.Rydberg and Walid Ibrahim[2]. This project will briefly review nano electronic challenges while focusing on reliability. We shall present and analyze a series of CMOS-based examples for addition starting from the device level and moving up to the gate, the circuit, and the block level. Our analysis backed by simulation results, on comparing parallel and serial addition shows that serial adders are more reliable while also dissipating less. Their reliability can be improved by using reliability- enhanced gates and/or other redundancy techniques (like e.g., multiplexing). Additionally, the architectural technique of short-circuiting the outputs (of several redundant devices/gates/blocks) exhibits “vanishing” voting and an inherent fault detection mechanism, as both transient and permanent faults could be detected based on current changes. The choice of CMOS is due to the broad design base available (but the ideas can be applied to other technologies), while addition was chosen due to its very solid background (both theoretical andpractical).

The design approach will constantly be geared towards enhancing reliability as much as possible at all the levels. Theory and simulations will support the claim that a serial adder is a very serious candidate for highly reliable and low power operations. Finally, our simulations will identify the $V_{DD}$ range where the power-delay-product and energy-delay-product are minimized. All of these suggest that a reliable (redundant) solution can also be a low power one if using serial architectures, while speed could still be traded for power (e.g., by dynamically varying the supply voltage both above and below $V_{th}$).

Accuracy Configurable Adder for Approximate Arithmetic Designs by Andrew B. Kahng and Seokhyeong Kang[4]. In this paper, we propose an accuracy configurable approximate (ACA) adder for which the accuracy of results is configurable during runtime. Because of its configurability, the ACA adder can adaptively operate in both approximate (in accurate) mode and accurate mode.

## III. PROPOSED ACCURACY CONFIGURABLEADDER

### Carry Maskable Half Adder (CMHA)

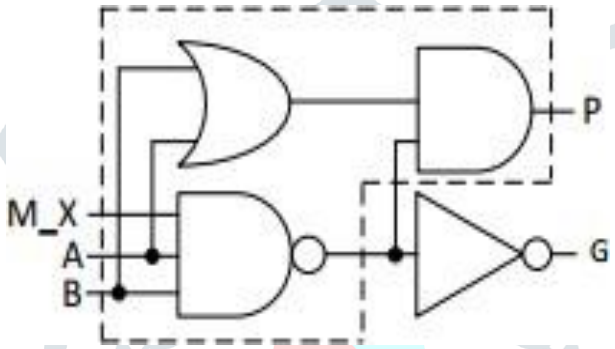


**Fig 3.1 A Carry- Maskable Half Adder.**

Fig.3.1,This is called a Carry Maskable Half Adder (CMHA). It shows an Equivalent Circuit of the conventional half adder. The dashed frame represents A two input XOR (M _X = 1) equivalent circuit. If M_ X =1, then P is equivalent to A XOR B and G is equivalent to A AND B; If M _X = 0, then P is equivalent to A OR B and G is0.The

M _X can be considered as a signal for the Carry mask.

Consider an n bit CLA, whose half adders are replaced by CMHAs (Carry Maskable Half Adder) for generating G and P Signals. A n-bit mask signal is requiredfor each CMHA in this scenario. We are used four Carry Maskable Half Adders (CMHAs) and one bit mask signal to mask the carry propagation of the CMHA,in each group to simplify the structure masking for carry propagation.

The group structure with four CMHAs is illustrated as shown in Fig.3.2, A3-0, B3-0, P3- 0, and G3-0 are four bit signals representing respectively { A3, A2, A1, A0 },{ B3, B2,

B1, B0 },{P3, P2, P1, P0 }, and { G3, G2, G1, G0,}.M X0 is a 1-bit signal connected to the 4 Carry Maskable Half Adders (CMHAs) to concurrently mask the carrypropagation.
When M_X = 1, P3-0 = A3-0 *XOR* B3-0, and G3-0 = A3-0 *AND* B3- 0; When M_X=0,

P3-0 = A3-0 OR *B3*-0, and G3-0 =0. We proposed an accuracy-configurable adder by using CMHAs to mask the carrypropagation.

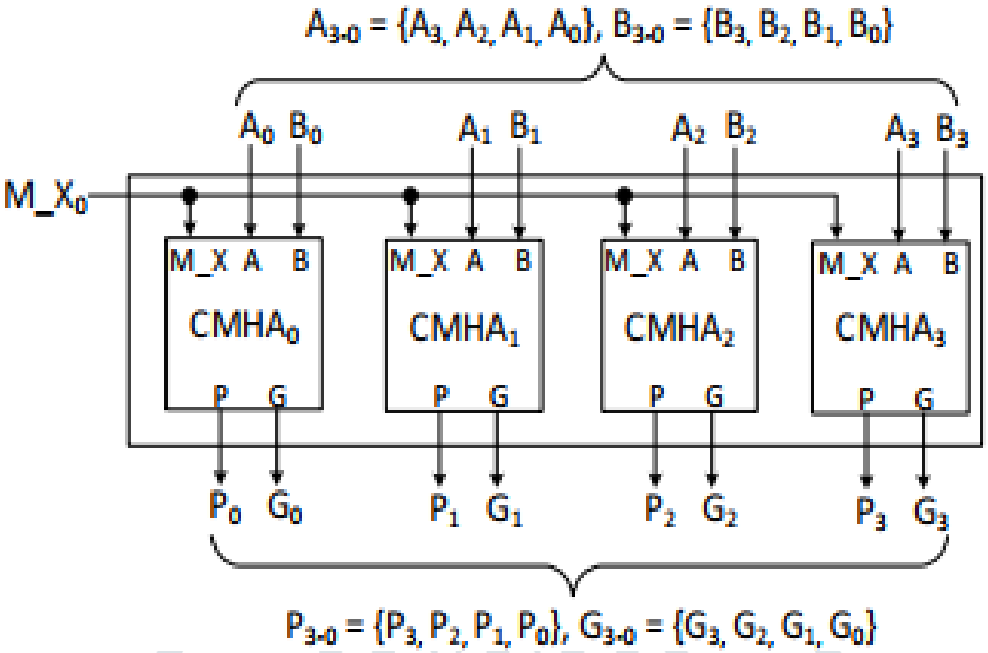


**Fig 3.2. Structure of a group with four CMHAs.**

Proposed an accuracy-configurable adder (ACA), which is based structure proposed an accuracy gracefully-degrading adder (GDA) which allows the accurate and approximate sums of its sub adders to be selected at any time. Our adder proposed in this project does not consider a pipeline structure either. To generate outputs with different levels of computation accuracy and to obtain the configurability of accuracy, some multiplexers and additional logic blocks are required. However, the additional logic blocks require more area. Furthermore, these blocks will cause power wastage when their outputs are not used to generate a sum.

Conventional carry look ahead adder and ripple carry adder are existing methods for multiplier lower-part-OR adder, which utilizes OR gates for addition of the lower bits and precise adders for addition of the upper bits. To construct an equivalent untimed circuit that represents the behavior of an approximate circuit. The static approximate designs with fixed accuracy may fail to meet the quality requirements of applications result in wastage of power when high quality is not required

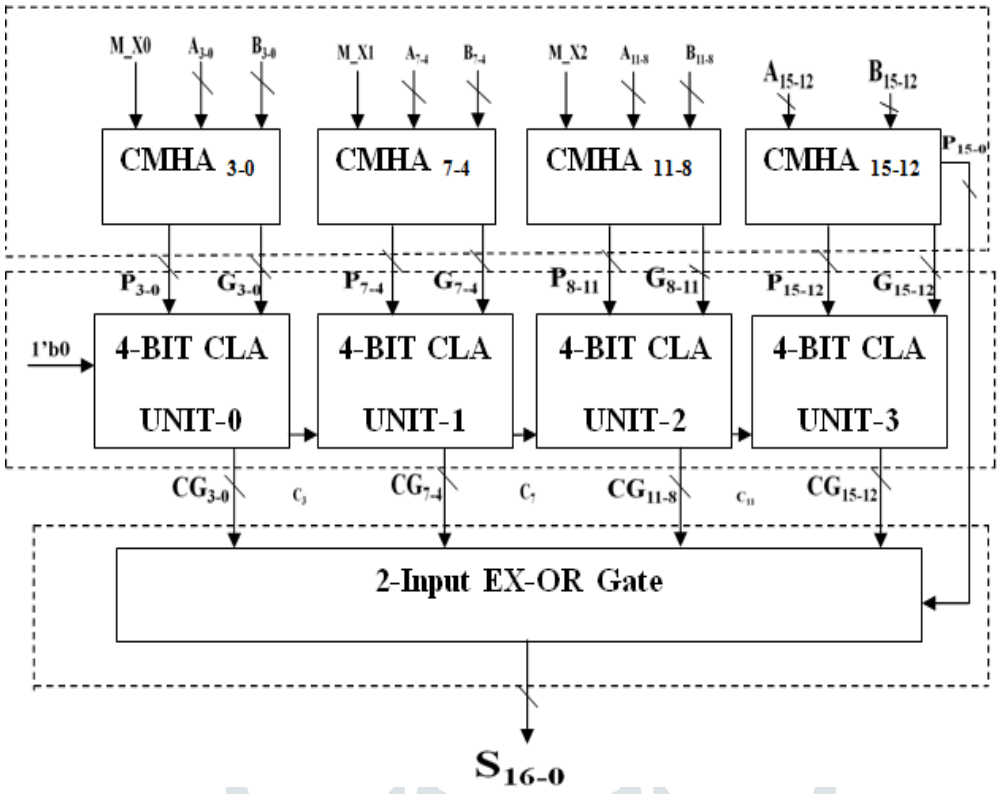


**Fig: 3.3 Structure Of Proposed 16 bit Accuracy Configurable Adder (CMHA)**

These are the suffer the cost of the increase in power or in delay. The structure of the suggested 16-bit Carry Maskable Half Adder Scheme is Shown as an in Fig.3.3, For the preparation of P and G signals, four groups (CMHA30, CMHA7-4, CMHA11-8 and CMHA15-12) are used. There are four CMHAs in each group.

In this instance, there is no mask signal for CHMA15-12, so accurate P15-12(=A15- 12 XOR B15-12) and G15-12 (= A15-12 AND B15-12) are always obtained. P15-0 and G15-0 are the outputs of Part 1 and are linked to Part 2. P15-0 is also connected for sumgeneration to Part 3. Four 4-bit look-ahead units (unit 0, 1, 2, 3) to produce 15 carry in Part 2, (CG3-0, CG7- 4, CG11-8, and CG15-12).

In Part 2 the existing 16 bit adder is required to have 5 units of CLA (Carry Look ahead Adder).Four 4-bit look-ahead units (units 0, 1, 2, 3) generate four PGs (PG0, PG1, PG2&PG3), four GGs (GG0, GG1, GG2, and GG3), and 12 carriers (C2-0, C6-4, C10-8 & C14-12) first,& then the look-ahead unit 4 generates the remaining 4 carries (C3,C7,C11 and C15) using PGs and GGs. However, only 4 units of CLA (Carry Look ahead Adder) are needed in the proposed system. These Carry Look ahead Adders produce 15 CG15-0 Carries. These carries are connected to the Part 3.These Carries (CG15-0) is the output of Part 2 and is connected to Part 3. Using these (CG15-0) carries and Propagating signal (P15-0) is connected to 2-input XOR gates in Part 3 for generate the sum.

## IV. SIMULATIONRESULTS

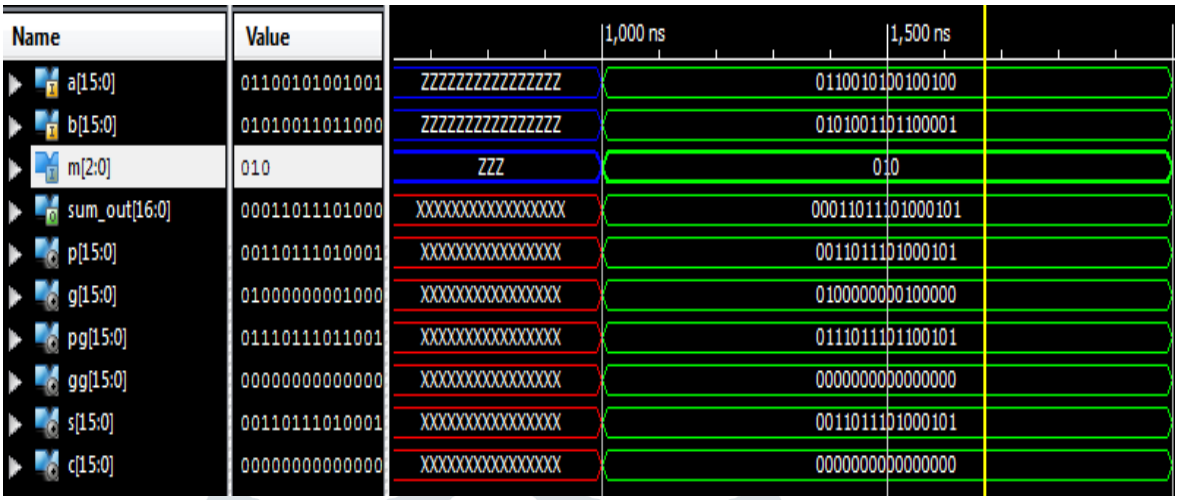


**Fig: 4.1 Simulation results of 16 bit Proposed CMHA**

Consider the Fig 4.1as shown in above, A=1000010111000001, B=0101001101100001, M_X= 101 Depending on the Maskable signal the operation is performed. If M_X=0, OR operation is performed. And if M_X=1, XOR operation is performed. The Approximate Result is 1000010011100101. Carry is the0000000000000000.

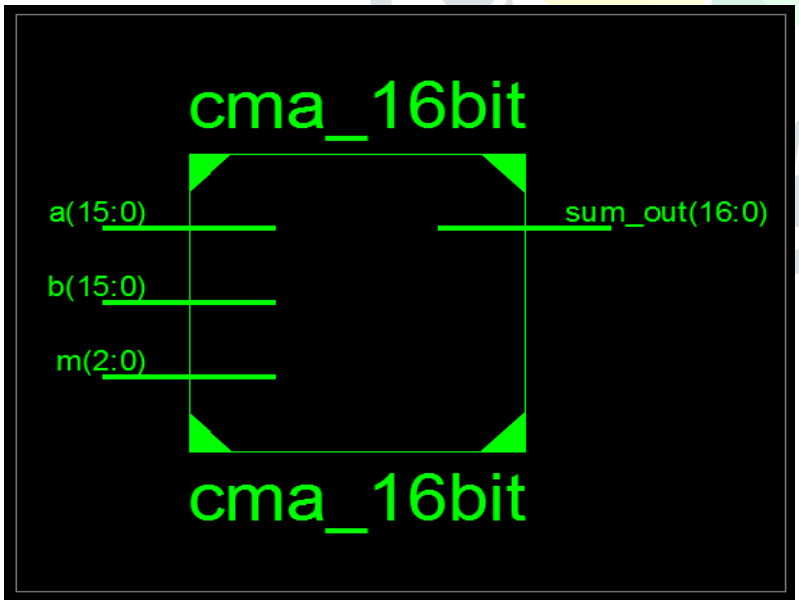


**Fig: 4.2 RTL Block Diagram of 16 bit Proposed CMHA**

RTL Block diagram shown in Fig 4.2, the two 16 bit inputs are a,b are given to the carry Maskable adder, Three bit Maskable signal is given. Depending on the Maskable signal operations are performed. If Maskable signal is zero, then OR operation is performed between 2 inputs, If Maskable signal is one, then

XOR operation is performed between the two inputsa&b.

| Device Utilization Summary (estimated values) | | | [-] |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 9 | 5472 | 0% |
| Number of 4 input LUTs | 16 | 10944 | 0% |
| Number of bonded IOBs | 52 | 240 | 21% |

**Table: 4.1 Design summary of 16 bit Proposed CMHA**

Design summary of 16 bit Proposed CMHA as shown in Table 4.1 the 9 number of slices are used only out of 5472 slices, very less number of slices are used so, the utilization is 0%. Sixteen number of 4 input LUTs are used only out of 10944 LUTs, this is also0%utilization. And 52 Number of bonded IOBs are used out of 240 bonded IOBs, 21% are utilized.

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Timing Summary:
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Speed Grade: -12

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 9.169ns

Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 629 / 17
-------------------------------------------------------------------------
Delay:               9.169ns (Levels of Logic = 10)
  Source:            b<5> (PAD)
  Destination:       sum_out<14> (PAD)
```

**Fig: 4.3 Timing Summary of 16 bit Proposed CMHA**

The Fig 4.3 shows the timing summary of the 16 bit proposed CMHA. The Delay of entire operation is 9.169ns.

| Logic Utilization | Available | Used | | Utilization | |
|---|---|---|---|---|---|
| | | Conventional adder | Proposed adder | Conventional adder | Proposed adder |
| No. of Slices | 5472 | 31 | 09 | 0.566% | 0.16% |
| No. of four input LUTs | 10944 | 53 | 16 | 0.484% | 0.14% |
| No. of Bonded IOBs | 240 | 52 | 52 | 21.6% | 21.6% |

**Table:4.2 Comparison Table of Conventional adder and Proposed 16 bit adder**

The Comparative analysis of a Conventional adder and proposed 16 bit adder as shown in Table 4.2, Conventional adder is used 31 No. of slices but proposed adder only 9 no. of slices are used out of 5472 slices.53 No. of 4 input LUTs are used by Conventional adder, but the proposed adder used 16 LUTs out of 10944 LUTs.The Conventional adder used 52 No. of bonded IOBs are used, the proposed adder also used 52 No. of Bonded IOBs out of 240 No. of Bonded IOBs.

## V. CONCLUSION

In this paper, an accuracy-configurable adder without suffering the cost of the increase in power or in delay for configurability was proposed. The proposed adder is based on the conventional CLA, and its configurability of accuracy is realized by masking the carry propagation at runtime. The experimental results demonstrate that the proposed adder delivers significant delay and speedup with a small area overhead than those of the conventional CLA. The proposed adder achieves the original purpose of delivering an unbiased optimized resultdelay.

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