# IMPLEMENTATION OF ARITHMETIC LOGIC UNIT USING VEDIC MATHEMATICS

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**Abstract:** Arithmetic and Logic Unit (ALU) is the most crucial and core component of central processing unit which consists of many computational units like adders, multipliers, logical units, etc. Real time applications such as controlling environmental conditions demand quick response of the processor for processing. The *vedic* mathematics consists of many *sutras* which can be used for improving speed with reduced component requirements and delay. It accomplishes arithmetic, logic operations on integers stored in accumulator, register array, operand register and fetch value from external memory. In this paper, *vedic* mathematics *sutra* were used for enhancing the overall performance of the processor. *vedic* ALU was coded in VHDL using Xilinx software. The synthesis results indicated an overall improvement of about 0.539 ns for *vedic* over conventional 16-bit ALU.

***Keywords:*** *Vilokanam, UrdhvaTiryakbhyam, Parvartaya,* ALU, etc.

## I INTRODUCTION

For arithmetic and logical operations various *vedic* mathematic techniques like Vilokanam Urdhvatiryakbhyam and Parvartaya have been used. It has been found that the Vedic sutra is the most suitable mathematical technique which gives minimum delay as compared to that of the conventional ALU. With the advent of new technology in the domain of VLSI, communication and signal processing, there is an ever growing demand for the high speed processing and low area design. In this paper, a modified ALU is introduced using *vedic* sutras. *Vedic* technique reduces the propagation delay in processor and hence it reduce the hardware complexity in terms of area and memory requirement. This *vedic* ALU was coded in VHDL by using Xilinx ISE 9.2i.

## II PREVIOUS WORK ON VEDIC ALU

Based on the *vedic* mathematics concepts for digital signal processing applications, many researchers have proposed ALUs and other computational units [1]. From these research, they have proved that conventional arithmetic computational algorithms are very robust when compared to proposed arithmetic computations.

In one of the studies 16-bit Vedic ALU using Vilokanam sutra, Urdhva Tiryakbhayam sutra and Parvartaya sutra for performing the addition, subtraction, multiplication and division respectively was proposed. In this technique to show the efficiency of proposed vedic ALU at 16 bit level, it has been compared with conventional ALU. For the comparison purpose some standard papers have been used. Addition using ripple carry scheme is less efficient when compared to applying *vedic* addition using vilokanam sutra in terms of delay and area. Subtraction using ripple carry scheme is less efficient when compared to applying *vedic* subtraction using vilokanam sutra in terms of delay and area. The efficiency of proposed *vedic* multiplier at 16-bit level has been compared with other popular multiplier structures and *vedic* multiplier showed lowest path delays. The result of device utilization and delay as the restoring division method shows a larger delay as compared to the proposed divider and the percentage of device utilization in restoring division method is quite [2].

In the other study an ALU design using *vedic* mathematics approach was proposed. High speed 8×8-bit multiplier was designed and analyzed. This method is different from the conventional method of employing product of two numbers accomplished by the process of add and shift. This method involved the vertical and crossed multiplication and it was found to be efficient and fast.[3].

Some researcher have proposed a modified compressor based multiplier, constructed experimental set up that used *vedic* mathematics to get a high speed multiplication operation. The designs of 16x16 bits and 32x32 bits *vedic* multiplier was designed using Xilinx 13.2 (vertex 7). The computation delay for 8x8 bits multiplier was found to be 5.02 ns, the computation delay for 16x16 bits multiplier was 9.09ns. The computation delay for 32x32 bits 4:2 compressor *vedic* multiplier was 15.8 ns and for 32x32 bits Wallace tree Vedic multiplier was 12.7ns. It is therefore seen that the Wallace tree *vedic* multiplier observed to be faster than the 4:2 compressor *vedic* multiplier. For vertex 7 the computation delay for 32x32 bits 4:2 compressor *vedic* multiplier was 18.71ns and for 32x32 bits Wallace tree Vedic multiplier were 18.80ns. Urdhvatiryakbhyam, Nikhilam and Anurupye sutras used in proposed algorithm results in minimum delay, power and hardware requirements for multiplication of numbers. Use of a compressor observed to be easy processing element with less complexity which used in digital logic design for compression of data. [4]

Some researcher have proposed an ALU design using *vedic* mathematics concepts. In their proposed designed *vedic* multiplier analysis was carried out using *Urdhav Triyagbhyam* sutra. In this multiplication they eliminated the unwanted steps with zeros that enabled parallel generation of intermediate product. In this high speed power efficient multiplier was achieved. [5]

In other studies an ALU design using *vedic* mathematics approach was proposed. Every digital domain based technology was operated only by ALU either partially or whole. For this high speed ALU was required. The proposed ALU could perform three arithmetic operations with the desired speed. [6]

Some of the other researcher have proposed an 8 bit ALU design using *vedic* mathematics concepts. In this technique, he reduces the propagation delay in processor and hardware complexity in terms of area and speed by eliminating the unwanted multiplication steps[7].

In one of the study, it is discussed that VLSI architecture have higher orders of time and space complexities. In this he designed binary division architecture using Nikhilam sutra and Paravartya sutra[8].

## III SCHEMATIC DIAGRAM OF VEDIC ALU

. The two binary inputs are given and output result is addition, subtraction, multiplication and division.The addition is carried out using vilokanam sutra. The subtraction is also carried out using vilokanam sutra based on 2's complement method. The multiplication is carried out using Urdhav Triyagbhyam sutra. The division is carried out using Paravartya sutra. Fig.1 shows the schematic diagram of the proposed *vedic* ALU

The vedic ALU consists of four blocks as follows:

1. Addition using Vilokanam Sutra
2. Subtraction by 2's complement using Vilokanam Sutra
3. Multiplication using Urdhva Tiryakbhayam Sutra
4. Division using Nikhilam Sutra

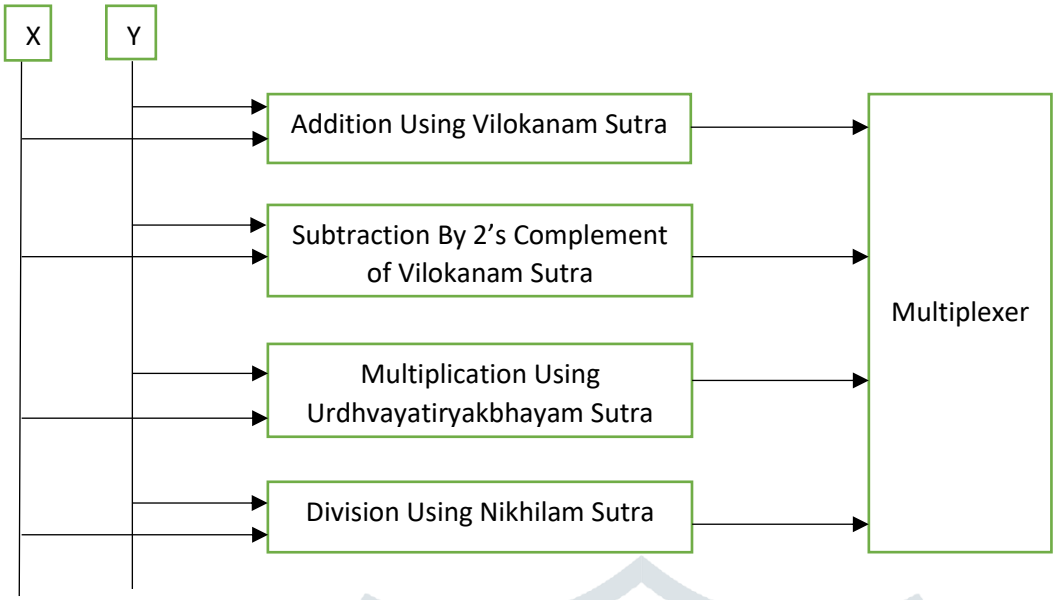


Fig.1 Schematic diagram of vedic ALU

## IV METHODOLOGY

The working of this vedic ALU is done as per the basic concept of vedic sutras:

A. Vilokanam Sutra For Addition

Vilokanam sutra basically follows 3 rules as follows

1. Left to right addition
2. End number concept (take only right most digit of once place addition)
3. Carry(sum>=10) and non-carry(sum<10) number consideration

Perform addition of 24 and 7 using Vilokanam Sutra:-

2 4

\+ 7

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2 1

3 1 (7+4=1 1) here the sum of 7 and 4 is 11 which is greater than 10 so carry is created and added to tens digit

Observation is that the overall system is carry independent due to which delay gets reduced.

B. Vilokanam Sutra for Subtraction

Figure 2 shows the basic concept for *N* bit adder and subtractor in which the subtraction is performed using the concept of 2's complement.

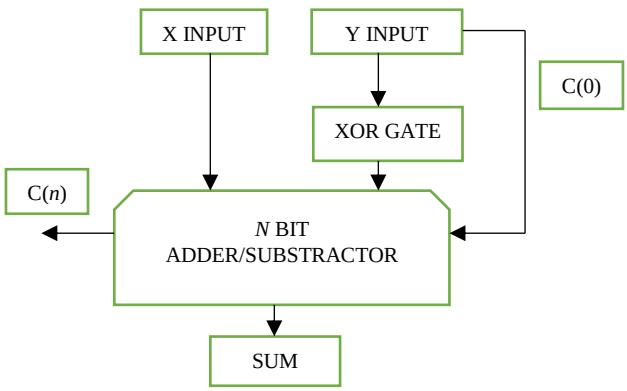


Figure 2 *N*-bit adder / subtractor

Perform subtraction using 2's complement method

54 – 22 =32 $(110110)_2 – (010110)_2 = (100000)_2$

The obtained result is 100000, for C(0) = 0 addition, otherwise subtraction

C. Urdhva-Tiryakbhyam for Multiplication

1. The word "Urdhva-Tiryakbhyam" shows vertical and crosswise multiplication.

2. This sutra is used for the multiplication of two numbers in decimal number system. The same concept can be applicable to binary number system.

Vedic mathematics is mainly based on 16 *sutras* dealing with various branches of mathematics like arithmetic, algebra, geometry etc.

These methods can be directly applied to plane and spherical geometry, trigonometry, conics, calculus (both differential and integral), and applied mathematics. In conventional mathematics the step required for calculation are more, in order to reduce the step for calculation in Vedic mathematics plays great role. This is so because the Vedic formulae are to be based on the natural principles on which the human mind works. Figure 3 shows that the line diagram for multiplication of two 2 digit numbers which perform the 2 digit multiplication operation. Take a two numbers, multiply the numbers in the unit place and put the product under unit place. Cross multiply first unit place tens place number and add the two products and place the answer to the left of the unit place's answer. Multiply the numbers in the tens place and place the answer to the left side of the previous answer step. This is a very interesting part of the mathematics and it presents some effective algorithms that can be applied to various branches of engineering.

The multiplier architecture can be generally classified into three types. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second one is the parallel multiplier (array and tree) which carries out high speed mathematical operations.

Observation is that the partial products and their sums are calculated in parallel due to which the multiplier independent of clock frequency of processor, thus multiplier require same amount of time to calculate product. Fig.3 shows the line diagram for multiplication of two 2 - digit numbers

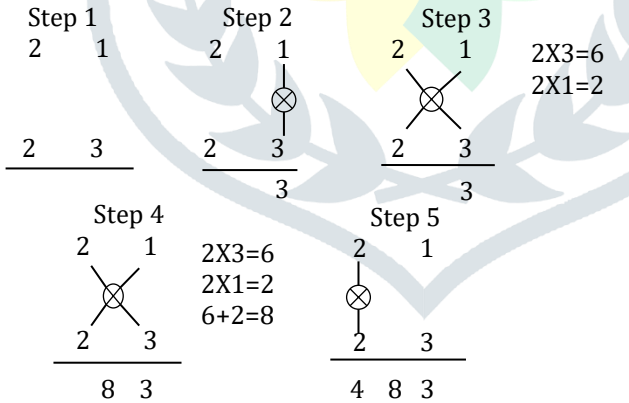


Fig.3 Line Diagram for Multiplication of Two 2 - Digit Numbers

D. Parvaartya Yojayet Sutra For Division

In this sutra the division is performed firstly by leaving the left most digit of divisor, after leaving the left most digit of the divisor apply transpose and then perform the right shift as shown in the below example.

1345 ÷ 112

| | |
|---|---|
| 1 1 2 | 1 3 4 5 |
| -1 -2 | -1 -2 |
| | -2 -4 |

1 2 0 1

For obtaining the quotient of the division (difference of digit in dividend and divisor + 1)= (4-3)+1=2. Thus two digits from left gives quotient as 12 and remainder as 01

## V RESULTS AND DISCUSSIONS

*Vedic* mathematics *sutra* were used for enhancing the overall performance of the processor. *vedic* ALU was coded in VHDL using Xilinx software. The synthesis results indicated an overall improvement of about 0.539 ns for *vedic* over conventional 16-bit ALU.This shows that data1 and data 2 are inputs provided to perform addition, subtraction, multiplication and division and Figure 4 shows the top level RTL schematic of 16-bit ALU.

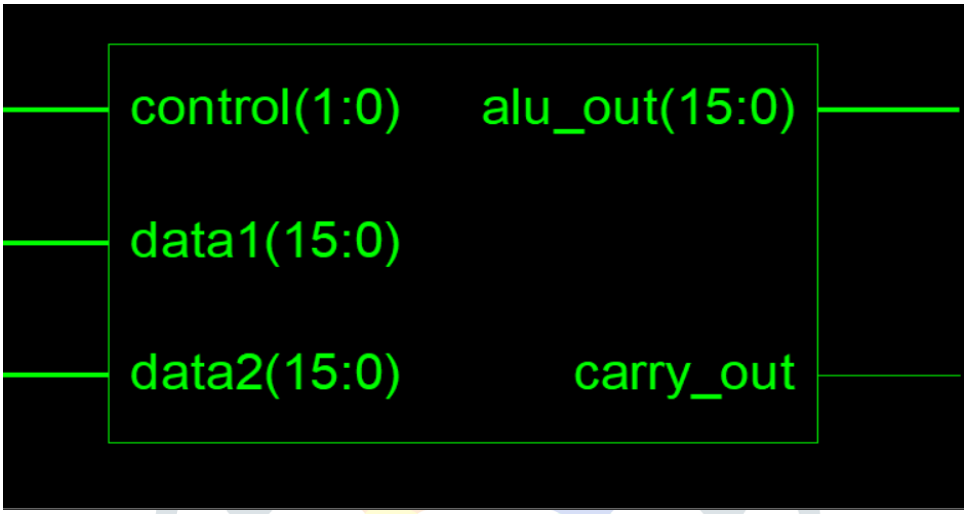


Fig.4 Top Level RTL Schematic of 16-Bit ALU

The description about the data inputs, control inputs and output of the ALU is given as follows

Description:-

I. DATA1 : Input data 16 – bit

II. DATA2 : Input data 16 – bit

III. ALU OUT :Output data 16 – bit

DATA1= 0000000000001100(12)

DATA2 = 0000000000001000(8)

CONTROL INPUT

00 for addition out1= 20

01 for subtraction out2=4

10 for multiplication out3=96

11 for division quotient out4=1

Thus, the obtained result is shown using the test bench waveform in fig.5

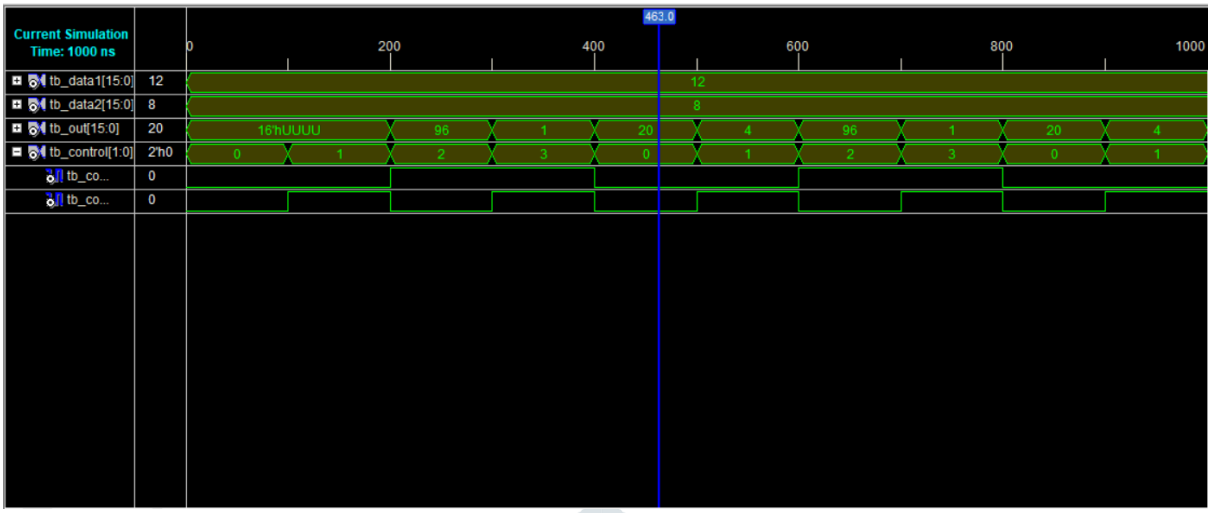


Fig.5 Test bench result for 16 bit Vedic ALU

Table 1 Comparison of different arithmetic and logic unit operations

| S.No | Delay(in nanosecond) | | | |
|---|---|---|---|---|
| Addition | Conventional | Delay(ns) | Delay(ns) | Vedic |
| | Ripple Carry Addition | 7.535 | 7.336 | Vedic Addition |
| Multiplication | Wallace Multiplier | 14.187 | 11.586 | Vedic Multiplier |
| Subtraction(by 2's complement method) | Ripple Carry Subtraction | 7.535 | 7.336 | Vedic Subtraction |
| Division | Restoring Division | 34.268 | 34.100 | Vedic Division |
| Overall ALU | Conventional ALU | 34.707 | 34.168 | Vedic ALU |

Table 1 displays the comparison of synthesis results of various arithmetic operations in terms of delay(in nanoseconds). To show the efficiency of proposed *vedic* ALU at 16 bit level, it has been compared with conventional ALU. Addition using ripple carry scheme is less efficient when compared to applying *vedic* addition using vilokanam sutra in terms of delay and area. Subtraction using ripple carry scheme is less efficient when compared to applying *vedic* subtraction using vilokanam sutra in terms of delay and area. The efficiency of proposed *vedic* multiplier at 16 bit level has been compared with other popular multiplier structures and *vedic* multiplier showed lowest path delays. Similarly, the division using *vedic* sutra is more efficient as compared to that of restoring division method.

Now the comparative analysis of different arithmetic and logical operations are shown in fig 6

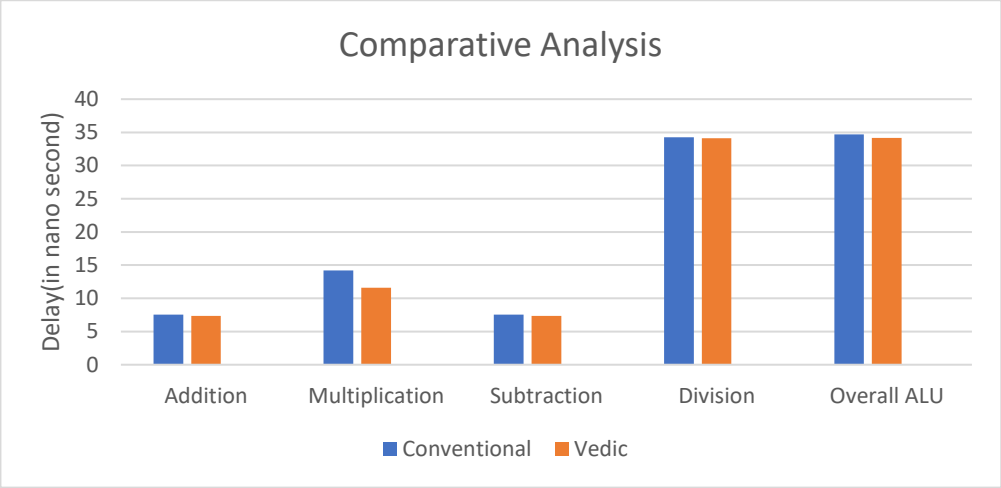


Fig.6 Comparative analysis of 16 bit Vedic and Conventional ALU

## Conclusion

Arithmetic and Logic Unit forms an important part of the digital system design and various architectures are proposed which reduces the area or the timing delay of the circuit in recent years. Design with *vedic* sutras is seen to be efficient in speed and delay in digital designs with respect to other logical circuits. Considering all the sutras discussed above, we can conclude that the *vedic* sutras based ALU observed as a promising technique in terms of speed, area and also might be in power also. The work can be further extended with the design of such *vedic* ALU with the help of *vedic* sutras. In this paper, a modified ALU is introduced using *vedic* sutras. *Vedic* technique reduces the propagation delay in processor and hence it reduce the hardware complexity in terms of area and memory requirement. This *vedic* ALU was coded in VHDL. The synthesis results indicated that the computation time delay for 16 bit *vedic* ALU was 34.168ns and 34.707ns for Conventional ALU.

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