Multilevel Inverter Topologies and Control Schemes: A Review

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ABSTRACT

The paper is devoted to the outlines of multilevel inverters and more in particular the form and function of topologies and recently used control schemes. In the recent years, the requirement of multilevel inverter is expeditiously increasing in the field of electrical energy utilization because the multilevel inverter is a key technology to integrate the renewable energy sources with the grid. Recently, various multilevel inverter topologies have been introduced which required a large number of power switches, gate drive circuit and voltage sources, as a result the complexity of the circuit, power losses and voltage stress on switch increases on the other hand the efficiency of the system reduces. The primary energy source can be for instance a battery, solar panel, fuel cell, generator etc. while the load can be anything from a motor to the connection with the power system. As will be shown with multilevel converters the number switch functions is increased, while increasing the power ratings with a switching frequency as close to the fundamental frequency. Multilevel converters provide and effective switching frequency increase allowing negligible filter requirements.

***Keywords*:**
Multilevel inverter, Selective harmonic elimination,

1. INTRODUCTION

Electricity is a convenient form of energy that can be channeled, simply controlled and distributed to a wide variety of distributed geographically dispersed consumers. There it is converted into other forms. Commonly electricity is controlled by varying parameters such as the voltage, current, frequency, impedance or combinations of these to adapt and control electrical energy, as provided by a primary energy source, to the characteristics of the load. This paper is about the dc-to-ac power conversion principles performed by so-called multilevel converters using solid state switching semiconductor devices [1]. A multilevel converter has been not only used for high voltage ratings, but also for medium-voltage applications such as motor drives, flexible ac transmission system (FACTS), traction drive systems and utility interface for renewable energy systems [2]. Multilevel inverters receive a lot of attention from both industry and academy. Recently, advances are made in the topological configurations of these converters by using floating energy sources such as capacitors, being an integral part of the switching process. This enabled the creation of a new path in the power electronics development for multipurpose power electronic converters connecting dc and/or ac sources and loads for low to very high power ratings. This paper will start with a short historical review, concerning commutations principles, the function of which is now embedded in solid state devices. Then the paper is mainly devoted by giving an example of topology synthesis starting from a basic commutation cell aiming at reaching higher power ratings and an optimized switching process. The techniques and principles discussed are a prerequisite to transfer the "static" electricity grid into a more dynamic controllable grid and/or loads as being controllable nodes in future grids. The main function of a multilevel inverter is given a desired output voltage from several levels of dc voltages as inputs [3]. A multilevel converter has been not only used for high voltage ratings, but also for medium-voltage applications such as motor drives, flexible ac transmission system (FACTS), traction drive systems and utility interface for renewable energy systems. Renewable energy systems such as photovoltaic module, wind turbine and fuel cell can be easily interfaced to a multilevel converter system for a high-power application. There are three well-known types of multilevel inverters as shown in Fig. 1.

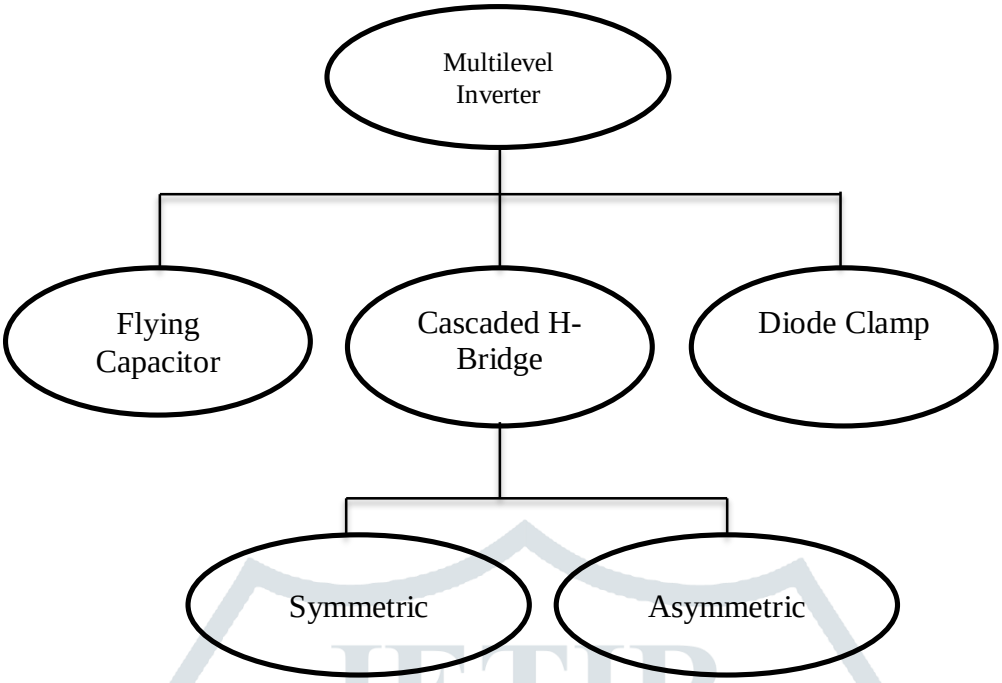

Figure 1. Classification of Multilevel Inverter

2. DIFFERENT TOPOLOGIES OF MULTI-LEVEL INVERTERS

Power electronic converters facilitate the flow of power between the source and the load. This is done by converting the voltage and current from one form to another through the utilization of power semiconductor switches in the power circuit that are controlled by a control unit [4]. The papers begins with a description on the fundamental concept of multilevel inverters including their advantages and drawbacks. Next, traditional multilevel inverter topologies are discussed before emerging topologies are presented. The various modulation techniques employed for these inverters are also provided before the current control techniques are explained.

2. 1. Diode-Clamped Multilevel Inverter

In 1980, the diode-clamped multilevel inverter was derived from the cascade inverter [5]. The first proposed diode-clamped inverter was a three-level inverter. The neutral point has been defined to be mid-level voltage; thus, the diode clamp inverter has another name: neutral point clamped (NPC) inverter as shown in Figure 2. The first implantation of this topology was done using pulse width modulation (PWM) [6]. Figure 2 shows a diode-clamped multilevel inverter with three and five levels.The diode-clamped inverter is noticeably characterized by the presence of clamping diodes [6]. For a three-phase m-level structure, the inverter generates line-to-line voltage waveforms with (2m – 1) steps. The inverter is typically supplied by one DC voltage supply V_{DC} which is then split by (m – 1) series connected capacitors. The voltage across each capacitor, which is defined as $V_{DC}/(m-1)$, can be tapped and connected to the inverter arm via power switches or clamping diodes [7]. Another issue with the diode-clamped inverter is the unequal loss distribution among the semiconductor devices. Several switches conduct longer than the others. As a result, these switches become hot earlier than the others. Therefore, for these switches, higher current rating and different cooling system are needed. Capacitor voltage balancing problem also poses a great challenge [8]. Additional circuit may have to be included to properly balance the voltage across each capacitor.

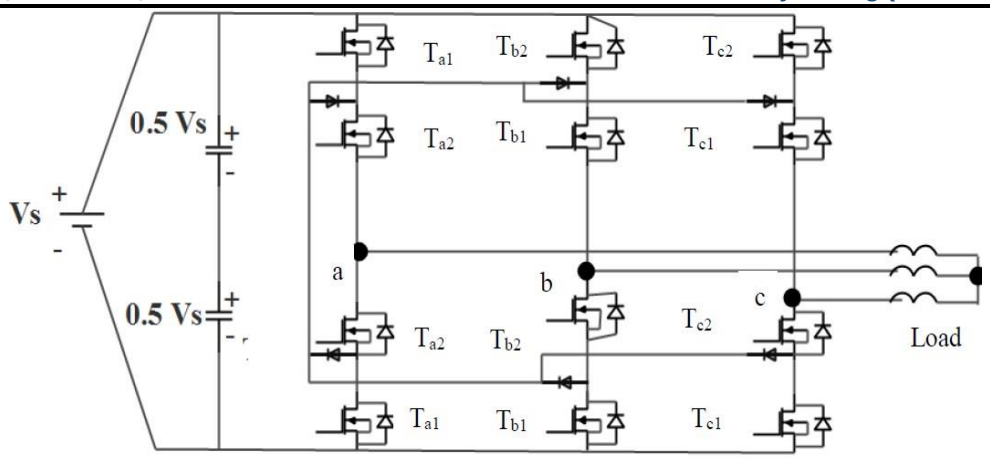

Figure 2. Three Level Diode Clamped Inverter Topology

The number of diodes increases quadratically as the number of levels increase, which makes it very difficult to build. Also, with high-voltage, high-power application, the reverse recovery time for the diode will be the major issue in the design, especially when it runs under PWM . Another disadvantage of the diode-clamped inverter is the lack of monitoring and control that makes the real power flow difficult in a certain inverter [7]. An advantage of the diodeclamped multilevel inverter is the presence of the capacitors, which allows a control for the reactive power flow. In addition, fundamental switching frequency will provide high efficiency because all the devices operate at low frequency.

2. 2. Flying-Capacitor Inverter

The flying-capacitor inverter does not require isolated DC sources and clamping diodes.
Nevertheless, these properties may be limited by flying capacitors' voltage unbalancing problem although the extra redundant switch combinations created by the flying capacitors can be exploited to tackle the unbalancing problem [9]. Unlike diode-clamped inverter, the flying-capacitor inverter is well recognized through the use of auxiliary capacitors known as flying capacitors in addition to the DC link capacitors. Another issue is that the flying capacitors are exposed to different voltage levels, similar to the blocking requirements of the clamping diodes. Therefore, several capacitors must be connected in series to divide equally the voltage stress across each capacitor [10]. As a result, a large number of flying capacitors are needed. For a three-phase m-level structure, the line-to-line voltage waveforms consist of (2m – 1) steps. The number of DC link capacitors required to divide the DC input voltage V_{DC} is (m – 1). Flying capacitors are used to clamp the switch voltage to one capacitor voltage level which is given by V_{DC} / (m −1). Figure 3 shows the Three Level Flying Capacitor Topology circuit diagram.

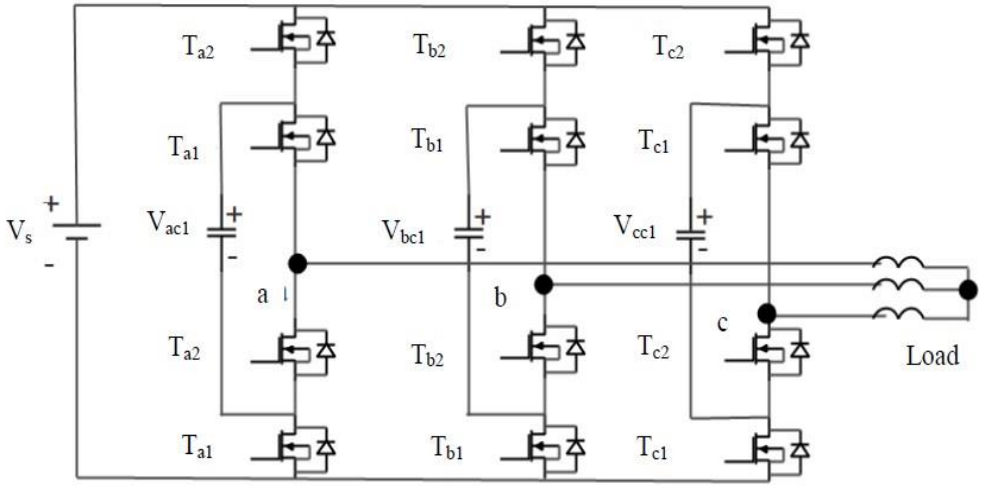

Figure 3. Three Level Flying Capacitor Topology

The large number of capacitors can provide large storage that gives extra time during a power outage and gets over voltage sags. However, the increment in the voltage levels will require a higher number of capacitors, which makes the inverter packaging very difficult and very expensive [11]. The capacitor-clamped multilevel inverter is a good option for the highvoltage DC transmission because the flow for both the real and the reactive power are controllable. On the other hand, in the real power transmission, the inverter requires a high switching frequency that increases the switching losses and control complexity [12].

2. 3. Cascaded H-Bridges Multilevel Inverter

The cascaded H-bridges inverter is the first MI based on semiconductors and was described and constructed by [13]. It was a cascaded topology, which is a serial connection of a one phase inverter. This MI is based on the series connection of single-phase H-bridge inverters with separate DC sources without clamping diodes or voltage capacitors [14]. Each bridge consists of four switches with their diodes—S1, S2, S3, S4—and one independent voltage source, "Vd." The voltage sources can include batteries, fuel cells, and solar cells. All the voltage sources have an identical voltage. Increasing the number of levels will smooth the output voltage signal and decrease the total harmonic distortion (THD). In addition, high and low couples of switching can be defined with respect to the voltage output direction. Considering with two bridges, the high output of one bridge is a shortcut to the low output of another one, resulting in a cascade connection between two bridges. Each bridge in the cascade adds two more levels to the output waveform. cascaded H-bridges inverter is illustrated in Figure 4. One of the main advantages is the number of the output voltage levels. The number of levels is more than twice the DC source (M = 2*S+1), where S is the number of DC sources. Another advantage from the production point of view is the modularization and packing of the series H-bridge, making it a quicker and less expensive process [7] . Also, it does not require additional clamping diodes or balancing capacitors such as those needed with other topologies. To increase the output voltage quality, more cascaded H-bridges cells must be used.

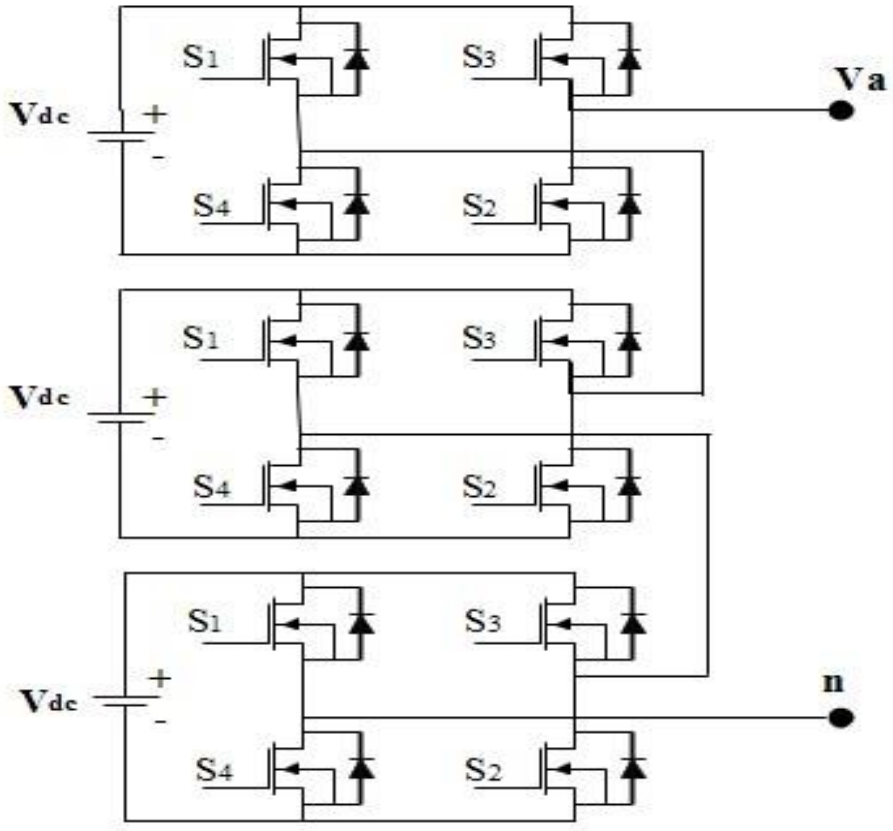

Figure 4. Single-Phase Structure of a Multilevel Cascaded H-Bridges Inverter

This increment in the number of cascaded H-bridges cells will increase the number of transistors used. A new topology has been developed to reduce the number of transistors that are used in the cascaded H-bridges inverter. This reduction has been accomplished by replacing some of the transistors with diodes, and it also reduces the total energy loss across the transistors [15].

2. 4. Emerging Topologies for Multilevel Inverter

Some of the concerns arising from the fact that the three classic multilevel inverters are lacking in certain areas, have contributed to the advent of new multilevel inverter topologies. Each of these new topologies was introduced to iron out some specific issues viewed from the perspective of the circuit's size and weight, overall cost, output quality, switching frequency, power loss, efficiency, reliability, device utilization, fault-tolerance capability and many more [16]. Most of these topologies were derived from classic multilevel inverters with some modifications. This section presents several topologies under this category which are also known as emerging topologies.

2. 4.1. Active Neutral-Point-Clamped Inverter

One of the main issues involving the diode-clamped or the NPC inverter is the unequal loss distribution among the power semiconductors in each inverter leg [17]. It was observed that the outer switches in the three-level neutral-point-clamped inverter conduct longer than the inner switches during a fundamental cycle. This requires the use of different heat sinks and cooling systems for switches that produce high and low losses. Besides, the maximum power rate, output current and switching frequencies have to be limited to a certain range [17]. A solution was proposed with the introduction of active NPC inverter [18]. This inverter uses clamping switches to replace the lamping diodes in the conventional NPC inverter. Figure 2.6 shows the active NPC inverter for a three-level structure. The clamping switches provide an additional path for the neutral current. There are two paths for the neutral current to flow to generate zero voltage level. If the current flows to the load, then the first path is through A3 and SA2, and the second path is through SA3' and the antiparallel diode of SA1'. Two paths can also be used if the current flows from the load. By forcing the current to flow in the two paths in the alternate manner through the appropriate control of SA2 and SA3', then the power loss distribution among the semiconductor devices can be properly adjusted. The NPC inverter obviously lacks this behavior since there is only one path for the neutral current to flow. Based on the three-level active NPC concept, a five-level structure has been derived by combining the three-level active NPC leg and the three-level flying-capacitor [19]. By having this combination, the strength of the NPC and the flying-capacitor inverters can be integrated in one superior topology. One leg of the five-level active NPC inverter. Despite the superiority shown in the active NPC topology in some aspects, the fact that the increase in the number of switches used may lead to a more complex control strategy. The use of flying capacitor cells also presents a challenge to balance the capacitor voltages [20].

2. 4.2. Modular Multilevel Inverter

Modular multilevel inverter is one of the next-generation multilevel converters intended for high- or medium-voltage power conversion without transformers [21]. This converter has attracted a lot of attention in recent years especially in the field of high voltage DC or HVDC transmission [22]. This inverter combines the elements of both the series-connected H-bridge converter and the flying-capacitor converter [23]. The converter consists of six arms in which every two of them forms one phase leg. Each arm is composed of a number of identical cells or submodules which are connected in series and an inductor. Half-bridge cells are typically used but full-bridge and clamp-double cells have also been proposed [24]. The inductor provides protection that limits the AC current in case of a short circuit at the DC side. For a half-bridge cell, two switching states can be generated. On state occurs when the upper switch is turned on and the lower switch is turn off which then lead to the cell output voltage to be equal to the capacitor voltage. Off state happens when

the opposite takes place which results in a zero cell output voltage. With a suitable number of cells connected in series, controlled by an appropriate switching scheme for the cells in the two arms per phase leg, a multilevel voltage waveform can be generated. As for the arm currents, they flow continuously and are not chopped [25].

2. 4.3. Mixed-Level Cascaded H-Bridge Inverter

Mixed-level cascaded H-bridge inverter is basically constructed from the combination of the cascaded H-bridge inverter with the other two classic multilevel inverters. This is realized by replacing the H-bridge cells with diode-clamped converter cells or flying-capacitor converter cells [26]. By having this arrangement, only six separated DC sources are needed as compared to 12 if the H-bridge cells are used. This accounts for a considerable reduction of 50% in the number of DC supplies. This saving is made possible since the flying-capacitor converter cells are of a five-level structure in contrast to the H-bridge cells of the three level structures. Nevertheless, the use of the five-level cells worsens the control complexity [27].

2. 4.4. Inverter Hybrid Multilevel Inverter

Like mixed-level cascaded H-bridge inverter, hybrid multilevel inverter is also introduced to basically reduce the number of separated DC supplies in the cascaded H-bridge inverter. Hybrid inverter integrates two different topologies into one that is expected to offer better characteristics and performance. By this definition, in the literature, some considered asymmetric and mixed-level cascaded H-bridge inverter as part of the hybrid inverter family and two different topologies are combined [28]. Through series connection, this inverter connects the three phase full-bridge circuit as the first stage to a single-phase H-bridge cell per phase leg, as the second stage. By doing so, one DC supply is sufficient to replace three separated DC sources in the first stage The second stage functions as an active filter that contributes to the enhancement of power quality and the reduction of common mode voltage [28-31]. To attain the desired number of voltage levels, the ratio of DC voltage of the first stage to that of the second stage is adjusted. Besides, unlike the symmetric or asymmetric cascaded H-bridge inverter that can only generate odd number of voltage levels, the hybrid inverter can also produce even number of voltage levels that may be necessary in some applications to achieve optimum device utilization [32]. In replacement of the six-switch full bridge circuit, the NPC inverter has also been employed in the first stage [33].

Table 1. Comparison Based on Number of Components if Different Levels Multilevel Inverters

Year	level	No. of Switch	No. of Capacitors	No. of Diodes	No. of Sources	Transformer	Reference
2018	9	9	-	-	2	N	Purposed
2018	5	6	1	-	1	N	[26]
2018	9	8	2	1	1	N	[27]
2018	9	12	2	-	1	N	[28]
2017	9	9	2	2	1	N	[29]
2017	7	7	1	2	2	N	[30]
2016	7	8	3	4	1	N	[31]
2016	9	10	2	-	2	N	[32]
2015	9	10	-	-	3	N	[33]
2015	7	8	-	-	3	N	[33]
2015	7	6	-	-	1	Y(1)	[34]
2018	19	12	-	-	2	Y(2)	[35]
2018	17	14	4	2	2	N	[36]
2018	17	12	-	-	4	N	[37]

2017	15	10	2	-	2	N	[30]
2017	15	10	-	-	5	N	[38]
2017	19	12	-	-	5	N	[39]
2016	25	24	9	-	6	N	[40]
2016	11	20	-	-	5	N	[44]
2015	11	10	-	-	4	N	[33]
2015	15	10	-	-	7	N	[41]
2015	15	12	-	-	3	N	[2]

3. DIFFERENT MODULATION TECHNIQUES FOR MULTILEVEL INVERTER

As multilevel inverters experience an increasing number of devices when the number of voltage levels grows, the level of complexity of modulation techniques also increases since more devices are needed to be controlled [34]. Most modulation techniques for multilevel inverters are adapted from the traditional methods employed for the conventional two-level inverters [35]. There are several ways to classify these techniques. One way of classification is by looking at the domain the modulation algorithms operate: the state-space vector domain that is based on the voltage vector generation, and the time domain that is based on the voltage level generation over a time frame as shown in Figure 5 [36]. Despite the complexity faced, the extra switching states generated provide flexibility in developing the modulation technique in order to achieve not only one particular target but also many desired criteria such as low harmonic contents, low switching loss, and voltage-balancing capability and so on. Another way of classification is by basing on the reference voltage type: the sampled reference, in which only the instantaneous reference amplitude is provided to the modulator, and the full-cycle reference, in which a sinusoidal output voltage is usually assumed, thus the amplitude, frequency and in some cases, the phase angle are provided to the modulator [37]. Besides the two ways of classification, the most common way mostly presented in the literature is the classification according to the switching frequency. 1-kHz boundary is usually used to differentiate between low and high switching frequency. Owing to the simplicity presented in defining the switching frequencies for easy understanding, this thesis describes the various modulation techniques based on their average operating switching frequency.

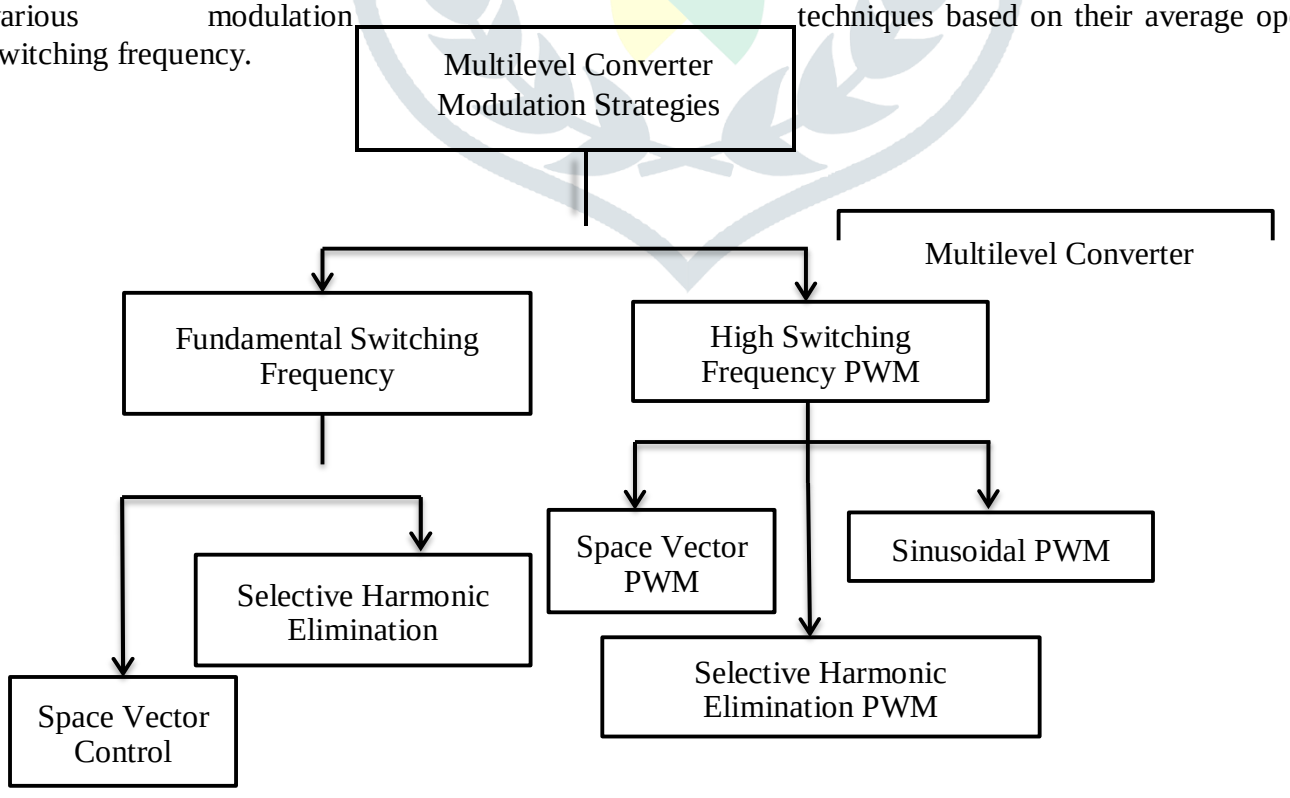

Figure 5. Modulation Strategies of Multilevel Inverters

3.1 Inverter Hybrid Multilevel Inverter

Low switching frequency is generally defined to be below 1 kHz. It is commonly observed that the range of the low switching frequency employed is up to few multiples of the fundamental frequency [38]. Low switching frequency methods are generally preferred for high power applications, owing to the switching loss reduction offered. The methods are also effective in cases in which a sufficiently high number of voltage levels are involved [39]. In this thesis, three low switching frequency methods mostly discussed in the literature are presented.

3.2 Selective Harmonic Elimination

Selective harmonic elimination (SHE) method is basically designed to eliminate undesired low order harmonics through the appropriate choice of the switching angles [39]. The process in determining the desired switching angles normally involves Fourier series analysis. Since these equations are nonlinear and transcendental, numerical methods such as Newton Raphson method is used [40]. Other methods have also been proposed such as those using genetic algorithms [41-43] and theory of symmetric polynomials and resultants [44-45]. Particle swarm optimization has also been applied to eliminate harmonics in a cascaded multilevel inverter with unequal DC sources [46]. The results obtained from solving the equations provide the optimum switching angles needed to eliminate the abovementioned harmonics. For practical implementation, the switching angles are usually pre-calculated and then stored in a look-up table. Since online calculations of switching angles are preferable in any real-time applications, an algorithm to carry out real-time calculation with any look-up table has been proposed [47]. To widen the modulation index range with low THD, a method known as optimized harmonic stepped waveform technique was proposed [48]. This method is an extension of the conventional SHE. The range of modulation index is divided into a number of levels. By introducing the modulation index levels, wide modulation index with low switching frequency and minimized harmonic distortion in the output waveform can be achieved. This technique has also been used with genetic algorithms to further improve the THD in a cascaded multilevel inverter with adjustable DC supplies [49-50].

3.3 Selective Harmonic Mitigation

The control objectives of this method are to follow voltage reference, to control the low order harmonic distortion and to reduce the switching losses. Using the sliding discrete Fourier transform algorithm, the objectives are successfully achieved with very low switching frequency. Since the technique is computed online, an improvement in the dynamic performance is also accomplished. Another technique which is similar to the SHM known as the optimal minimization of THD is also proposed. The main objective of this technique is to minimize the waveform THD with the proper selection of switching angles by reducing most of the harmonics without eliminating them completely [51]. The THD minimization process uses genetic algorithms to improve the output voltages with less THD has been proposed by [52]. Selective harmonic elimination technique is effective enough to fully remove a number of dominant low order harmonics that can significantly contribute to high harmonic distortion. However, the action of eliminating these harmonics somehow creates some side effects. It is reported that the elimination of the low order harmonics causes the harmonic energy to move to higher frequencies which results in the corresponding harmonic amplitudes to increase [5355]. This is not acceptable in some applications such as the grid-connected system. The increased awareness in the power quality of the grid has led to the introduction of more stringent grid codes that limit the amplitudes of the harmonics up to the 50th order. Although passive filters can be used to reduce the harmonic distortion into the grid, they are usually bulky and expensive. It is more convenient to use an efficient modulation method to obtain output waveforms that can meet the grid regulations. A method known as selective harmonic mitigation (SHM) was proposed in [56].

3.4 High Switching Frequency Methods

For high power applications, high switching frequency is considered to begin from 1 kHz. Modulation methods that employ high switching frequency are suitable for multilevel inverters with low number of voltage levels [57]. In the presence of high number of levels, these methods can also be applied but at the expense of increased complexity. Generally, the better output power quality and the higher bandwidth offered make the high switching frequency methods attractive for high dynamic range applications [58]. There are a number of methods that use high switching frequency in which some of the popular ones are explained in the following subsections.

3.5 Multicarrier PWM Methods

Multicarrier PWM method is basically derived from the classical sinusoidal PWM method. In this method, high frequency multicarrier signals are used and compared with a low frequency sinusoidal reference signal to generate the switching signals for the power switches [59]. There are two categories of multicarrier PWM that are characterized by the way the carriers are arranged. For a vertical arrangement of carriers in which each carrier is set in between two voltage levels, the category is known as level-shifted PWM [60-61]. Another category known as level-shifted PWM. Another category known as phase-shifted PWM arranges the carriers horizontally in which a phase shift is introduced between two carriers. Level-shifted PWM method is particularly suitable for diode-clamped inverter since each carrier signal can be easily related to each power switch [62].

4. CONCLUSIONS

The fact that the inverters are able to generate output voltages higher than the ratings of the individual semiconductor devices with reduced THD and harmonic contents make them a strong competitor to the traditional two-level inverters especially in the high voltage and high power applications. Three classic multilevel circuit topologies namely diode-clamped, flying capacitor and cascaded H-bridge inverters and they all have become the basis for the development of new multilevel topologies with improved characteristics and performance as well as less complexity to ease practical implementation. In tandem with the growth of multilevel inverter topologies, modulation methods for multilevel inverters have also witnessed a rapid progress. Many modulation methods of low and high switching frequency have been developed with various targets to achieve such as low harmonic contents, low switching loss, voltage-balancing capability, simplified implementation and so on. These techniques are basically an extension of the existing techniques employed for two-level inverters with some have to undergo a certain level of modifications to suit the multilevel characteristics.

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