FPGA Implementation of Discrete Wavelet Transform using Distributed Arithmetic Architecture For Image Compression

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Abstract: **The wavelet transform is an emerging signal processing technique that can be used to represent real-life non-stationary signals with high efficiency. Indeed, the wavelet transform is gaining momentum to become an alternative tool to traditional time-frequency representation techniques such as the discrete The lack of disk space seems to be a major challenge during transmission and storage of raw images, which in turn pushes the demand for an efficient technique for compression of images. Although, lot of compression techniques are available today, any upcoming technique which is faster, memory efficient and simple surely has the greatest probability to hit the user requirements. In this paper, we have developed wavelet-based image compression algorithm using well-known Distributed Arithmetic (DA) technique.**

Keywords: DA, FPGA, Discrete Wavelet Transform, Image Compression.

I. INTRODUCTION

The wavelet transform is an emerging signal processing technique that can be used to represent real-life non-stationary signals with high efficiency. Indeed, the wavelet transform is gaining momentum to become an alternative tool to traditional time-frequency representation techniques such as the discrete Fourier transform and the discrete cosine transform because Fourier analysis is ideal to analyze signals with stationary data, but is not suited for data with transients that cannot be predicted from data's past. By virtue of its multi-resolution representation capability, the wavelet transform has been used effectively in vital applications such as transient signal analysis, numerical analysis, computer vision, image compression, among many other audiovisual applications. Wavelet transform is capable of providing the time and frequency information simultaneously, hence giving a time-frequency representation of the signal. The wavelet transform breaks the signal into its "wavelets", scaled and shifted versions of the "mother wavelet". The discrete wavelet transform is computationally intensive and operates on large data sets. DWT is generally implemented by using FIR filters.
Finite impulse response (FIR) digital filters are extensively used due to their key role in various digital signal processing (DSP) applications. The complexity of implementation grows with the filter order and the precision of computation, real-time realization of these filters with desired level of accuracy is a challenging task. Several attempts have, therefore, been made to develop dedicated and reconfigurable architectures for realization of FIR filters in application specific integrated circuits (ASIC) and field programmable gate arrays (FPGA) platforms.

II. RELATED WORK

Lifting-based Discrete Wavelet Transform (DWT), a time/frequency analysis conversion method, used in JPEG2000

image compression systems is explained. Its filter bank has a dual-mode base function that consists of coefficients of 9/7 and 5/3. Generally, in the process of realizing Very Large Scale Integration (VLSI) architecture, there is a longer critical paths and increased cost of hardware, so paper proposes a folding and pipelined architecture to solve the problems in VLSI architecture design; In order to solve the problem of a large area of hardware due to the excessive use of the multipliers in dual mode operation, a shifter-adder-multiplier architecture and dual-mode filter architecture are combined. The experimental results show that the hardware architecture proposed in this work has a short critical path. The hardware supports dual mode hardware wavelet coefficients, decrease latency, and multiplierless, and more suitable for VLSI to implement and apply in low cost JPEG2000 compression systems.

Some paper presents the design and implementation of distributed arithmetic (DA) architectures of three-dimensional (3-D) Discrete Wavelet Transform (DWT) with hybrid method for medical image compression. Due to the separable property of the multi-dimensional Haar and Daubechies, the proposed architecture has been implemented using a cascade of three N-point one-dimensional (1-D) Haar/Daubechies and two transpose memories for a 3-D volume of N×N×N, suitable for 3-D medical imaging applications. The architectures were synthesized using VHDL and G-code and implemented on field programmable gate array (FPGA) single board RIO (sbRIO-9632) with Spartan-3 (XC3S2000). Experimental results and an analysis of the area, power consumption, maximum frequency, latency, throughput as well as the subjective test are discussed in this paper.

III. PROPOSED SYSTEM

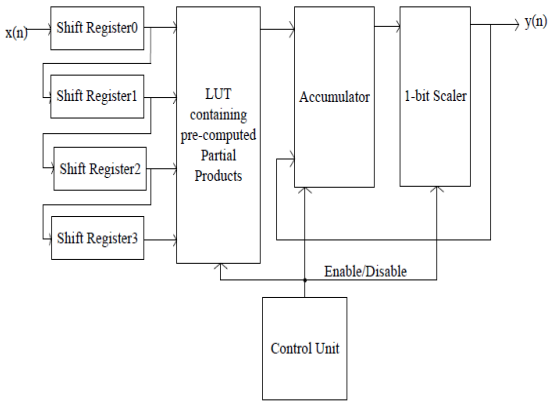


Fig System Block Diagram

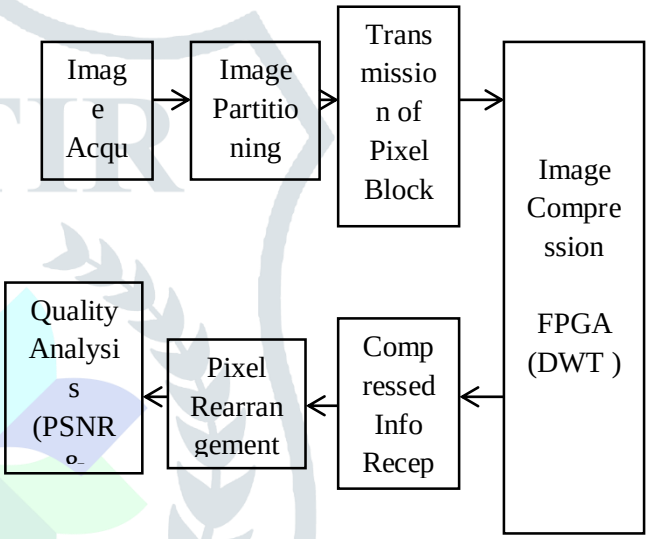


Fig Image Processing Steps

Our proposed system is as shown in above fig. The working of each component is given below: Matlab is responsible for creating the GUI and taking the input image from user After acquisition of image, it is divide into group or block of pixels of 4x4 or 8x8 Block of pixel is then sent to FPGA for data compression. Reconfigurable FPGA is performing the task by receiving input pixels and apply distributed arithmetic DWT on it and send processed dwt samples to pc.

IV. HARDWARE DESIGN

SPARTAN 3A FPGA

Introduction

Elbert V2 is an easy to use FPGA Development board featuring Xilinx Spartan-3A FPGA. Elbert V2 is specially designed for experimenting and learning system design with FPGAs. This

development board features Xilinx XC3S50A TQG144 FPGA. The USB 2.0 interface provides fast and easy configuration download to the on-board SPI flash. You don't need a programmer or special downloader cable to download the bit stream to the board.

Applications

• Product Prototype Development
• Home Networking
• Signal Processing
• Wired and Wireless Communications
• Educational tool for schools and universities

Board features

• FPGA: Spartan XC3S50A in TQG144 package
• Flash memory: 16 Mb SPI flash memory (M25P16)
• USB 2.0 interface for On-board flash programming
• FPGA configuration via JTAG and USB
• 8 LEDs ,Six Push Buttons and 8 way DIP switch for user defined purposes
• One VGA Connector
• One Stereo Jack
• One Micro SD Card Adapter
• Three Seven Segment Displays
• 39 IOs for user defined purposes
• On-board voltage regulators for single power rail operation Along with this, two items are required for this project which are-

USB Interface

The on board full speed USB controller helps a PC/Linux/Mac Computer to communicate with this module. Use a USB A to Mini B cable to connect with a PC. By default the module is powered from USB so make sure not to overcrowd unpowered USB hubs.

A high performance very low cost USB to UART interface allowing you to communicate with TTL serial devices such as microcontroller UART's using your PC. The module has a silicon labs CP2102 based device and a convenient pin header which includes a 5V and 3.3V supply. Tx and Rx data pins are at 3.3V TTL levels. Virtual COM port drivers are available for Windows, Mac, Linux, and Android operating systems.

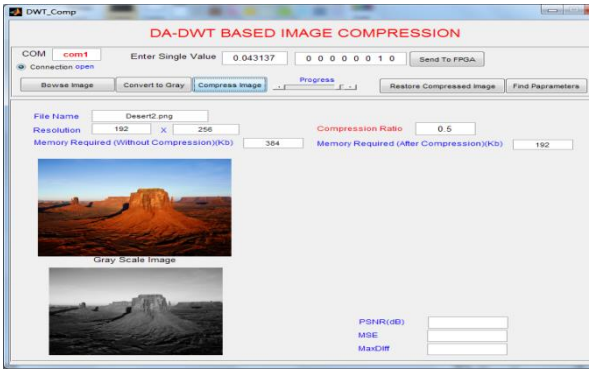
The CP2102 is a highly-integrated USB-to-UART Bridge Controller providing a simple solution for updating RS-232 designs to USB using a minimum of components and PCB space.

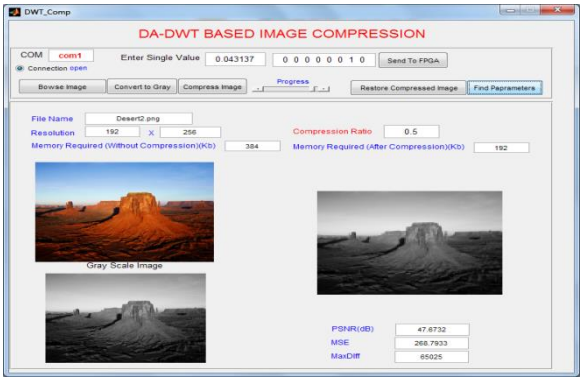
Fig . USB to serial converter

The CP2102 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) with full modem control signals in a compact 5 x 5 mm MLP-28 package. No other external USB components are required.

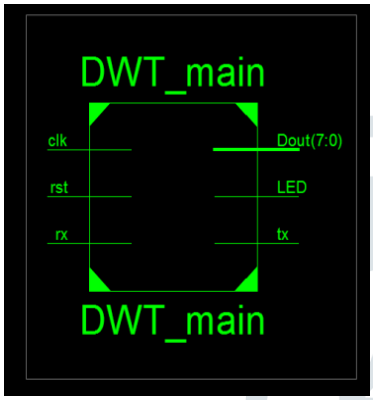
V. RESULT AND DISCUSSION

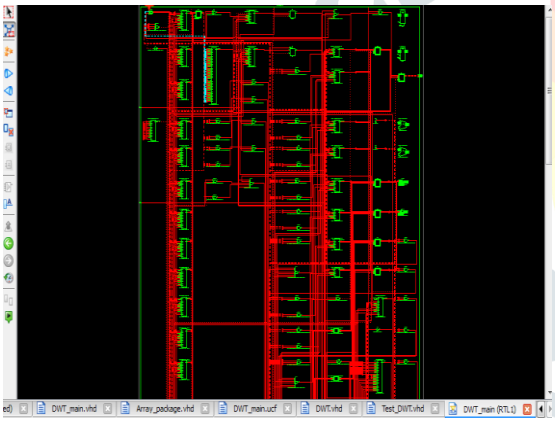
Matlab Simulation Results

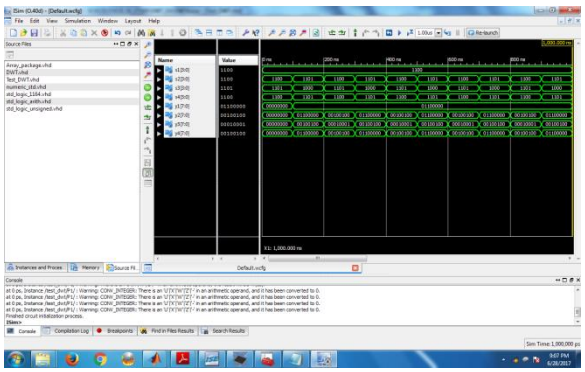




RTL Schematic







Test-Bench Waveforms

VI. CONCLUSION

A new mechanism is to perform a level-1 DWT without the use of high cost resources. Mechanism used reduces the power consumption by disabling certain blocks when computations are not needed for an efficient scheme of DAA. Throughput of system is lowered which makes it suitable for low speed applications, but low cost applications are usually the ones which are low speed applications. The level-1 DWT system can also be used recursively to produce further levels of DWT.

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