Review: Different designs of BCD Adder

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Abstract: Binary adder is the basic cell in any computation system. These binary adders are widely used in the ALU (arithmetic logic unit), DSP processors, in microprocessor for memory addressing computation etc. Here binary coded decimal (BCD) adder is explained and different design techniques are presented .This paper focuses on the different designs of BCD adder which are designed by different authors. All the designs are efficient in terms of area, power and the most important parameter delay.

***Index Terms* – Binary adder, BCD (binary coded decimal) adder, power, area.**

I. INTRODUCTION

Arithmetic unit is the most important component of modern embedded computer systems. In computing, Binary and decimal arithmetic operations are performed by arithmetic unit. The arithmetic unit is a basic building block which play vital role in performing operations of a computer. Very powerful and complex arithmetic units are used in the processors of current generations Cental Processing Units (CPUs) and Graphics Processing Units (GPUs).

Arithmetic unit generally includes floating point and fixed point arithmetic operations and trigonometric functions. The arithmetic unit which is used to perform complex operations will have long latencies and high power consumption. In electronics system, each digit in the decimal number can be represented in binary format using Binary Coded Decimal (BCD) encoding method. Decimal fractions cannot be represented by binary fractions, as they are pervasive in human activities. Extensive work has been done on building adders for BCD arithmetic and different adders have been proposed [9, 10, 11, 12]. Enhancing the speed of operation is still the major consideration while implementing BCD arithmetic which is being addressed in this paper. In arithmetic operations such as multi-operand addition [3, 4], multiplication [5] and division [6], adders form the core.

This paper introduces and analyses various techniques for high speed addition of higher order BCD numbers.

II. DESIGN OF THE 4-BIT BCD ADDER

BCD adder is used for packed binary numbers, in which every decimal digit is represented in 4bits. A BCD adder is a circuit that adds two BCD digits and produces a sum digit also in BCD This adder uses two 4-bit adder. These 4-bit full adders are basically Ripple Carry Adders (RCAs), where carry output of one full adder block is fed as the carry input for the next full adder. Besides that, for the purpose of forming the carry detection logic circuit, two AND gates and one OR gate have been used. Now, the full adder being the basic building block for designing the proposed 4-bit BCD adder, the proper selection of the 1-bit full adder cell becomes obvious. The design criteria of a full adder are actually multi-fold. Besides the transistor count which is one of the primary concerns, the two other important design criteria are the power consumption and the speed.

BCD numbers use 10 digits, 0 to 9 which are represented in the binary form 0 0 0 0 to 1 0 0 1, i.e. each BCD digit is represented as a 4-bit binary number. When we write BCD number say 5 2 6, it can be represented as 0101 0010 0110. Here, we should note that BCD cannot be greater than 9.The addition of two BCD numbers can be best understood by considering the three cases that occur when two BCD digits are added. By examining the three cases of BCD addition we can summaries the BCD addition procedure as follows:

1. Add two BCD numbers using ordinary binary addition.
2. If four-bit sum is equal to or less than 9, no correction is needed. The sum is in proper BCD form.
3. If the four-bit sum is greater than 9 or if a carry is generated from the four-bit sum, the sum is invalid.
4. To correct the invalid sum, add 0110 to the four-bit sum. If a carry results from this addition, add it to the next higher-order BCD digit.

Thus to implement BCD adder we require:

• 4-bit binary adder for initial addition
• Logic circuit to detect sum greater than 9
• One more 4-bit adder to add 0110 in the sum if sum is greater than 9 or carry is 1.The logic circuit to detect sum greater than 9 can be determined by simplifying the Boolean expression of given truth table.

As shown in the Figure 1, the two BCD numbers, together with input carry, are first added in the top 4-bit binary adder to produce a binary sum. When the output carry is equal to zero (i.e. when Sum <= 9 and Cout=0) nothing (zero) is added to the binary sum. When it is equal to one (i.e. when Sum >9 or Cout = 1), binary 0110 is added to the binary sum through the bottom 4-bit binary adder. The output carry generated from the bottom binary adder can be ignored, since it supplies information already available at the output-carry terminal.

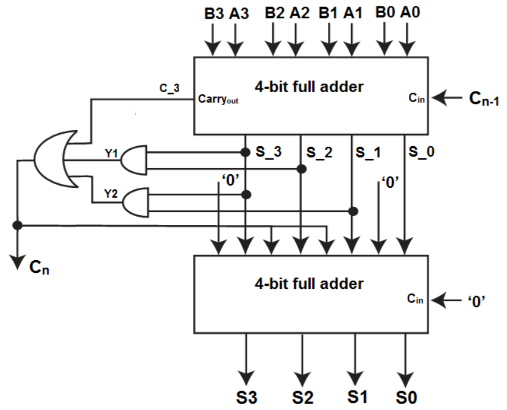

Figure 1.Conventional 4-bit BCD adder.

III. DIFFERENT TECHNIQUES OF BCD ADDER DESIGN

3.1Efficient Design of Reversible BCD Adder

This is the equivalent design of the approach shown in figure 1. Reversible BCD adder optimized for the number of reversible gates, memory usage and quantum cost. The design of BCD adder is shown in figure 8. In first part 4 MTSG gates are connected in series. It can Work as 4-bit binary adder produce sum and carry [2]. Second part is equivalent design of over 9 detection unit and correction unit [8].

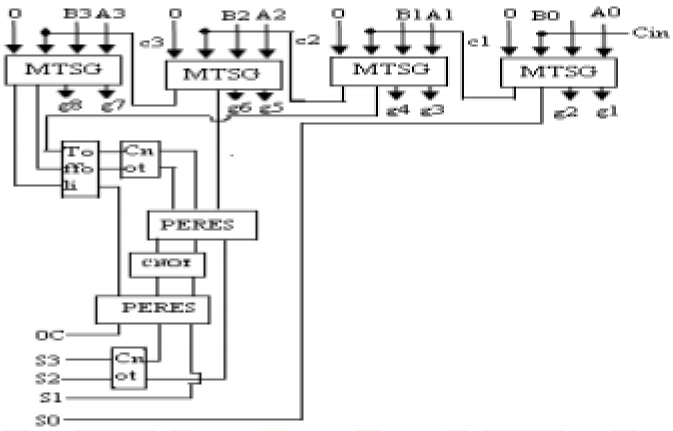

Figure 2. Reversible BCD adder

3.2A Low-Voltage, Low-Power 4-bit BCD Adder, Designed Using the Clock Gated Power Gating, and the DVT Scheme

Moreover, the concept of multiple channel length technique has also been utilized in the proposed architecture. For the conventional CMOS technology, the multiple channel length technique is known to be one of the popular means by which we can reduce the Leakage Power [29]. As per the technique, the channel length of the transistors used in a circuit can be increased, wherever it is needed to control the leakage current. On the other hand, wherever it is required to maintain the performance (specially, for the transistors in critical path), we need to increase the width of the transistors [29].

For the proposed design, the effective sizing of the sleep transistors and the transistors used in transmission gates has been done using this technique. From the block level representation of the proposed 4-bit BCD adder (as shown in Fig. 4), it can be seen that the CLK1 and CLK2 are the two different clock signals which actually used for the purpose of Power Gating.

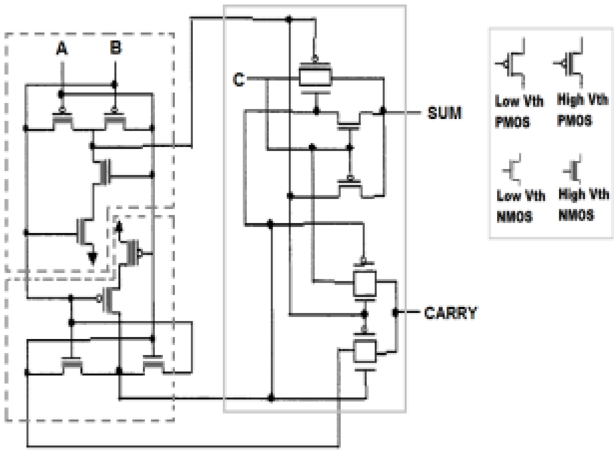

Figure 3. 16 transistor 1-bit full adder, modified with DVT scheme

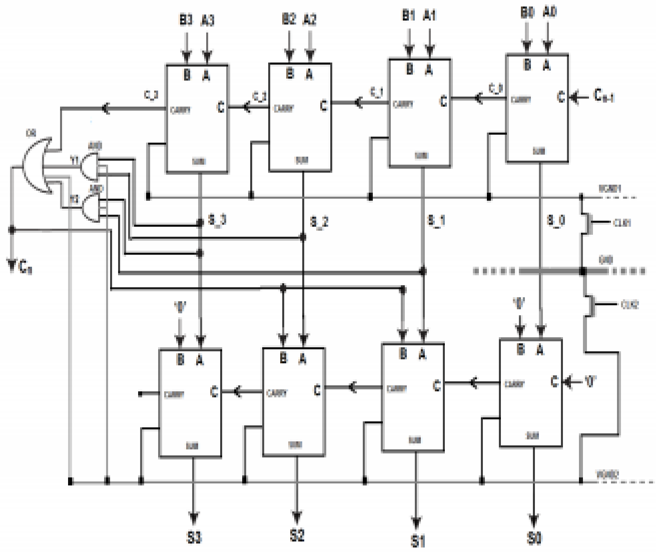

Figure 4. Block diagram of the proposed 4-bit BCD adder design

3.3High Speed BCD Adder

The conventional BCD adder is very simple, but also very slow due to the carry ripple effect. If the BCD addition is analyzed carefully, we see that there are three cases:

Case 1: The sum of two BCD digits is smaller than 9. In this case, it is certain that there is no carry output even if there is a carry input. Furthermore, the result for this digit does not require a correction.

Case 2: The sum of two BCD digits is greater than 9. In this case, a correction is required. Moreover, a carry output is produced regardless of the carry input.

Case 3: The sum of two BCD digits is exactly 9. In this case, the input carry determines whether a correction is required and whether a carry output is produced.

For the first two cases, the incoming carry has no effect on determining the carry output; therefore, the carry output can be determined without knowing the existence of the carry input. On the other hand, if the addition result is 9 (Case 3), then the input carry determines the existence of the carry output, which may ripple even up to the most significant digit. Therefore, Case 2 and Case 3 can be represented by a digit generate (DG) and a digit propagate (DP) signals, respectively.

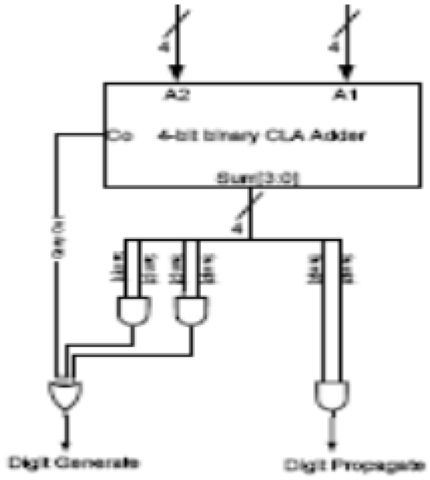

Figure 5 Adder and Analyzer Unit

Figure 5 shows how the DG and DP signals of a digit are computed in our design. After having all the DG and DP signals, the output carry for each digit can be found easily by Equation 1.

$$\text{Output Carry}=DG+DP \cdot \text{Input Carry} \quad (1)$$

Due to the nature of this equation, we can form DP by ANDing only Sum [0] and Sum [3] instead of using all bits of Sum[3:0]. The DG and DP signals can be utilized similar to the generate and propagate signals used in a binary CLA circuit. Therefore, all schemes developed for a binary CLA can be used in order to speed up carry computation. The carry value for each digit is computed inside the Carry Network using Equation 1. The Carry Network can be any type of parallel prefix network or two level carry look-ahead logic can be used instead. The carries computed by Carry Network are used in the correction step. Figure 4.3 shows the complete BCD adder including the 4-bit adders used for correction. Correction is done by adding 0, 1, 6, or 7 to the binary sum coming from the first level adder. For each digit, the existence of the output carry and the input carry determine the value to be added for correction

The carry value for each digit is computed inside the Carry Network using Equation 1. The Carry Network can be any type of parallel prefix network or two level carry look-ahead logic can be used instead. The carries computed by Carry Network are used in the correction step. Figure 6 shows the complete BCD adder including the 4-bit adders used for correction. Correction is done by adding 0, 1, 6, or 7 to the binary sum coming from the first level adder. For each digit, the existence of the output carry and the input carry determine the value to be added for correction.

The Value added for correction	Possible Cases	
	Input Carry from prev. digit	Output Carry from next digit
0	0	0
6	0	1
1	1	0
7	1	1

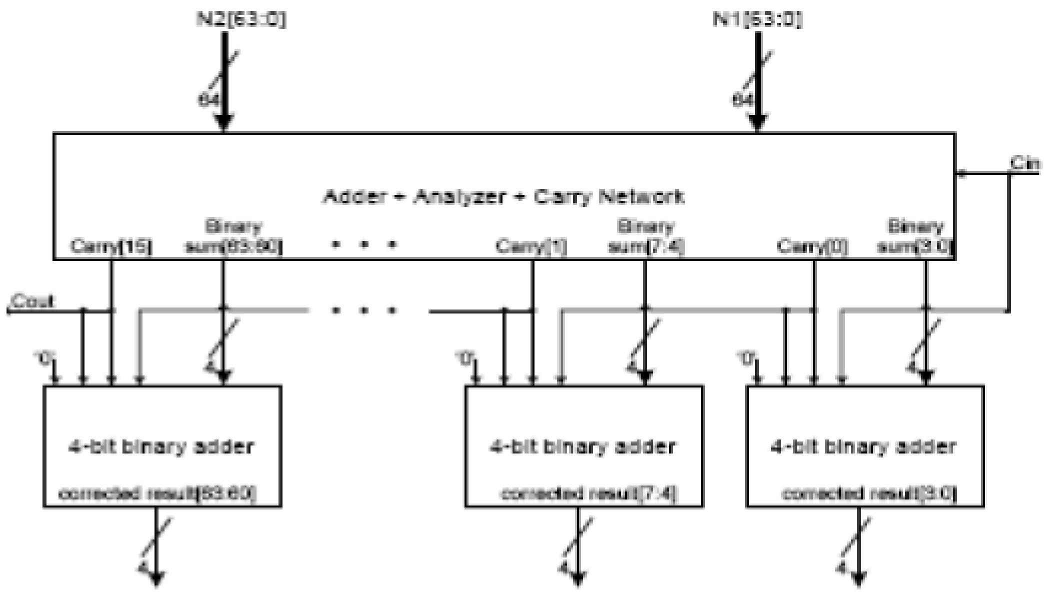

Figure 6.High Speed BCD Adder

IV. RESULTS AND DISCUSSION

4.1 Results of Reversible BCD Adder

This design is implemented on Xilinx tool. Here no of gates will define the area of the adder.

Table 4.1: Simulation results of Reversible BCD Adder

BCD Adder	No. of slices	No. Of gates	Delay (ns)
Conventional BCD Adder	9	36	12.15
Reversible BCD Adder	6	10	11.22

4.2 Results of Reversible BCD Adder

4.2 Results of BCD Adder Using the Clock gated power gating and DVT Schme

	Conventional 4-bit BCD adder	4-bit BCD adder with DVT (without Power Gating)	Proposed 4-bit BCD adder	Unit
Average Power	3.722× 10-6	1.668× 10-6	1.384× 10-6	Watt
Delay	11.440× 10-11	19.229× 10-11	16.181× 10-11	Second
(Average Power × Delay)	42.588× 10-17	32.077× 10-17	22.394× 10-17	Joule

4.3 Results of BCD Adder

	Adder	Delay(ns)
1.	Conventional BCD Adder	231.377
2.	Reduced Delay BCD Adder	103.649

Conclusion:

The 4-bit BCD adder is designed with different design technique using different tools. Different designs gives different delays .the delays are 11x10-11.

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