A Highly Reliable Differential Dual Buck-Boost Inverter for single phase and three phase applications

FARHEEN BEGUM
M.Tech Student
P.D.A College of Engineering, Kalaburagi 585102,

CHANDRASEKHARA.SEREGARA
Assistant Professor,
P.D.A College of Engineering, Kalaburagi 585102.

Abstract—In this paper, we present selective harmonic elimination PWM strategy for single and three phase differential dual buck- boost inverter. Due to the switching technique adapted in this work, the switching and conduction losses are reduced as the body diodes are made ineffective and also as the switches operates at high frequency only for the half cycles. Switching cell is made up of MOSFETs instead of IGBTs due to its better performance. The simulation work is carried out for single phase and three phase differential dual buck-boost inverter and its performance is noted.

IndexTerms—**IGBT, MOSFET, buck-boost inverter, switching cell, switching and conduction losses.**

I. INTRODUCTION

The most frequently used voltage source inverter(VSI) can perform only buck function while current source inverter(CSI) can perform boost function. Due to this, a dc-dc converter is used for voltage control.

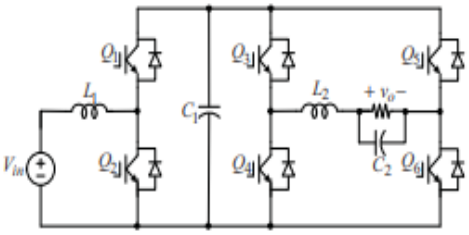

Fig.1: cascade structured inverter

But it results in less efficiency and also the cost, size and weight are increased. A step up transformer is used and same issues prevailed. Coupled inductors replace the normal inductors present in previous types of inverters in order to reduce current ripples and also the commutation issues get solved.

Switching cells are introduced to avoid the parasitic inductances and dead time minimization and the boost or buck ratio can be changed by varying the number of cells connected. A selective harmonic elimination PWM technique is used to eliminate the circulating current due to switching cells without using coupled inductors & hence efficiency is improved.

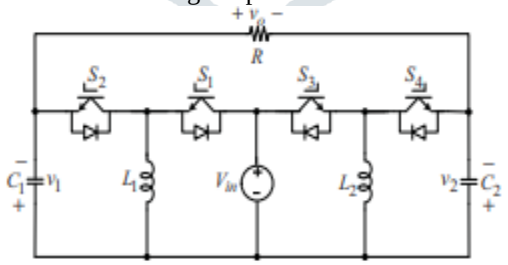

Fig.2: Differential dual buck boost inverter

Then, the single stage dc-ac buck or boost inverters are introduced. Due to the reduction in number of switches, size and cost was reduced. But in this, due to overlap time of pulses for complementary switches caused by EMI or improper gating pulses, current shoot-through problem arises.

In this paper, we are proposing single and three phase differential dual buck boost inverter by arranging the structure of the switching cells in a manner, which avoids the current shoot through issue as the current is forced to flow through the inductors. Also we propose a SHE-PWM strategy by which only two switches will operate on high frequency at any given instant of time which in turn reduces the switching and conduction losses.

II. OPERATION OF PROPOSED DIFFERENTIAL INVERTER

The single phase topology of the proposed differential dual buck-boost inverter is depicted in Fig.3.

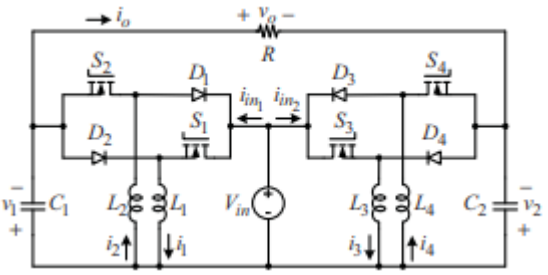

Fig.3: Proposed single-phase differential dual buck-boost inverter

The voltage across the capacitors C_1 and C_2 are V_1 and V_2. Let d_1 and d_2 are the duty ratios for the switch $S_1$and S_2.

In positive half cycle,

$$V_1 = \frac{-V_{in}d_1}{1-d_1} = 0$$

$$V_2 = \frac{-V_{in}d_2}{1-d_2} = A\sin(\omega t - \pi)$$

In negative half cycle,

$$V_1 = \frac{-V_{in}d_1}{1-d_1} = A\,sin\,\omega t$$

$$V_2 = \frac{-V_{in}d_2}{1-d_2} = 0$$

From the above equations, we can find d_1 and d_2 which is as follows:

For positive half cycle,

$$d1=0$$

$$d_2 = \frac{A\sin(\omega t - \pi)}{A\,sin(\omega t - \pi) - V_{in}}$$

For negative half cycle,

$$d_1 = \frac{A\sin\omega t}{A\,sin\,\omega t - V_{in}}$$

$$d2=0$$

The following figure.4 provides the modes of operation of the proposed differential buck boost inverter:

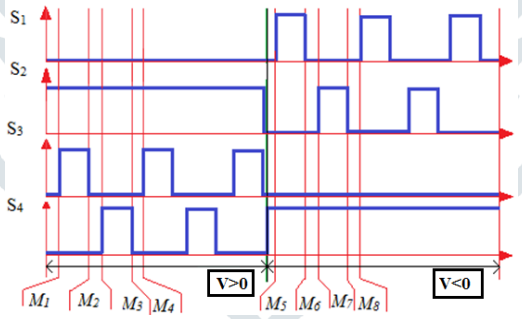

Fig.4: Modes of operation

Mode 1: In this mode, S_2 and S_3 are ON where S_1 and S_4 are OFF. C_2will discharge to the load through D_2 and S_2. The voltage across the inductor L_3 is equal to input voltage.

Mode 2 & 4: In this mode, S_1, S_3 and S_4 are OFF where S_2 is ON. C_2 still discharged to the load through D_2 and S_2. The diodes D_2, D_3 and D_4 are in forward bias.

Mode 3: In this mode, S_2 and S_4 are ON where S_1 and S_3 are OFF. C_2 will discharge to the load through D_2 and S_2.

The same will occur for the negative cycle and the above four modes gets repeated. Here in these modes, the capacitor C_1 will discharge to the load through S_4 and D_4.

III. DESIGN PARAMETERS FOR PROPOSED DDBBI

The parameters needed for the design of proposed inverter circuit can be calculated by using the following relations:

The equation for duty ratio, D is given below:

$$D = \frac{V_c - V_{in}}{V_o}$$

The inductor ripple current is calculated from the following equation:

$$\Delta I_L = 0.2 * \frac{V_o}{V_{in}} * I_o$$

The inductor value can be calculated with the following equation:

$$L = \frac{V_{in} * D}{\Delta I_L * F_s}$$

The capacitor value can be calculated with the following equation:

$$C = \frac{I_o * D}{\Delta V_c * F_s}$$

IV. SIMULATION SETUP & RESULTS

The models of proposed single phase and three phase inverters were designed using MATLAB/Simulink software. The ratings of proposed inverters are tabulated in the following table 1:

TABLE I
Ratings of the propose inverter

Parameters	Values for single phase	Values for three phase
Input voltage	37V	220V
Load voltage	230V	440V
Output Power	800W	19kW
Switching Frequency	50kHz	50kHZ
Inductors	0.12mH	203mH
Capacitors	22µF	150µF

The simulation circuit for the single phase differential dual buck-boost inverter is depicted in Fig.5.

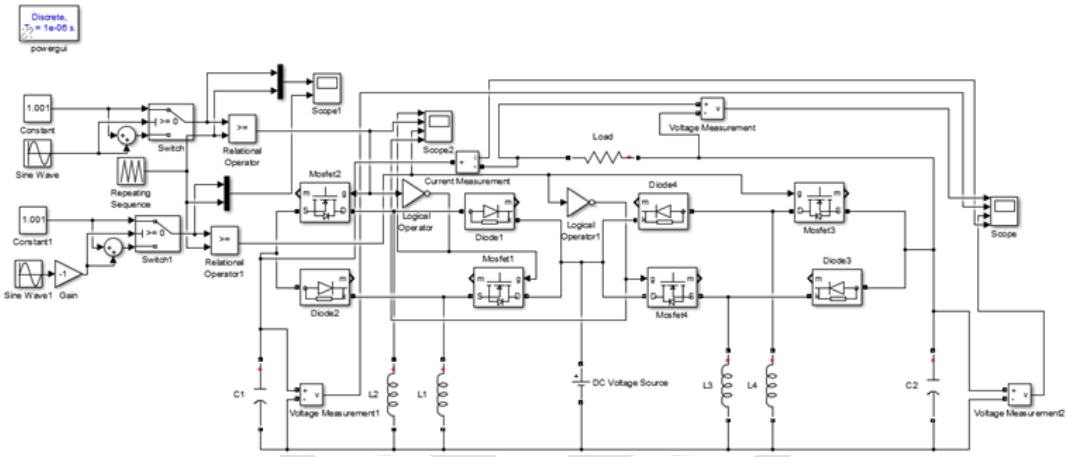

Fig.5:Simulation diagram of 1ϕ Differential inverter

The waveforms of the pulses are given in the following Fig.6.

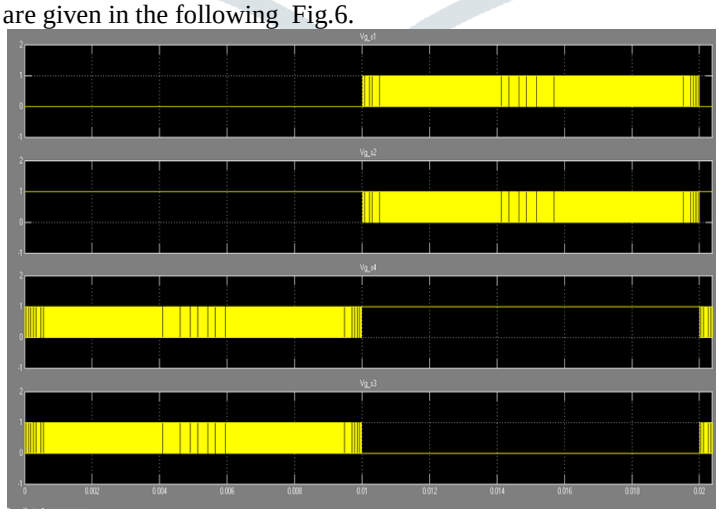

Fig.6: Pulses of 1ϕ Differential inverter

Here, we got high frequency (50KHz) pulses for half cycle and low frequency (50 Hz) pulses for next half cycle. At any given instant of time, only two switches are subjected to high frequency pulses which will reduce the switching losses on other two switches.

The capacitor voltage and the load voltage waveforms are shown in Fig.7.

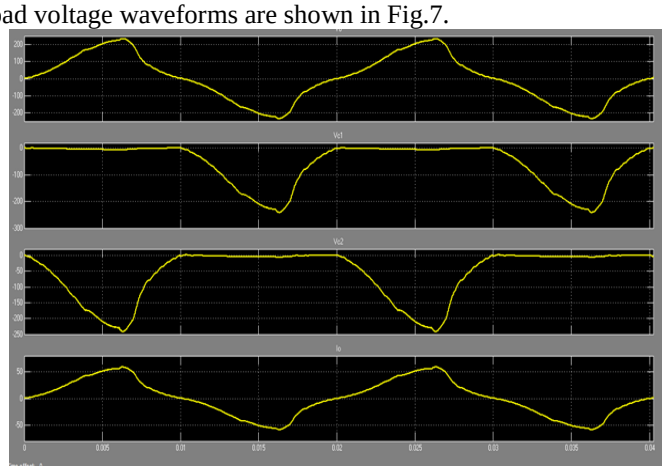

Fig.7: Capacitor and load voltage waveforms

In this Fig.7 we can see that the load voltage is the difference between the capacitor voltages. While C2 is discharging, C1 will gets charged and when C2 is charging, C1 gets discharged.

The three phase circuit for simulation is shown below Fig.8

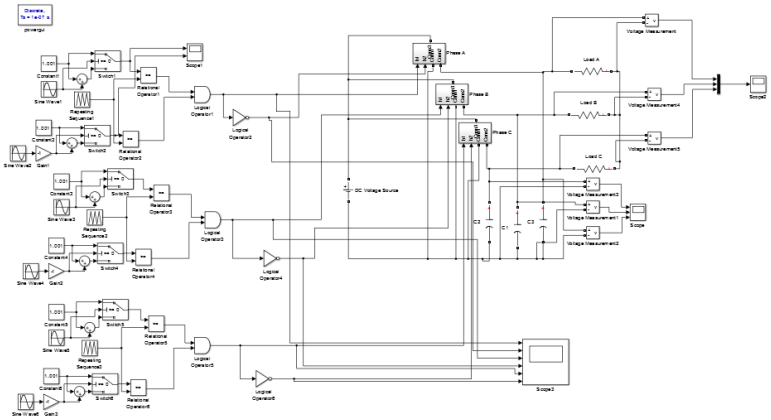

Fig.8: Simulation diagram of 3ϕ Differential inverter

The pulses for the three phase differential inverter are shown below Fig.9:

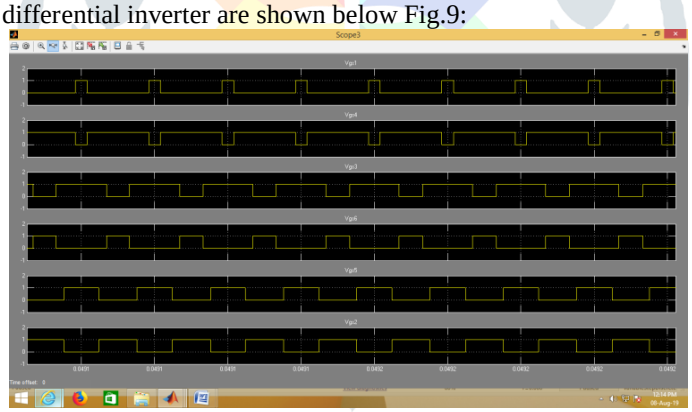

Fig.9: Pulses of 3ϕ Differential dual buck-boost inverter

The capacitor voltages for the three phase differential inverter are shown in Fig.10.

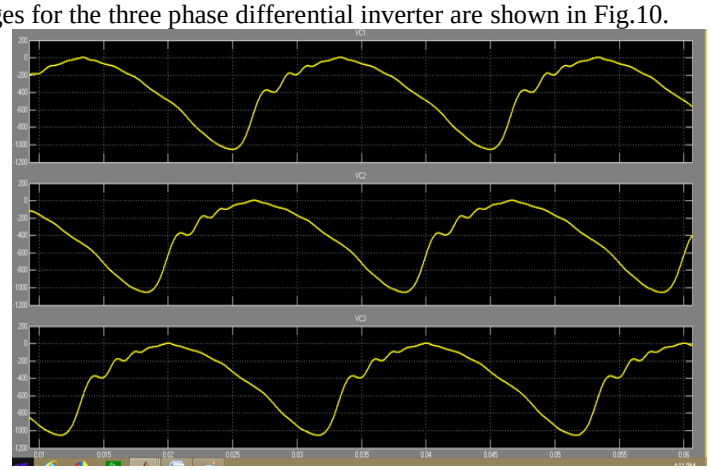

Fig.10: Capacitor voltage waveforms for 3ϕ Differential inverter

In the above Fig.10 we can see the capacitor voltages and from the difference between those capacitor voltages each phase voltage can be verified which is shown in the following waveforms.

The three phase load voltage is provided below Fig.11.

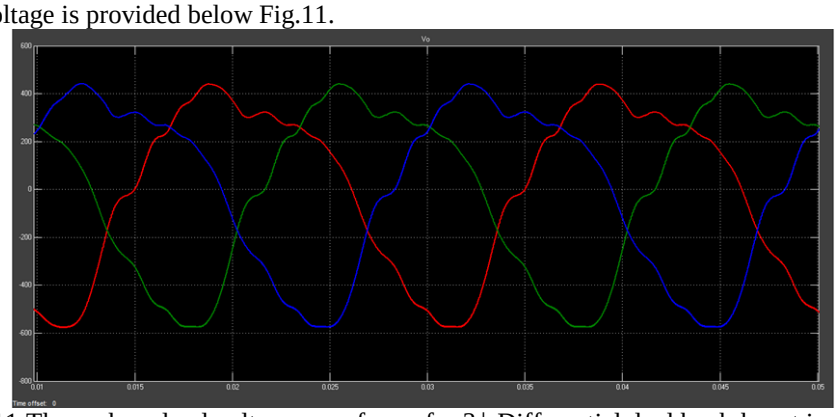

Fig.11:Three phase load voltage waveforms for 3ϕ Differential dual buck-boost inverter

VI. CONCLUSION

A selective harmonic elimination PWM strategy for single phase differential type buck boost inverter is designed and implemented for simulation. Due to the switching technique adapted in this work, as the switches operate at high frequency only for the half cycles, the conduction and switching losses are greatly reduced and efficiency is improved. Proposed model is designed with power MOSFETs which increases its reliability. The simulation work is further extended to three phase inverter and its performance is noted.

REFERENCES

1. F. Akbar, H. Cha, A. A. Khan and H. G. Kim,"**A Highly reliable and efficient differential type Buck-Boost DC-AC converter,"** IEEE Trans. pp.1791-1796, 2017.
2. A.A. Khan, H. Cha, H. F. Ahmed, **"High-Efficiency single phase AC-AC converters without commutation problem,"** IEEE Trans. power electron., vol. 31, no. , pp. 5655-5665, Aug. 2016.
3. A. Khan, H. Cha, and H. F. Ahmed, "**An improved single-phase direct PWM inverting buck-boost ac-ac converter,**" IEEE Trans. Ind. Electron., vol. 63, no. 9, pp. 5384-5393, Sep. 2016.
4. O. Ray, and S. Mishra, "**Boost derived hybrid converter with simultaneous DC and AC outputs,**" IEEE. Trans. Ind. App., vol. 50, no. 2, pp. 1082-1093, Mar/Apr. 2014.
5. J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L G. Franquelo, P. W. Wheeler, M. A. Aquirre, **"Selective Harmonic Mitigation Technique for Cascade H-Bridge Converters With Nonequal DC Link Voltages,"***IEEE Trans. Ind. Electron.*,vol. 60, no. 5, pp. 1963-1971, May 2013.
6. R. R. Errabelli, and P. Mutschler, "**Fault-tolerant voltage source inverter for permanent magnet drives,**" IEEE Trans. Power Electron., vol. 27, no. 2, pp. 500-508, Feb. 2012.
7. P. W. Sun, C. Liu, J.-S. Lai, and C.-L. Chen, "**Cascade dual buck inverter with phase-shift control,**" IEEE Trans. Power Electron., vol. 27, no. 4, pp. 2067-2077, Apr. 2012.
8. Y. Xue, L. Chang, S. B. Kjar, J. Bordonau, and T. Shimizu, "**Topologies of single-phase inverters for small distributed power generators: An overview,**" IEEE Trans. Power Electron., vol. 19, no. 5, pp. 1305-1314, Sep. 2004.
9. R. O. Caceres, W. M. Garcia, and O. E. Camacho, "**A buck-boost DCAC converter: operation, analysis, and control,**" in Proc. IEEE International Power Electronics Congress (CIEP), Oct. 12-15, 1998, pp. 126-131.
10. R. O. Caceres and I. Barbi, "**A boost dc-ac converter: analysis, design and experimentation,**" in Proc. IEEE IECON'95 Conf., Orlando, FL, Nov. 5-11, 1995, pp. 546-551.