Simulation and Analysis of Various Levels of Diode Clamped Multilevel Inverter

J. Hemalatha, Sr. Assistant Professor,
PVP Siddhartha Institute of Technology, Vijayawada
Dr. Basavaraja Banakara, Professor,
Davanagere University, Davanagere.

***Abstract*—Diode Clamped Multilevel inverters (DCMLI) are the most widely used topology of multilevel inverters in high-power applications up to several megawatts. This paper presents the basic operation of single phase and three phase diode clamped multilevel inverter from 5 level to 15 level. A MATLAB simulation has been carried out and the results are presented.**

***Index Terms*—Diode Clamped Multilevel Inverter, Total Harmonic Distortion.**

I. INTRODUCTION

Recently, for increasing use in practice and fast developing of high power devices and related control techniques, multilevel inverters have become more attractive to researchers and industrial companies. Multilevel inverters have achieved an increasing contribution in high performance applications.

At low voltage, there is a single topology that dominates the market, the voltage source two level inverter. However, at medium and high voltages, the situation is completely different. A wide variety of topologies share the market and the applications of industrial MV drives [1]. In effect, for High power applications, it is possible to use direct converters (cycloconverters) or indirect converters (with current or voltage dc link).

The continuous development of high-voltage insulated-gate bipolar transistors (IGBTs) and integrated-gate commutated thyristors (IGCTs) and the application of these power semiconductors in several multilevel voltage-source converter (VSC) topologies have led to a drastic increase of the nominal voltage and power ratings of self-commutated converters in recent years.

The different multilevel inverter structures are diode clamped, flying capacitors and cascaded H-bridge multilevel inverters [1]-[4]. Increasing the number of levels in the inverter without requiring high ratings on individual devices can increase the power rating [5].

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S. B. Author, Jr., was with Rice University, Houston, TX 77005 USA. He is now with the Department of Physics, Colorado State University, Fort Collins, CO 80523 USA (e-mail: author@lamar.colostate.edu).

T. C. Author is with the Electrical Engineering Department, University of Colorado, Boulder, CO 80309 USA, on leave from the National Research Institute for Metals, Tsukuba, Japan (e-mail: author@nrim.go.jp).

Among the high-power converters the Diode Clamped Multilevel Inverter is the most widely used in all types of industrial applications [6-9], in the range of 2.3 to 4.16 kV, with some applications up to 6 kV.

This paper presents a comparison of Total Harmonic Distortion for single phase and three phase cascaded multilevel inverter starting from 5-level to 15-level(odd only). This paper is organized as follows. Circuit topology and working principle of diode clamped multilevel inverter is explained in section II. Simulation results for single phase and three phase inverter are discussed in section III. Finally, conclusions and future trends are presented in section IV.

II. DIODE CLAMPED MULTILEVEL INVERTER

A. Basic Operation

An m-level diode-clamp converter typically consists of m-1 capacitors on the dc bus and produces m levels of the phase voltage. Fig. 1 shows a three-phase full bridge five-level diode-clamp inverter in which the dc bus consists of four capacitors, C_1 C_2 C_3 and C_4. For a dc bus voltage V_{dc} the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$, through clamping diodes.

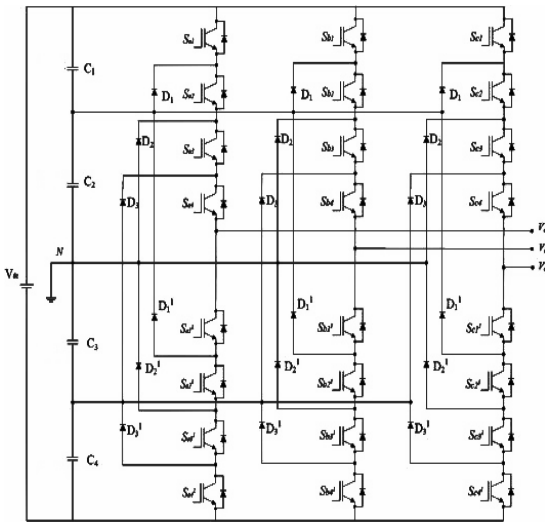


Fig. 1 Three Phase 5 level diode clamped multilevel inverter

T the neg tage reference point. Using the 5-level converter shown in Fig. 1 as an example, there are five switch combinations to synthesize five level voltages across a and 0.

(1) For voltage level $V_{a0}=V_{dc}$ turn on all upper switches S_{a1} through S_{a4}.

(2) For voltage level $V_{a0}=3V_{dc}/4$, turn on three upper switches S_{a2} through S_{a4} and one lower switch S_{a1}^1.
(3) For voltage level $V_{a0}=V_{dc}/2$ turn on two upper switches S_{a3} and S_{a4} and two lower switches S_{a1}^1 and S_{a2}^1.
(4) For voltage level $V_{a0}=V_{dc}/4$, turn on one upper switches S_{a4} and three lower switches S_{a1}^1 through S_{a3}^1.
(5) For voltage level $V_{a0}=0$, turn on all lower half switches S_{a1}^1 through S_{a4}^1.

Table I lists the voltage levels and their corresponding switch states. State condition 1 means the switch is on, and 0 means the switch is off. Notice that each switch is only switched once per cycle. There exist four complimentary switch pairs in each phase. The complimentary switch pair is defined such that turning on one of the pair switches will exclude the other from being turned on. Using phase-leg a as the example, the four complementary pairs are (S_{a1}, S_{a1}^1), (S_{a2}, S_{a2}^1), (S_{a3}, S_{a3}^1) and (S_{a4}, S_{a4}^1).

TABLE I
DIODE-CLAMP 5-LEVEL CONVERTER VOLTAGE LEVELS AND THEIR CORRESPONDING SWITCH STATES

Output V_{ao}	Switch States							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}^1	S_{a2}^1	S_{a3}^1	S_{a4}^1
$V_1=0$	0	0	0	0	1	1	1	1
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_5=V_{dc}$	1	1	1	1	0	0	0	0

Fig. 2 shows phase and line voltage waveforms of the example 5-level converter. The line voltage consists of a positive phase-leg a voltage and a negative phase-leg b voltage. Each phase voltage tracks one-half of the sinusoidal wave. The: resulting line voltage is a 9-level staircase wave. This implies that an m-level converter has an m-level output phase voltage and a (2m-l)-level output line voltage.

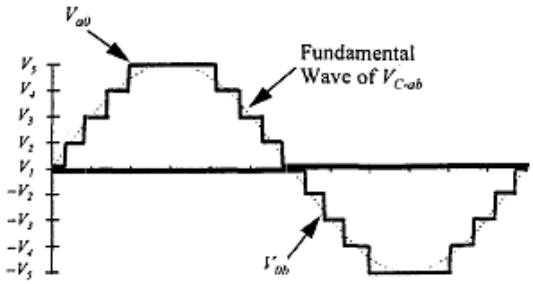


Fig. 2 Phase and line voltage waveforms of a 5-level diode-clamp voltage source inverter.

B. Advantages

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Efficiency is high because all devices are switched at the fundamental frequency.
- Reactive power flow can be controlled.
- The control method is simple for a back-to-back intertie system.

C. Disadvantages

- Excessive clamping diodes are required when the number of levels is high.
- It is difficult to do real power flow control for the individual converter.

D. Analysis

A 9- level output line voltage waveform of single phase cascaded H bridge multilevel inverter is shown in Fig. 2. For an output voltage waveform that is having quarter-wave symmetry with s steps of generally equal magnitudes $V_1 = V_2 = V_3 = \ldots = V_{DC}$, its Fourier Series expansion is given by

$$V(\omega t)=\sum_{m=1,3,5,\ldots}^{\infty}\frac{4V_{DC}}{m\pi}\left(\cos(m\theta_1)+\ldots..+\cos(m\theta_N)\right)*\sin(m\omega t) \quad (1)$$

Where N is the number of switching angels and m is the harmonic order.

The THD of a signal is the ratio of the sum of powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency, and it can be obtained by

$$\%THD=\frac{100}{U_1}\sqrt{\sum_{h=2}^{\infty}U_h^2} \quad (2)$$

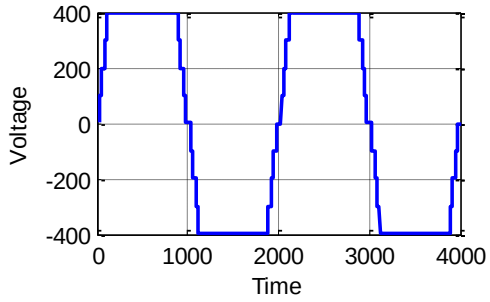
Where U_1 is the first harmonic of the signal analyzed, h is the harmonic order and U_h is the harmonic that presents order h.

III. SIMULATION AND RESULTS

This paper presents the comparison of THD for single phase and three phase diode clamped multilevel inverter starting from 5- level to 15- level. Both single phase and three phase DCMLI are implemented in MATLAB/SIMULINK. An IGBT with a diode is selected as a bidirectional switch. The DC input voltage of the inverter is 400V. The frequency of output voltage is 50Hz. Output voltage waveforms are observed across a resistive load.
These inverters are simulated at 0.06seconds. TableII. show the rms, maximum and THD of single phase diode clamped multilevel inverter for 5-, 7-, 9-, 11-, 13- and 15- levels. It can be observed that as the number of levels increases THD decreases. Output voltage waveforms and THD of single phase diode clamped multilevel inverter are shown in Fig. 3 and Fig. 4 respectively.

TABLE II. SINGLE PHASE CASCADED H BRIDGE MULTILEVEL INVERTER

Sl. No.	LEVEL	Output Voltage(rms)	Fundamental voltage(max)	THD
1	5	367.2	494.5	28.08%
2	7	352.9	480.4	20.63%
3	9	337.5	461.4	13.79%
4	11	321.5	438.1	8.25%
5	13	304.8	411	7.18%
6	15	313.1	424.6	6.73%



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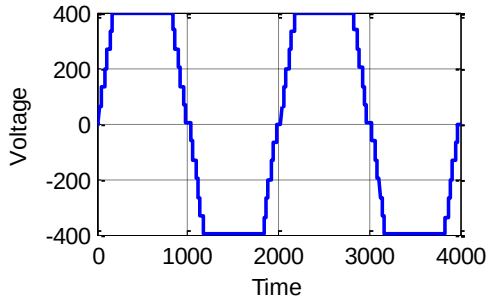

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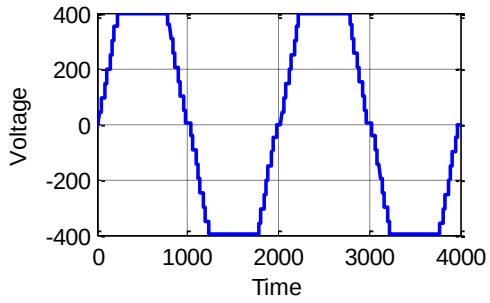

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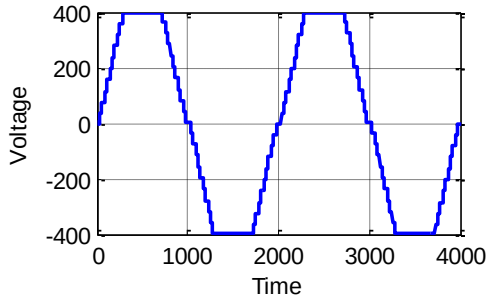

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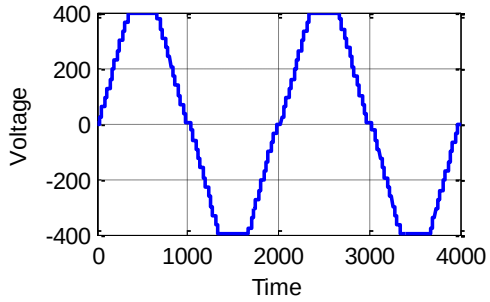

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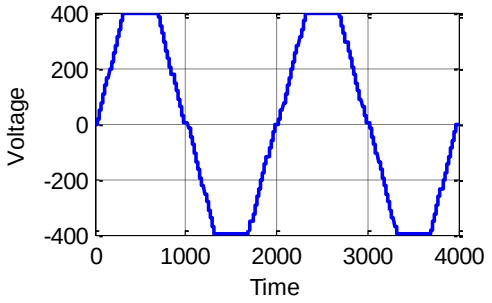

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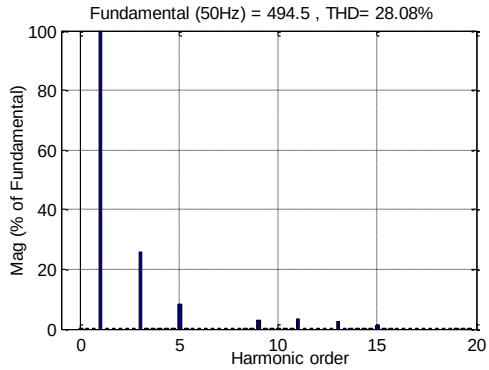
Fig. 3 Output voltage waveforms of single phase diode clamped multilevel inverter
(a) Five level, (b) Seven Level (c) Nine Level
(d) Eleven Level (e) Thirteen Level (f) Fifteen Level



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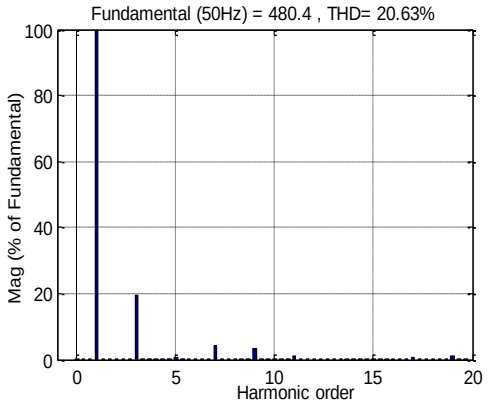

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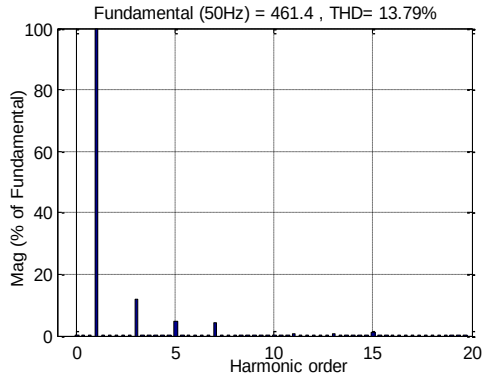

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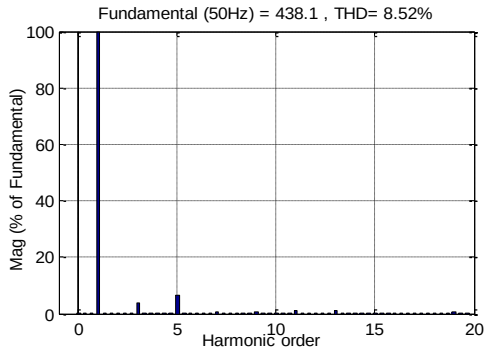

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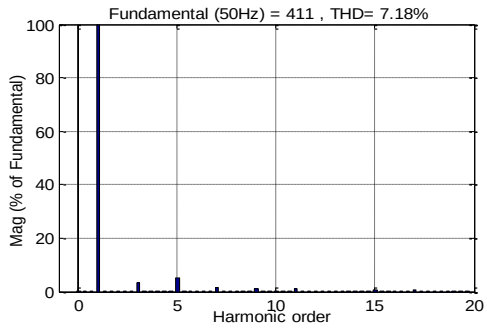

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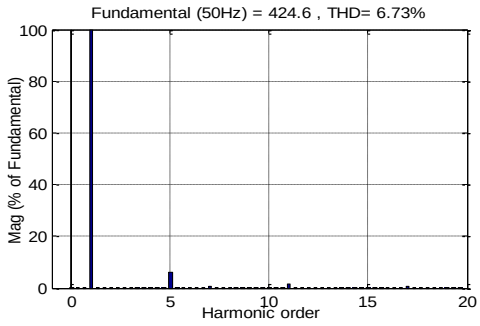

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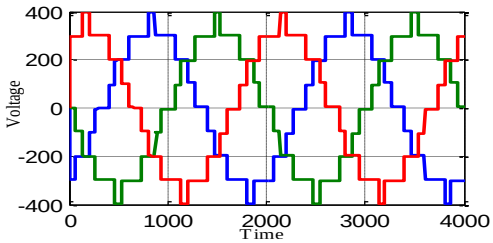
Fig. 4 THD of Single Phase DCMLI
(a) Five level, (b) Seven Level (c) Nine Level
(d) Eleven Level (e) Thirteen Level (f) Fifteen level

TableIII. gives the rms, maximum and THD of Diode Clamped Multilevel inverter for 5-, 7-, 9-, 11-, 13- and 15-levels. Fig. 5 shows the three phase output voltage waveform of three phase Diode Clamped multilevel inverter. Input DC source applied to inverter is of 100V. Switches are triggered at regular intervals. Switches of leg B and leg C are triggered at 120^0 and 240^0 phase delay respectively with respect to phase A. THD of three phase cascaded H bridge inverter is shown in Fig. 6

TABLE II. THREE PHASE CASCADED H BRIDGE MULTILEVEL INVERTER

Sl. No.	Level	Output Voltage(rms)	Fundamental voltage(max)	THD (Vab)
1	5	251.6	340	13.72%
2	7	290.2	393.1	8.79%
3	9	308.2	419.2	6.02%
4	11	309.8	421.9	6.10%
5	13	307.9	421.9	5.86%
6	15	311.4	424.2	6.91%



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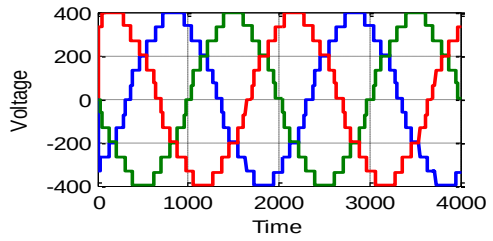

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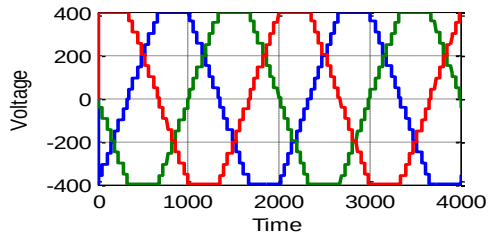

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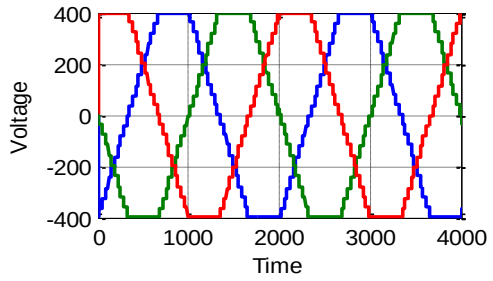

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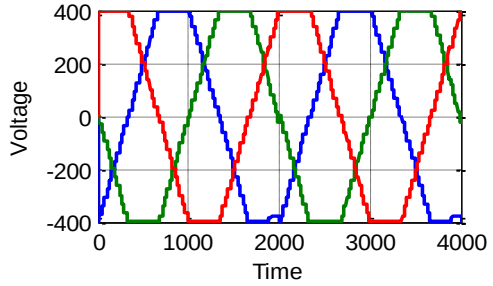

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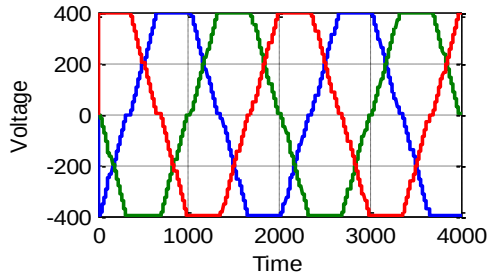

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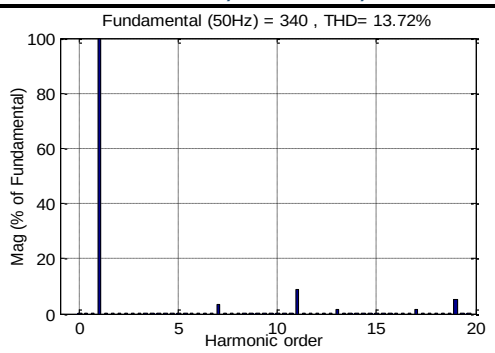
Fig. 5 Output voltage waveforms of three phase diode clamped multilevel inverter



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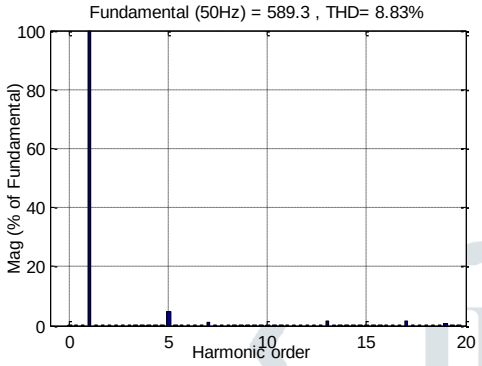

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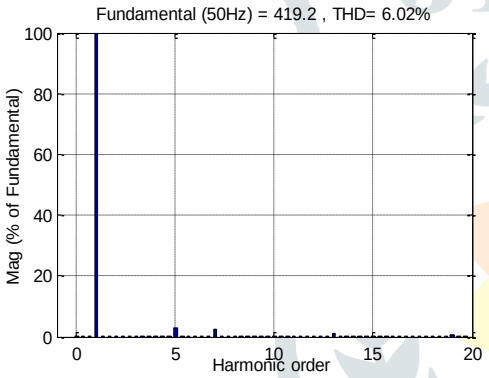

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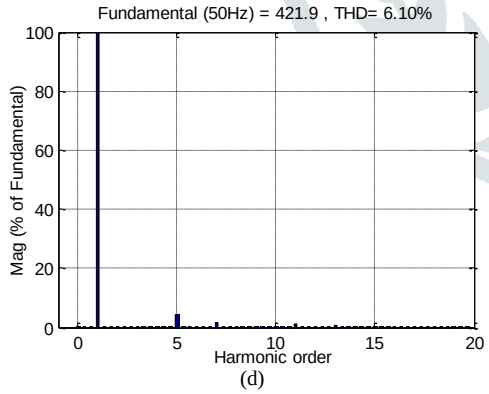

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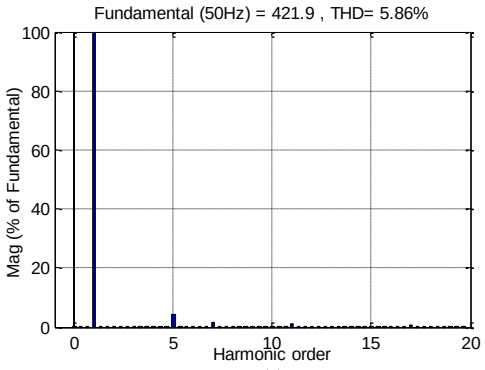

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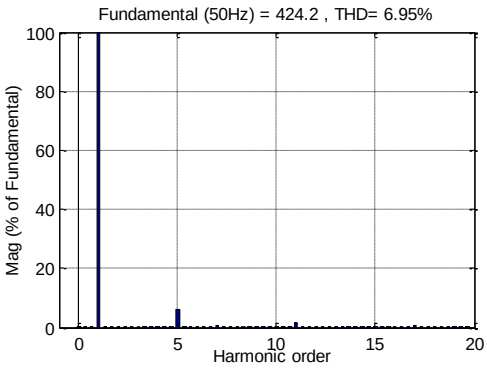

(f)

Fig. 4 THD of Single Phase DCMLI
(a) Five level, (b) Seven Level (c) Nine Level
(d) Eleven Level (e) Thirteen Level (f) Fifteen Level

Table IV. gives the comparison of THD for single and three phase diode clamped multilevel inverter. It can be observed that the THD reduced by using the three phase cascaded H bridge inverter also by increasing the number of levels.

TABLE IV. COMPARISON OF THD

LEVEL	THD	
	Single phase	Three phase
5	28.08%	13.72%
7	20.63%	8.79%
9	13.79%	6.02%
11	8.25%	6.10%
13	7.18%	5.86%
15	6.73%	6.91%

IV. CONCLUSIONS AND FUTURE SCOPE

This paper presents the comparison of THD 5-, 7-, 9-, 11-, 13- and 15- level single phase and three phase diode clamped multilevel inverter. The results show that as the number of levels increases the THD reduced in single phase inverter and further reduced by choosing three phase inverter.

To generate the pulses lot of computations are required, as the switches are triggered at regular intervals. This can be avoided by applying the PWM techniques for multilevel inverters in future. THD can be further decreased by applying the PWM methods.

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