Utilization of Low Power Linear-Phase FIR Filter or Reconfigurable Applications

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Abstract: **In multiplier less FIR filter, tremendous effects came into existence to minimize the adders which are present in the multiplier block, for the sake of reducing total area of chip and consumption of power. If the adder's quantity in multiplier block is less in number then there is no need to minimize the power consumed in a FIR circuit. Here comes a power oriented method of optimization in a linear phase finite impulse response filter used in our system. In search of discrete coefficient algorithm, we use the power index which has the average adder depth in structural adders. The existing systems techniques uses transposed form configuration, the drawback are less efficiency and area complexity. Instead the adders search of coefficients pairs which minimizes adders, in order to get coefficients pair that reduces the AAD addition adder depth of SA's structural adders. By using stable and reconfigurable applications they are developed to find discrete coefficient. As a result, area complexity reduces with increases performance and high efficiency is obtained .XILINX system generator toolbox is required for circuit implementation.**

IndexTerms - Transposed form FIR, multiple constant multiplication (MCM), Low power, block processing, VLSI.

I. INTRODUCTION

FIR filter which acts as a frequency selective network, which is used in modifying the input signal in order to facilitate further processing in DSP systems. FIR digital filters are used in some applications of DSP systems; such as, speech processing, cancellation of echo, and various applications including software defined radio. Many of these applications require FIR that has higher orders to meet certain frequency criteria. In digital communication which is in high speed these FIR filters should support higher sampling rate. The no of multipliers adders which are required for output of filter will increase rapidly with respective with the filter order. The nodes will have up to some extent battery power. To extend or to increase the lifetime of a network these batteries should be used in order to increase the life time of a network. The energy consumption of each node-will vary with its communication

State: transmitting, receiving, listening or sleeping modes. Scholars are working on thesis principle to increase the nodes battery lifetime. Whereas for deciding the node that should select for communication. We use routing algorithm as it plays a vital role in energy efficiency. In signal processing applications filter coefficients remain constant very often. This features realization of multiplication. Finite impulse response filters is having two maintain the coherences of the specifications, configurations, known as transposed form and direct form FIR filter.

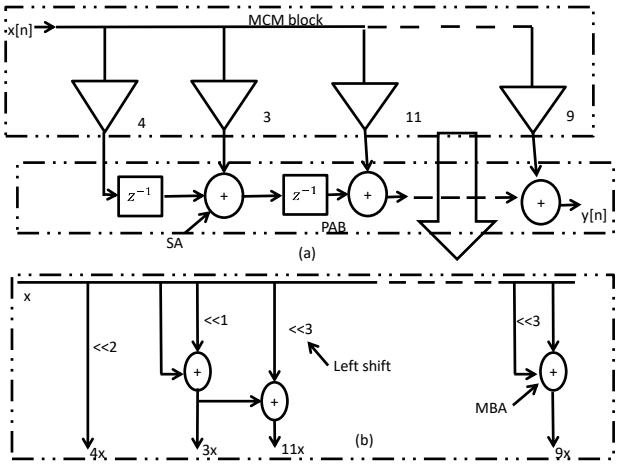

Fig.1 (a) transposed direct form FIR structure
(b) Shift-add implementation of the MCM block

For efficient realization of FIR filter several design are made to be designed by researcher. To store pre computed results we use lookup tables (LUT's) in DA based design. The transposed FIR in fig.1 needs only N delay units, N represents order of filter. By back pedaling the numerator and denominator sectors orders in direct form we can obtain this structure. Hence once can identify that the both delay columns which taps the centers and can be merged as they are redundant. The drawback of the transposed form is it increases the possibilities of arithmetic overflow for FIR filter which is high and resonance can be increased. In this paper, we realize the possibility of block FIR filter in transposed form configuration to take the benefit of MCM method and pipelined for delay and area. The main contributions of this paper are as follows:

1. The computational performance analysis of transposed FIR and deriving of flow graph with reducing register complexity.
2. In transposed FIR filter block processing is used.
3. For reconfigurable applications we design transpose FIR filter block.
4. Using MCM technique for block implementation of Fixed FIR filter low complexity method is designed.

II. EXISTING SYSTEM

In the previous paper we have used multiple constant multiplication algorithms MCM. It is an arithmetic operation like addition, subtraction, multiplication and shifting. But in this paper we have used multiplier less multiple constant multiplication algorithms to decrease the area complexity of the chip. The regular structure of the transposed form FIR filter is not changed just we can change multiplier block. In the place of multiplication we have used shifting. From a circuit Fig.2, MCM dominates the complexity of the whole category of linear time invariant (LTI) system like FIR filters to be implemented, MCM must avoid costly multipliers. The hardware alternative must be multiplier less, i.e. using only additions, subtractions and shifting. In this project we have used left shifting it can be compared to the multiplier because we have to show the difference between the performance of FIR filter by using multiplier and multiplier less MCM algorithms. The computational complexity of MCM is conjectured to be NP-hard. Because of increasing the demand in high – speed and low-power design MCM algorithm is most preferable to obtain the low power optimization designs. It has so many advantages compared to the existing MCM algorithms. But coming to my project I want to analyze to find the parameters like area, delay and dynamic power. The upper-depth (AD) and average (Avg) are known with exact analytic formulas.

$$\mathbf{AAD} = \frac{\mathbf{1}}{\boldsymbol{N}} \sum_{\boldsymbol{i}=\mathbf{1}}^{\boldsymbol{N}} \boldsymbol{AD}(\boldsymbol{i})$$

Where AD (i) is the adder depth of i^{th} interval
N no of iterations of adder depth

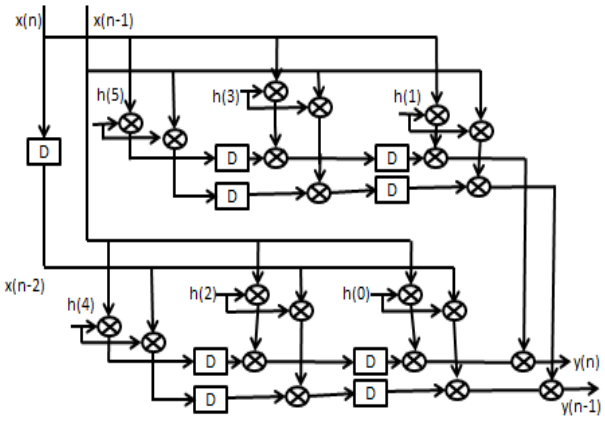

Fig.2 Transpose form type-I configuration for block FIR structure

This features not only allows design to get a pre-implementation on area, speed and power, but it also enables synthesis tool to rapidly satisfy user constraints and performs necessary trade-offs without the 'endless' feedbacks looking for the appropriate solution. For a given number M of nonnegative constraints with a bit-length N, RADIX-2r exhibits a sub linear runtime complexity O (M*N/r). Adder – Depth (AD) is not only a measure of the critical – path (speed), but also a good indicator of the power consumption. I want to compare the existing method to the design of FIR filter by using Wallace tree multiplier and kogg stone adder. Because the existing method is multiplier less so we are to clearly explain the difference between performance analysis of FIR filter by using multiplier and without multiplier. The Wallace tree multiplier has to a fast way to multiply two binary integers.

Any multiplier has 3 stages:
(a) .Partial products
(b). partial products addition
(c). final addition

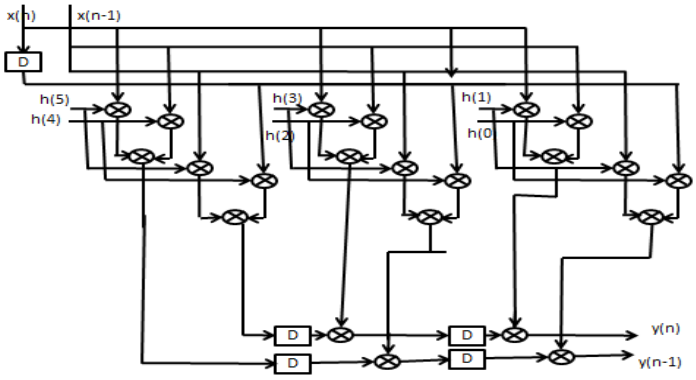

Fig.3 Transpose form type-II configuration for block FIR structure

Then the comparison between the FIR filter by using with a multiplier and without multiplier is shown in Table.1. If the above table we consider the dynamic power like it will be tells about the consumption of power in transistor switching. Static power is not consider because the static power is different in different IC family. We want to consider spartan6 its static power is 13.69mW. It is represents the base paper improvement result

Table 1.Comparison between WTM&KSA and existing method

Method	Delay (ns)	Area	Dynamic power (mW)
WTM&KSA	1.641	982	1.86
MCM	2.058	426	0.75

III. PROPOSED SYSTEM

The configured structure for block FIR is shown in Fig.4 for size L=4. Block size consists of one register unit, one selection unit, one IPU. It can be implemented by using N ROM LUT's and can be obtained in one clock cycle. Where N is filter length. The RU receives X_K during K^{th} cycle and produces L rows in parallel. The M IPU's also receive M short weight vector form CSU during K^{th} cycle. Each IPU has vector product of So^K with short weight vector. In every cycle, the structure receives a block of inputs 'L' and produces a block of outputs 'L'. Where the duration of cycle is $\mathbf{T = T_M + T_A + T_{FA} \log_2 L.}$

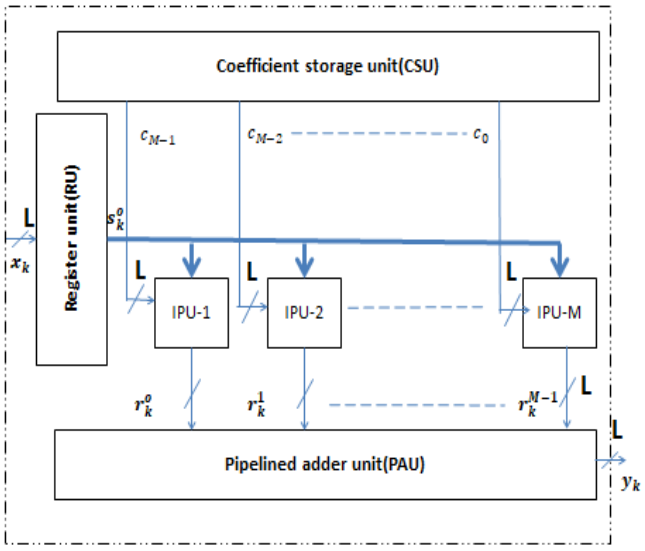

Fig.4 Proposed structures

Then the equation of FIR filter is

$$\mathbf{Y(z) = z^{-1}.z^{-1}\,(z^{-1}.r_{m-1} + r_{m-2} + r_{m-3}) \ldots\ldots + r_1 + r_0.}$$

Where $\mathbf{r = So^K}$

For low complexity realization multiplications are required to map to the MCM units. We will show that proposed formulation for MCM based implementation of block FIR can on make using symmetry in input to minimize no of shift-add operations in MCM blocks.

A.PROPOSED SYSTEM EQUATIONS:

By using Keizer's formula, we can find the order of the filter: then the equation becomes

$$N = \frac{[-20\ \log_{10}\sqrt{(\omega p.\omega s)} - 13]}{14.6(\omega s - \omega p)/2\pi}$$

Where δp and δs is pass band and stop band ripples
ωp and ωs is pass band and stop band frequencies

The desired filter coefficients are obtained by equation

$$h(n) = h_d(n) * W(n)$$

Then $h_d(n) = \frac{1}{2\pi}\int_{-\omega c}^{\omega c} H(\omega) * e^{j\omega n}$

$W(n) = \alpha + (1-\alpha)\cos(\frac{2\pi n}{N-1})$

Where ωc= cut-off frequency
α = hamming window

B. RECONFIGURABLE APPLICATIONS:

A filter is a circuit capable of passing certain frequencies while attenuating other frequencies. Thus, a filter can extract important frequencies from signals that also contain undesirable frequencies. In the field of electronics, there are many practical applications for filters. Examples:

1. Radio Communications
2. DC Power Supplies
3. Audio Electronics
4. Analog-to-Digital Conversion

IV. SIMULATION AND RESULTS

If the reconfigurable coefficients can be derived from the filter length like the filter order is 15 and its pass band ripple values become 0.01 and 0.01. It will do by using MATLAB software. Magnitude and phase plots become shown in Fig.5 and Fig.6.

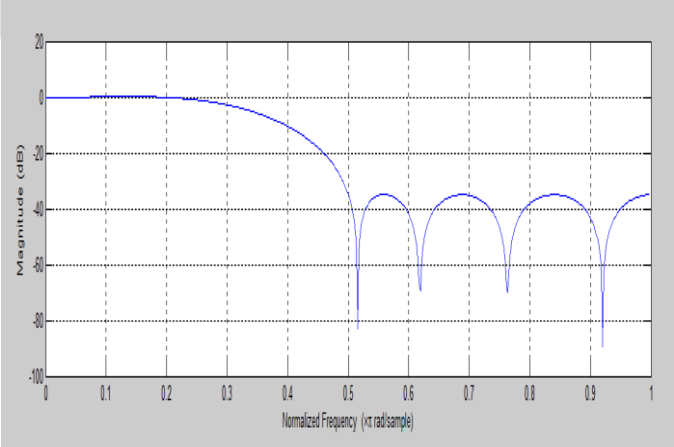

Fig.5 magnitude plot

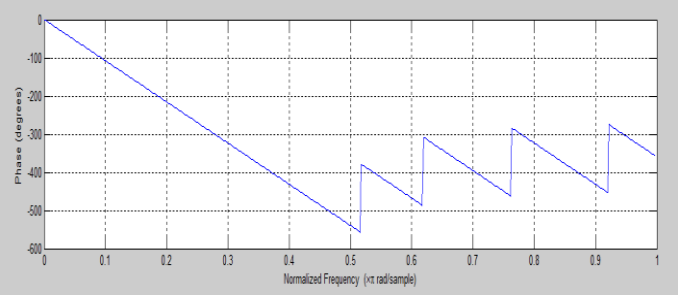

Fig.6 Phase plot

To implement the stable and reconfigurable coefficients Transpose form and also in cascaded form FIR filter is simulated using Xilinx Tool. The family of integrated circuit is spartan6 and the code will be written in behavioral structure. The area (no. of LUT's and flip-flops clock buffers and I/O buffers), delay and power were analyzed for reconfigurable circuits. For analyzing it is observed that the area is reduced when compared to the direct form FIR filter. The area of the transposed form of reconfigurable coefficients is less when compared to the cascaded form. But the delay will be reduced in both in reconfigurable transposed form and cascaded form compared to the direct form filter. Dynamic power also compared because the real power is observed in on-board but in this paper we consider only simulation that's way we can analyze the performance of the dynamic power. Static power is negligible in this case because static power is different in different IC families. It is constant at that IC family, so we are not considering the static power.

In Fig.7 RTL schematic view, when the structure is divided into two different blocks and at the end it will be added.

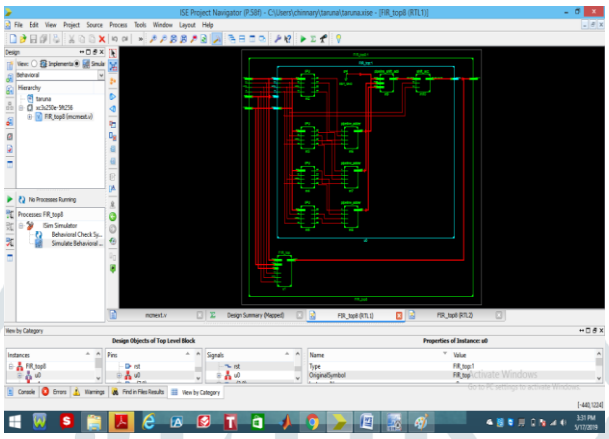

Fig.7 RTL schematic view

In Fig.8 experimental result of FIR filter, it is a simulation result of reconfigurable coefficient transposed form FIR block with two coefficients. The input given to the filter is 00000101 and the output achieved for the filter is 0001101100110100. The delay for the reconfigurable transposed form FIR filter structure is 1.64ns. The delay for compared to the direct form filter delay. The delay of the direct form FIR filter structure is 2.94ns.

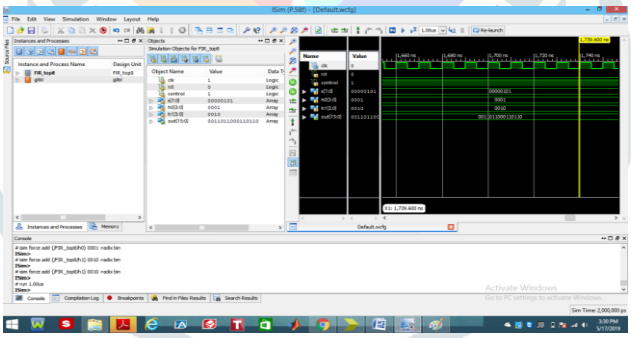

Fig.8 Experimental Result of FIR Filter

The total number of LUT'S utilized in the reconfigurable FIR is 135; the flip-flops are 52, no of bonded input/output buffers 25 and the number of slices 70. The LUT'S, Flip-flops are reduced when compare to the direct form FIR filter The length of the reconfigurable transposed form and cascaded form FIR filter is increased like 8-bit, 16-bit, 32-bit and 64-bit. Then the comparison of area, delay and dynamic power is shown in below Table 2.

TABLE.2 COMPARISION TABLE

LENGHT	DELAY (ns)	AREA (LUT's)	DYNAMIC POWER(mW)
8-bit	2.446	294	0.45
16-bit	3.312	312	0.96
32-bit	4.562	384	1.86
64-bit	5.963	419	2.73

Graphical representation of reconfigurable transposed form FIR filter at different lengths is shown in Fig.9

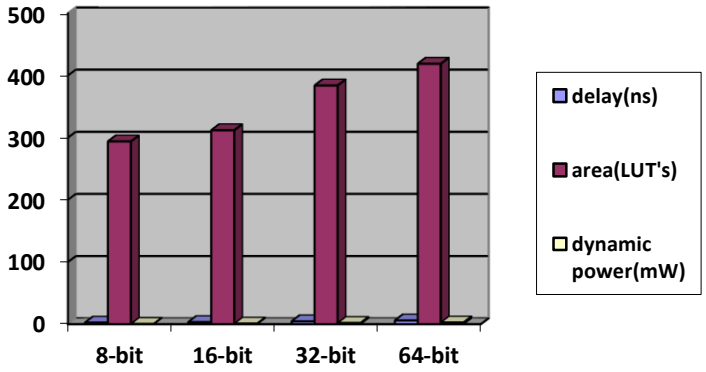

Fig.9 comparison of delay, area and power

V. CONCLUSION

In this paper, we have performed the design of cascaded form FIR and reconfigurable coefficient of transposed form FIR filter. At its nature transposed form FIR filter is a pipelined structure, in reconfigurable coefficients. MCM technique implementation is a bit difficult. But in reconfigurable coefficients transposed form FIR filter, the area and dynamic power can be minimized up to some extent by using MCM technique. In reconfigurable transposed form FIR filter we use the multiplier design, the structure which we have implemented. i.e., transposed form FIR filter will have less area and dynamic power compared with direct form FIR. In future delay can be further minimized by applying various techniques in transposed FIR filter.

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