Improvement of Performance in Architecture of Ring Oscillator Clock Generation using CPG

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Abstract: **Power management (PM) in System on Chip (SoC) plays a crucial role in mobile device architectures. Several new architectures were proposed to reduce the power inside the IPs (Intellectual property) like clock gating and power gating, with the task of reducing system level IDLE power gating. According to the nature of the system , multiple system states are created based on power and IDLE conditions such as 'P states ' and 'C states'. In order to power down the circuit further, it has to go to a deeper state, but in order to achieve this we need to do power gating in various regions of the circuit. As a consequence when the system goes through various power up sequences, the wake up latency will be much bigger which affects the system performance. In order to combat this situation, alternate clock sources were introduced such as a ring oscillator clock. Since the ring oscillator clock is susceptible to Process, Voltage and Temperature (PVTA) variations, a innovative way to reduce the system latency by a new power architecture flow with a calibrated ring oscillator clock that runs all power management operations on the newly generated clock is introduced. The main goal of this design is to reduce the system latency while being more resistant to PVTA variations.**

***Index Terms*: CRO, Power Management, Power Gating, Save- Restore, PVTA, RTC, IP.**

1. INTRODUCTION

Power management (PM) in System on Chip (SoC) plays a crucial role in mobile device architectures which reduces the power inside the IPs (Intellectual property) like clock gating and power gating, with the task of reducing system level IDLE power gating. According to the nature of the system, multiple system states are created based on power and IDLE conditions such as 'P states ' and 'C states' as discussed in [1],[2],[3]. In order to power down the circuit further, it has to go to a deeper state, when the system goes through various power up sequences, the wake up latency will be much bigger.

In order to combat this situation, alternate clock sources were introduced such as a ring oscillator clock. Since the ring oscillator clock is susceptible to Process, Voltage and Temperature (PVTA) variations, we developed a novel architecture to reduce PVTA variations. The main goal of this design is to reduce the system latency while being more resistant to PVTA variations.

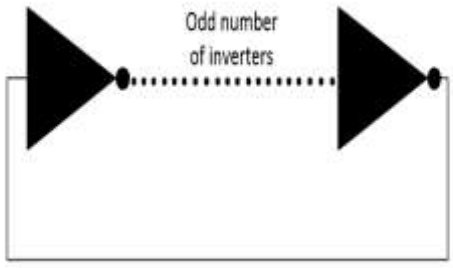

Fig. 1: Basic Ring Oscillator Architecture

The Ring oscillators are usually used to generate clock. The frequency is varied by varying the length of the oscillator. It consists of an odd number of inverters connected in a closed loop chain. A total phase shift of 2π around the loop at a frequency where the small signal gain is about 0dB is required for proper oscillation [4]. There is a frequency dependent phase shift of π/n for each n-stage of the ring oscillator and the dc inversion provides a phase shift of π giving a total phase shift of 2π as shown in fig.1.

This condition along with the frequency where the small signal gain is 0dB is necessary for proper oscillation. The equation for the frequency of oscillation is given by,

$$f = 1/2nTd \ldots. (1)$$

Where Td is the delay for each inverter stage. This equation shows that the time delay of nTd gives the phase shift of π. The main drawback in this model that it does not provide flexibility in changing frequencies due to the dependency on the number of inverter stages n and the propagation delay Td.

The PVTA variations are variations which cause the circuit to behave in unexpected ways. The process variation deviations can occur due to variations in the fabrication process. Non uniform conditions during deposition and diffusion of impurities can cause different impurity concentration densities, oxide thickness and diffusion depths. This can cause variations in sheet resistance. During manufacturing it is not possible to obtain uniform device dimensions for each MOS circuit such as transistor length and width will lead to variations in threshold voltage and can affect the propagation delay. As a result different areas of chips has different electric properties.

The supply voltage provided can deviate from the ideal value. This can occur due to the resistance present across the supply lines. The presence of self inductance of supply lines can also contribute to the voltage drop[6]. Voltage variations can affect the saturation current of the circuit. Since the propagation delay depends on the saturation current, the change in voltage drop across various regions of the circuit can cause difference in propagation delay across different areas.

The Variation in temperature can occur in different regions of the circuit due to dissipation of power. This can occur due to switching, short circuit and leakage power of the circuit where switching is the dominant mode of power dissipation. With the increase in temperature at a certain point mobility of electrons and holes will begin to decrease, due to this, it can cause increase in delay. Higher temperature can also cause decrease in threshold voltage which can in turn lead to decrease in delay. However the decrease in mobility has the greater effect on delay.

The Power consumption in SOCs (System on chip) is one of the most important concerns that the silicon industry is facing recently[7]. To resolve this issue, efficient power management techniques have been introduced. Power management in battery-operated systems can lead to lower average power consumption, which helps in developing smaller, lighter and cheaper batteries[8]. In the case of live batteries like mobile and hand held devices, lower power means longer operating life and that directly translates to greater customer satisfaction. Improvements in device-level methods such as system level and application level improvements are some of the steps in the enhancement of SOC power management, which can boost the effectiveness of power management efforts significantly. Dynamic power gating is one example of the system level implementation for better power management.

The Static power and dynamic power dissipation are the two kinds of power dissipation that is common in CMOS circuits. In modern low power, high performance microprocessors, the power consumed by the device when it is in quiescent mode is known as static power and the power consumed when the device is in operational mode is known as dynamic power. Dynamic power is caused due to switching. When we shrink the size of the circuit the inductive and capacitive effects of the wires will become more significant and so as a first order approximation, the wires connected as either input or output is modeled as capacitive loads that are connected to the circuit. Whenever switching happens these capacitive loads will get simultaneously charged or discharged resulting in power dissipation[9].The circuits which are switched more rapidly will dissipate more power. If we are dealing with a circuit working under an extremely high frequency, the power dissipation will be very high. There are several ways of reducing dynamic power, one is by reducing clock frequency. However the drawback of this approach is that it affects the performance of the circuit. The other method is by reducing load capacitance, but this solution is hard to implement as it requires careful circuit design using fewer wires. Hence alternative methods are developed in order to reduce dynamic power dissipation which will be discussed in the coming sections. If the circuit is not switching, theoretically it is expected that it should not consume power. However in reality, power consumption can take place due to unwanted current that leaks between source and drain called 'sub threshold current'. This current can occur even if the gate voltage is below the threshold voltage (off condition). This effect is even more significant as we scale down the CMOS circuits since other unwanted effects can occur such as punch through- where through channel length modulation the depletion regions around the source and drain merge, or tunneling- where the gate voltage is high enough such that the charge carriers tunnel through the oxide layer. Several techniques have been developed for reducing static power dissipation such as voltage islands certain large portions of the circuit is shut off from voltage, however this paper will focus mainly on dealing with dynamic power dissipation.

This paper is organized as section II describes Existing System and in section III discussed Proposed Method and Section IV describes in Simulation results and Section V concludes the paper followed by references.

2. EXISTING SYSTEM

In system level there are two ways of power gating i.e., by partition aware power gating and partition unaware power gating methods for Ring Oscillator and are static with respect to variation in frequencies as shown in fig.1.

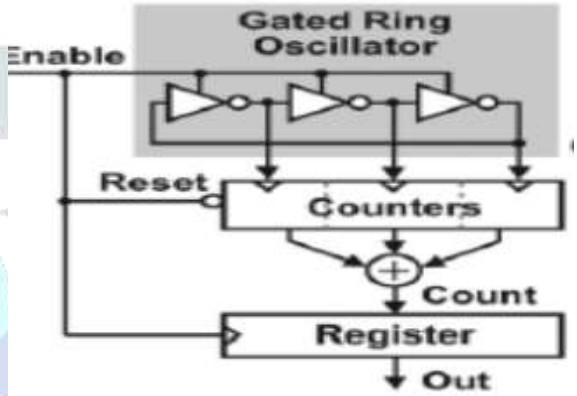

Figure 1. Power Gated Ring Oscillator

It has several drawbacks like large area is occupied, more power is dissipated, it is affected by PVTA variations and it uses the PLL clock.

The other existing design includes calibrated Ring Oscillator Clock by dynamically varying the trigger signal condition according to the varying Ring Oscillator (RO) clock frequency even though the frequencies vary with process corners and also with other parameters such as temperature and voltage as shown in fig.2.

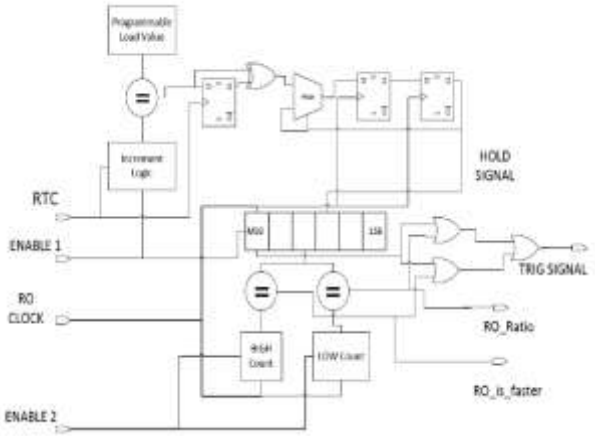

Figure 2: Architectural Diagram for calibrated RO Clock generation

The Ring Oscillator Clock is a very secure tamper proof clock because it is entirely generated internally. While it is a highly secure clock, it's not widely used since the frequencies vary with process corners and also with other parameters such as temperature and voltage. This concept proposed here talks about calibrating the Ring oscillator clock so it can be used in a predictable manner for standard applications such as Watch Dog Timers for generating platform reset. The solution is to calibrate the Ring Oscillator Clock and then using it for various applications. The diagram of proposed architecture is shown in Fig.2.

The trigger signal condition is dynamically varied according to the varying Ring Oscillator (RO) clock frequency. In Current SOCs platform, reset is generated based on ring oscillator clocks because of its secure nature. But because of the variation of frequency it may make false triggering. The proposed solution will resolve this issue. With reference to Figure 2, there are two Counters. One of them runs on a Ring Oscillator Clock and the other one runs on a Real Time Clock(RTC) supplied externally. Using the RTC Clock, the Ring Oscillator is calibrated. This calibration happens only at the time of boot and it never uses the RTC Clock further. Upon reset, both Counters commence counting based on the enable condition. Enable 1 will be asserted once power good reset is asserted and enable 2 will be asserted after the enable 1 assertion by software. Once the RTC Clock Counter reaches the desired value , it stops itself and it also stops the free running Ring Oscillator Clock Counter. This way, the Ring Oscillator Clock Counter gets calibrated.

This also secures the SoC platform from a potential threat of hacking the RTC Clock. In this case MSB bit of RO Counter will get set as the RO is continuously running and hence triggers a platform reset. It has several drawbacks like the calibration is performed only internally, but has the advantages like it is user calibrated which occupies less area, less power consumption and is faster in performance.

3. PROPOSED METHOD

The Cyclic Power-Gating (CPG) is a form of aggressive power-gating, where the core is powered-on and off over a small time period. The effective frequency of the processor and its power consumption can be controlled by changing the duty-cycle, the ratio between on and off states in a single power-gating period.

Dynamic Voltage and Frequency Scaling is the most commonly used power management technique in modern processors. However, the ability of an individual chip to operate under reduced supply voltage can no longer be predetermined at the design stage and may even change over time. This paper presents Cyclic Power-Gating (CPG), a novel power management strategy where the power consumption of a core can be finely controlled without scaling the supply voltage. CPG builds on state-retentive power-gating which allows the power supply to a core to be switched off and on again at high speed (tens of clock cycles) with minimal disruption to running programs. The power-gating is cyclic, by altering the ratio of time spent powered-on and off in each power-gating period the effective operating frequency and power consumption of a core can be controlled.

The operation of Cyclic Power Gating is shown in Fig.3. The CPG scheme has a fixed period, TCPG. The effective operating frequency of the core is determined by the duty cycle ratio:

$$Duty - cycle = \frac{T_{CPG} - T_{off}}{T_{CPG}} \text{ ..... (2)}$$

where Toff is the powered-off time during each CPG period. Toff is controlled by a timer circuit in the CPG controller which is initialized at the start of each CPG period and so the duty-cycle (and hence the core frequency) can be changed between any CPG cycle with no overhead. The duty-cycle may be assigned to any value over the range ½ 0::1 allowing for fine-grained power consumption control, without scaling the supply voltage. To maximize the ability of a CPG-based power manager to respond to changes in program execution it is desirable to make TCPG as small as possible. However, the power-gating scheme has delay and energy overheads which reduce the power savings.

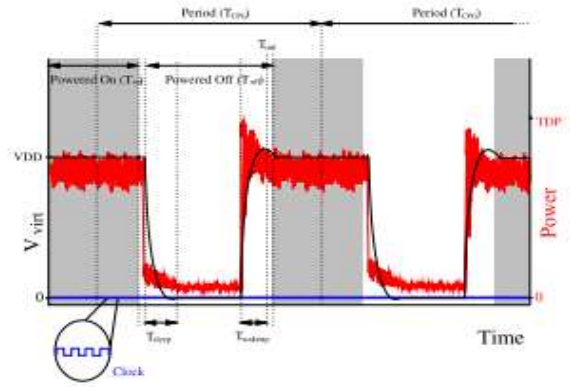

Figure 3. Cycle Power Gating

This design has several advantages like improved performance, less power dissipation and fine grain scaling of power consumption.

4. SIMULATION RESULTS

The designs are modelled in Verilog HDL and are functionally verified by using Xilinx ISIM Simulation Tool. The designs are synthesized for Spartan3E FPGA by suing Xilinx ISE 14.5 Tools for the device XC3S500E with a package of FG320 and a speed grade of -5.

The simulation waveform for power aware ring oscillator design is shown in figure 4 where the clock_out shows the output clock signal from the ring oscillator. This design is converted to register transfer logic by the Xilinx synthesizer as shown in figure 5 and to 90nm CMOS technology based LUT mapped schematic as shown in figure 6. The power aware ring oscillator design is extracted for FPGA along with its sample routing without imposing constraints is shown in figure 7.

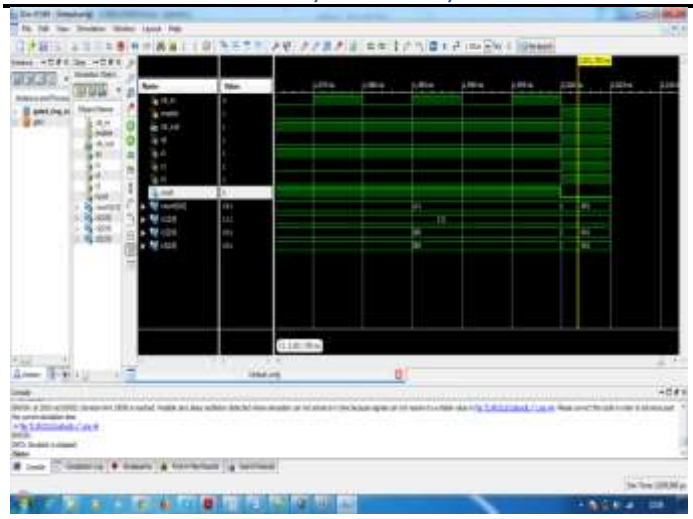

Figure 4: simulation waveform for power aware ring oscillator design

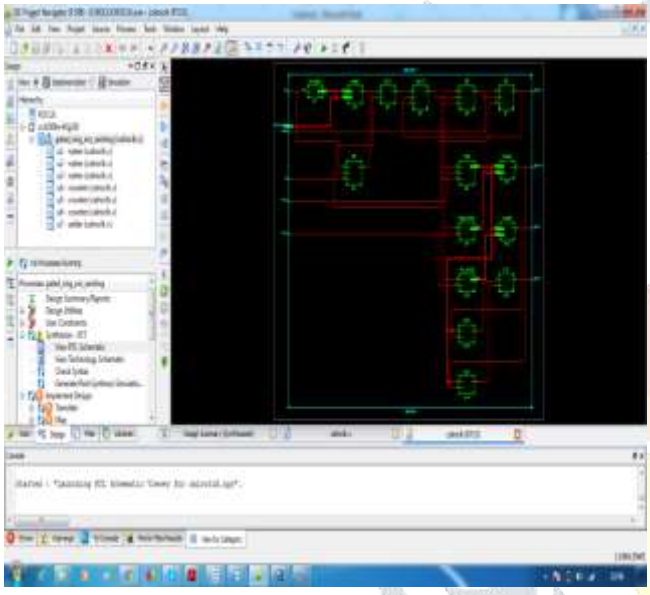

figure 5: RTL Schematic of power aware ring oscillator design

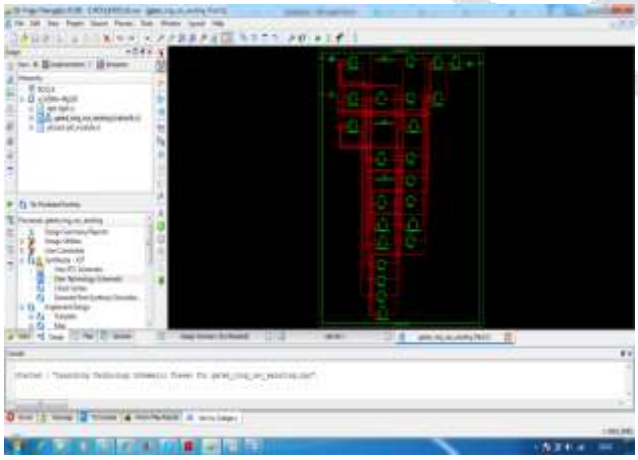

figure 6: RTL Schematic of power aware ring oscillator design

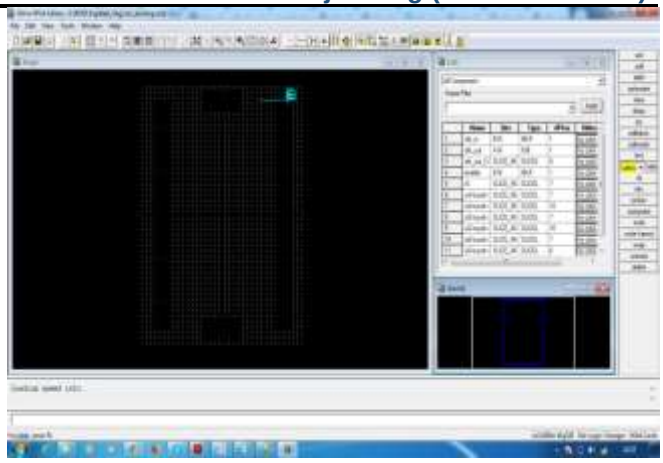

figure 7: FPGA Implementation of power aware ring oscillator design

The simulation waveform for Calibrated ring oscillator design is shown in figure 8. This design is converted to register transfer logic by the Xilinx synthesizer as shown in figure 9 and to 90nm CMOS technology based LUT mapped schematic as shown in figure 10. The calibrated ring oscillator design is extracted for FPGA along with its sample routing without imposing constraints is shown in figure 11.

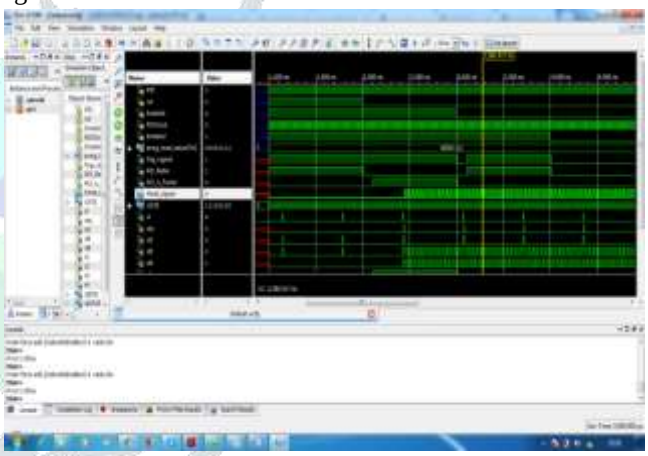

Figure 8: Simulation waveform of Calibrated Ring Oscillator Design

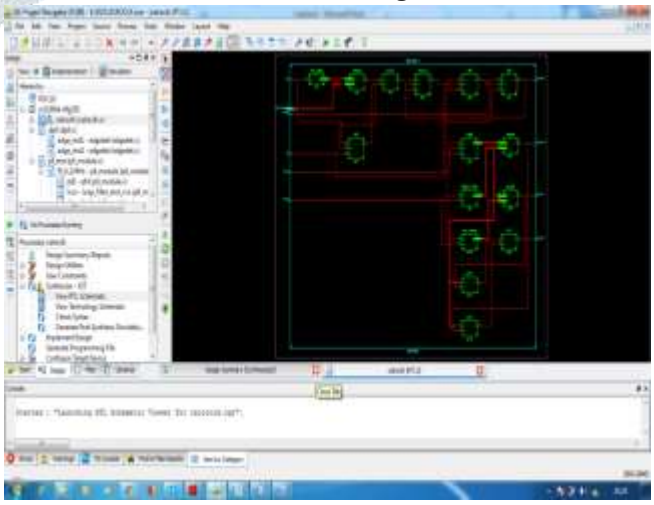

Figure 9: RTL Schematic of Calibrated Ring Oscillator Design

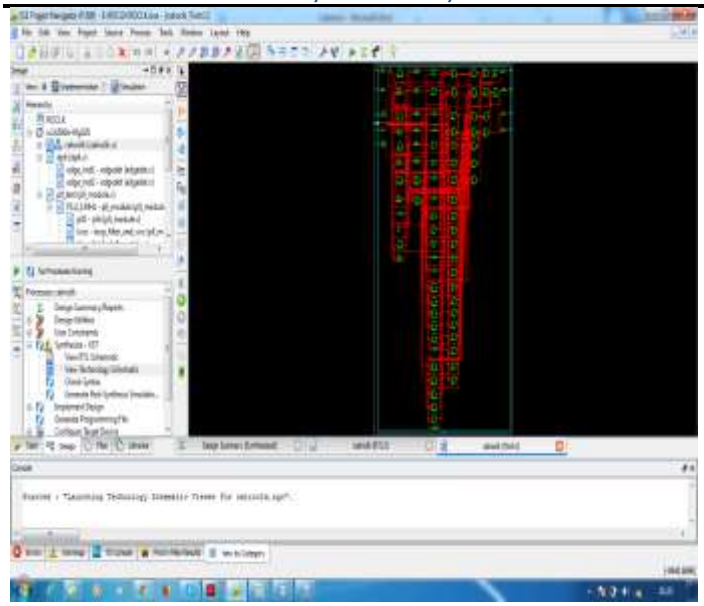

Figure 10: Technology Schematic of Calibrated Ring Oscillator Design

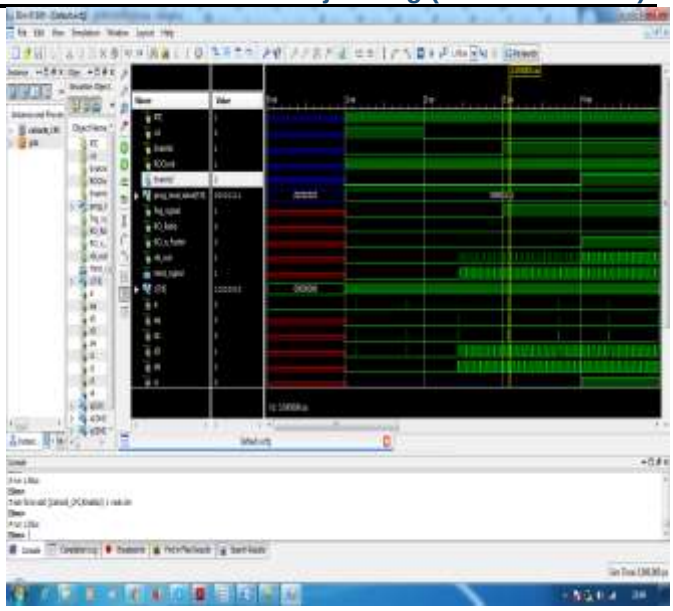

figure 12: Simulation Waveforms of cyclic power gated ring oscillator design

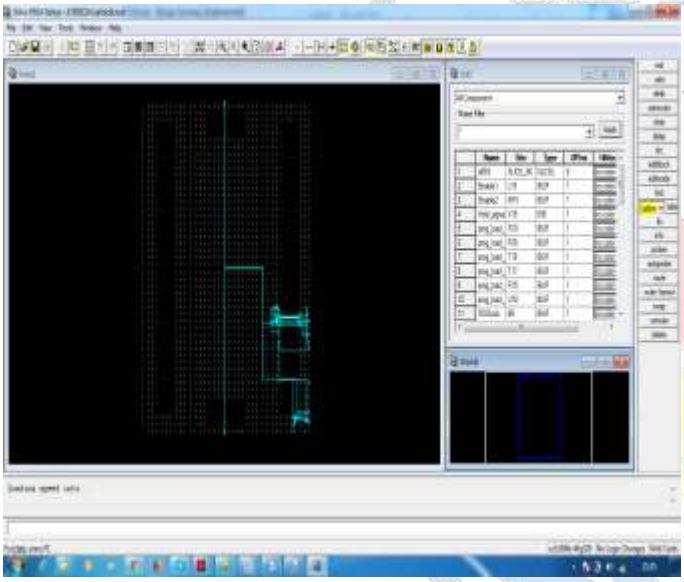

Figure 11: FPGA Implementation of Calibrated Ring Oscillator Design

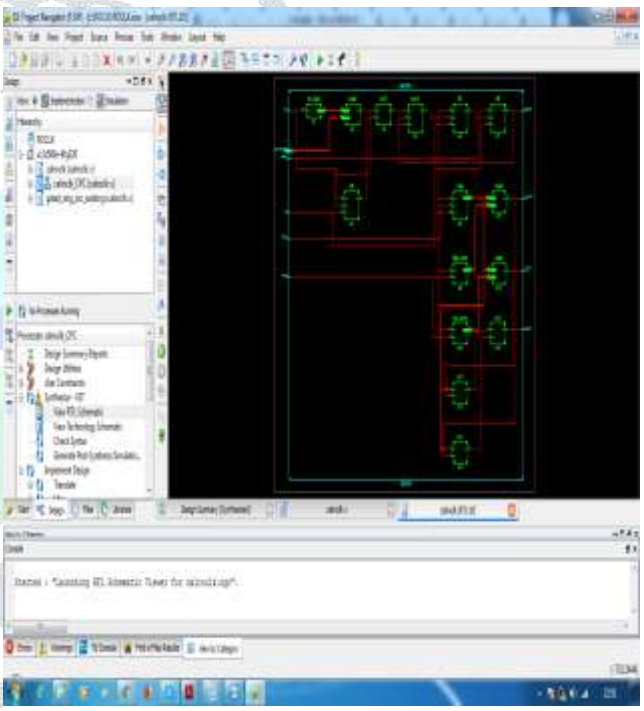

Figure 13: RTL Schematic of cyclic power gated ring oscillator design

The simulation waveform for cyclic power gated ring oscillator design is shown in figure 12. This design is converted to register transfer logic by the Xilinx synthesizer as shown in figure 13 and to 90nm CMOS technology based LUT mapped schematic as shown in figure 14. The cyclic power gated ring oscillator design is extracted for FPGA along with its sample routing without imposing constraints is shown in figure 15.

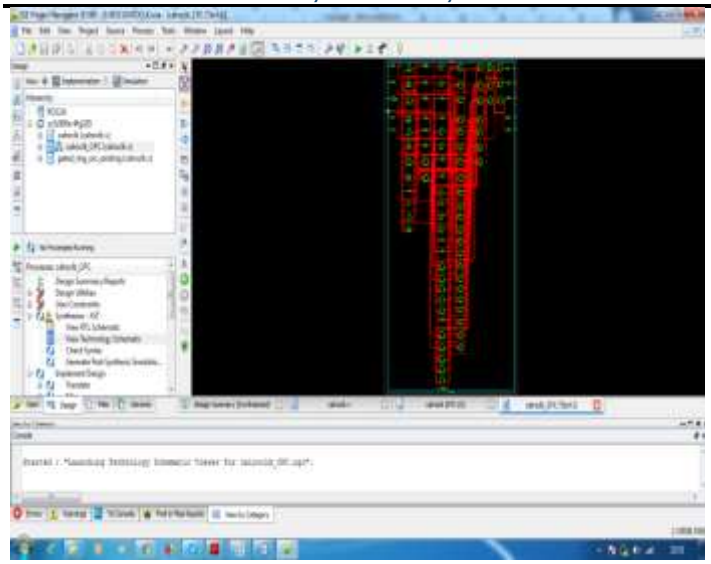

Figure 14: Technology Schematic of cyclic power gated ring oscillator design

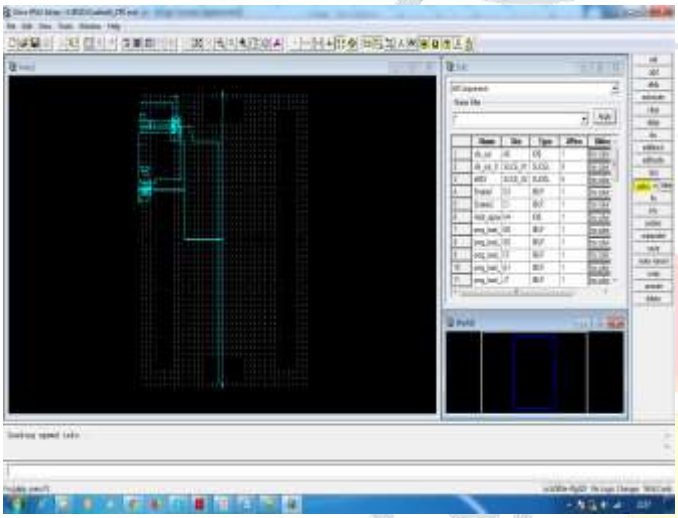

Figure 15: FPGA Implementation of cyclic power gated ring oscillator design

Table-I: Comparison of various Ring Oscillator Designs

Parameters	Tree Based Multicast NOC Design	IPM and OPM based Multicast NOC Design	Proposed Multicast NOC Design
No. of slices	8 out of 4656	18 out of 4656	18 out of 4656
No. of 4-input LUTs	17 out of 9312	34 out of 9312	35 out of 9312
Combinational Path Delay	-	-	6.096ns
Average Fanout	2.00	2.52	2.53
Logic Power	0.00003	0.00007	0.00001
Signal Data Power	0.00002	0.00003	0.00002
I/O Power	0.00106	0.00319	0.00420

From Table I, it is clear that the proposed design slightly increases the area with an acceptable delay but with a reduction of 85.7% in logic power and 33.3% in data power. Also there is slight increase in fanout of the proposed design.

5. CONCLUSION

In mobile architectures, Power management architectures were proposed to reduce the power inside the IPs (Intellectual property) like clock gating and power gating, with the task of reducing system level IDLE power gating. Alternate clock sources were introduced such as a ring oscillator clock which is susceptible to Process, Voltage and Temperature (PVTA) variations i.e., a innovative way to reduce the system latency by a new power architecture flow with a calibrated ring oscillator clock that runs all power management operations on the newly generated clock is introduced. The main goal of this design is to reduce the system latency while being more resistant to PVTA variations. In this paper, a new architecture for ring oscillator calibration circuit which is faster in performance and has less area and power compared to the existing power management architecture. The proposed design slightly increases the area with an acceptable delay but with a reduction of 85.7% in logic power and 33.3% in data power. Also there is slight increase in fanout of the proposed design.

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