Efficient Area and Delay of Error Avoidance Technique using Synchronizer and Flip-flops

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Abstract: **Time borrowing techniques have been widely used to mitigate the timing errors in high-performance designs. The dynamic flip-flop conversion technique is introduced by Ahmadi et al. which dynamically converts flip-flops into transparent latches to grant the time borrowing from the next stage and prevent setup time violation but it could not prevent the timing violation in the successive critical path (SCP) and critical feedback path (CFP) structures. Then a fast prediction logic of the critical path along with dynamic clock stretching in SCP and CFP structures was introduced which also could not prevent the timing errors. The proposed technique uses glitch free clock switching for unrelated clocks which is more effective in terms of the performance improvement and less area utilization when compared with the best existing technique. The designs are modelled in Verilog HDL and are functionally verified by using Xilinx ISIM Simulation Tool. The designs are synthesized for Spartan3E FPGA by suing Xilinx ISE 14.5 Tools for the device XC3S500E with a package of FG320 and a speed grade of -5. The proposed design proves to be better than the remaining designs functionally. Also the proposed design occupies an area which is around 33% less than the previous designs.**

Index Terms**: Dynamic clock stretching, high-performance design, prediction logic, setup time violation, time borrowing**

1. INTRODUCTION

The demand for high-performance design has been significantly increasing over the past few years. The maximum tolerable frequency, is computed based on the delay of the longest paths (called critical paths) in the circuit. In Literature, there exist several methods to increase the performance of the design. In [3], data are captured by a shadow latch with a delayed clock signal, as well as by the main flip-flop which caused timing violation and the system could correct the propagated error by halting the next stages for a cycle. In variable latency (V.L.) designs, the period of the clock is set to T. Then, in the case of activating a path with the latency of T +T, an extra clock cycle is required [4]. Time borrowing is another technique in which the clock period of the circuit, i.e., T1, is set to a smaller value than the maximum delay of the critical path, i.e., T1 + T. Whenever a path having a larger delay than T1 is activated, the extra T time is borrowed from its successive stages. In [5], latches were used to perform time borrowing during the high phase of the clock cycle. In [6], soft-edge flip-flops (SEFFs), having a small window of transparency instead of a hard edge, have been used. In [7], a pulsed latch augmented with an additional circuit to delay the clock signal over multiple cycles in case of time borrowing. In [1] and [8], a dynamic flip-flop conversion (DFFC) technique is introduced in which the timing violation is predicted by a timing violation predictor (TVP) block that detects a transition at the midpoint (the node that cuts the path into half in terms of delay) during the second half of the clock period. In the case of detecting a late data at the midpoint and predicting error, the Error signal is issued by the TVP block. Then, a data arrival detector (DAD) block toggles the Conv signal, and the flip-flop operates as a transparent latch. When the late data arrive at the input of the critical flip-flop, it is captured. Then, the Conv signal toggles again and the critical flip-flop goes back to its normal operation. In [1], it proves that DFFC is not able to prevent the timing errors in problematic path structures as these paths include critical paths with short sequential depth, critical feedback path (CFP)—a feedback path which is also a critical path—and successive critical path (SCP)—a critical path followed by another critical path in successive sequential stages. In [2], a hybrid technique is proposed which uses the DFFC of [1] in critical paths. Whenever a problematic path is activated, the clock is, dynamically, stretched for half of the clock cycle using the clock shifter but it suffers from the large number of clock stretching. To overcome this problem, a dynamic timing error avoidance (DTEA) technique is used which tries to prevent timing violation using DFFC else the output of a faster logic (prediction logic) along with dynamic clock stretching and time borrowing is used to prevent timing violation. The demand for high performance designs which are not susceptible to variations, in worst case design methodology the maximum allowable frequency (MAF), is computed based on the delay of the longest paths (critical paths) in the circuit which make the designer keep the frequency low while losing the performance. But the performance degradation is even worse when process variation is taken into account that force the designer to include timing margins in the design which leads to the performance degradation. Hence a simply the operational frequency of the circuit is increased beyond the MAF. Then timing violations occur because critical paths would not be able to finish their job in a single clock period.

To address these timing violation issues three main approaches including error detection and correction, retiming and time borrowing have been proposed. In error detection and correction technique a timing error is detected at each flip-flop using a transition detector circuit and then a recovery mechanism corrects the data after some clock cycles [2] which do not prevent timing errors. Retiming is a technique to prevent timing violations by moving flip-flops backwards or forwards in the paths which is not efficient due to increase in number of flip-flops [3]. The time borrowing technique [4], [5], [8] is used where a critical stage in which the setup time is violated can borrow some time from the successive stage if it has enough timing slack. In [5] and [6] the timing yield was improved by replacing some flip-flops with latches as the latches are level sensitive, the late data from critical paths can cross the latches when they are transparent. Still these latch based designs suffer from large transparency windows and large delay elements that should be inserted in short paths to avoid hold time violation (HTV). In [7] and [19] a latch is placed at the destination flipflop to perform time borrowing. A transition detector block is used to detect time borrowing in critical latch and issues a warning signal which raises the supply voltage of the next stage to speed up the next stage and prevent further timing violations. In [8] and [9], soft-edge flip-flops (SEFF) have been used which have a small window of transparency instead of a hard edge, allowing limited cycle stealing on critical paths, and thus compensating for delay variations.

This paper proposes a timing error prevention method which reduces the timing errors and the area occupied by using the synchronizer and flipflops. The paper is organized as the description in section-II for existing designs and Section-III for proposed designs. The results are discussed in section-IV and finally the paper is concluded.

2. EXISTING SYSTEM

(a) Timing Error Prevention using Elastic Clocking

Timing error prevention using elastic clocking is an effective method for preventing timing failures by utilizing time borrowing and elastic clock stretching, thereby eliminating a safety margin as shown in figure 1. Since an additional recovery or replay operation for the error management is not required, this technique is delay-error tolerant method can minimize the performance penalty, i.e., it can tolerate timing variations due to process, voltage, and temperature fluctuations with minimal performance penalty even at high activation probability of critical paths. Hence, it allows a system operate over a wider voltage/frequency range. The drawbacks of existing system are the input clock frequency has to be till the first error is detected and the time borrowing flip flops are to be used in critical path.

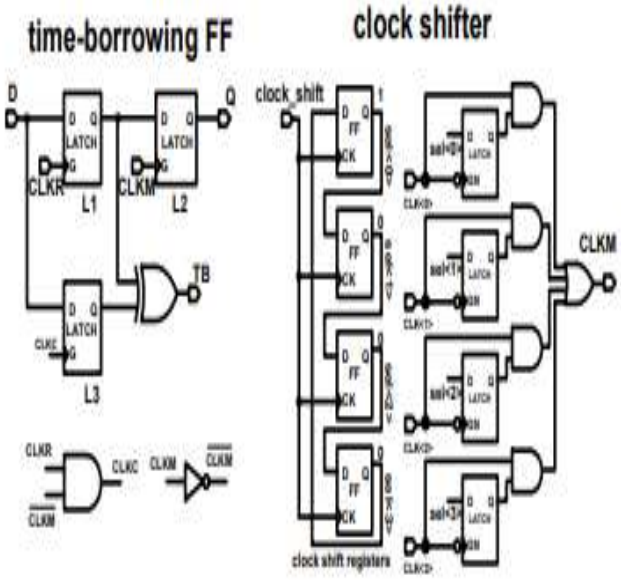


Figure 1: block diagram of the time-borrowing flip flop and the clock signals

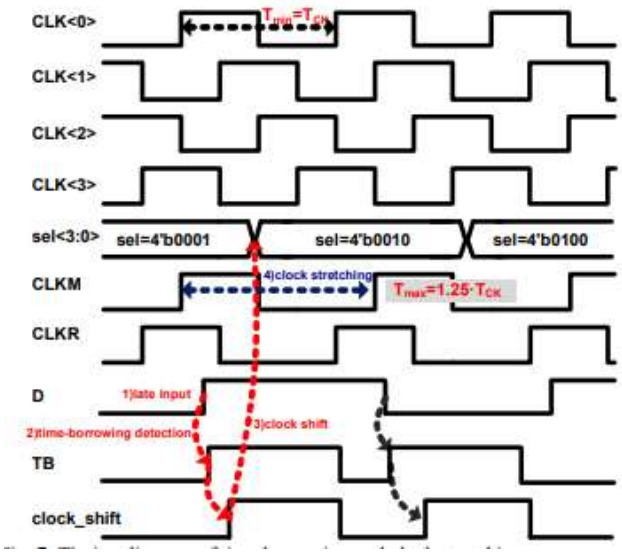


Figure 2: Timing Error Prevention using Elastic Clocking

(b) Dynamic Timing Error Avoidance Technique

Dynamic Timing Error Avoidance technique was presented which first tries to prevent timing errors using the time borrowing technique. If the structure of the critical paths does not allow time borrowing, it utilizes prediction logic of the critical paths—having a smaller delay than that of the exact one—along with dynamic clock stretching to achieve the high-performance operation of the circuit as shown in figure 2. The drawbacks of this technique are it does not prevent timing errors in problematic path structures and it requires hybrid combination of clock stretching and prediction logic.

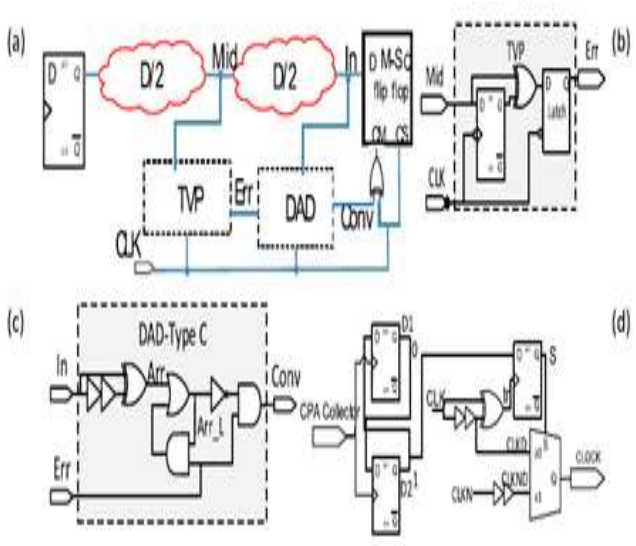
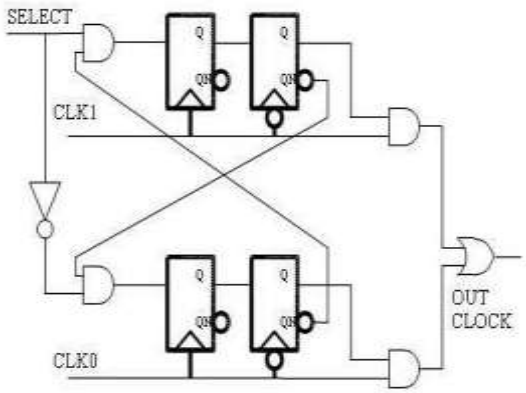


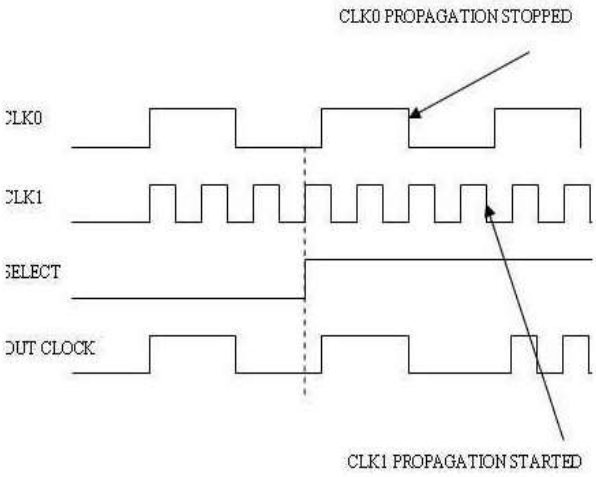
Figure 3: Dynamic Timing Error Avoidance technique (a) DFFC Micro architecture (b)TVP Block (c)DAD Block (d) Clock shifter block

3. PROPOSED METHOD

The proposed technique uses the concept for avoiding glitches which are the major sources of error by using synchronizer and dual Flip-flop configuration as shown in figure 3. It helps in avoiding the races of asynchronous circuits too. It has advantages like it can avoid meta-stability condition which is caused due to timing errors and it can be used for multiple clocking systems. When the select is enabled only one set of flip flops are active which minimizes the power dissipation.



(a) Logic Diagram



(b) Input and Output Waveforms

Figure 4: timing error prevention by using synchronizer and flip-flops

4. SIMULATION RESULTS

The designs are modelled in Verilog HDL and are functionally verified by using Xilinx ISIM Simulation Tool. The designs are synthesized for Spartan3E FPGA by suing Xilinx ISE 14.5 Tools for the device XC3S500E with a package of FG320 and a speed grade of -5.

The simulation waveform for Timing Error Prevention using Elastic Clocking is shown in figure 4 where clearly the extracted clock minimizes the timing errors. The modelled Timing Error Prevention using Elastic Clocking design is converted to register transfer logic by the Xilins synthesizer as shown in figure 5 and to 90nm CMOS technology based LUT mapped schematic as shown in figure 6. The Timing Error Prevention using Elastic Clocking design extracted for FPGA along with its sample routing without imposing constraints is shown in figure 7.

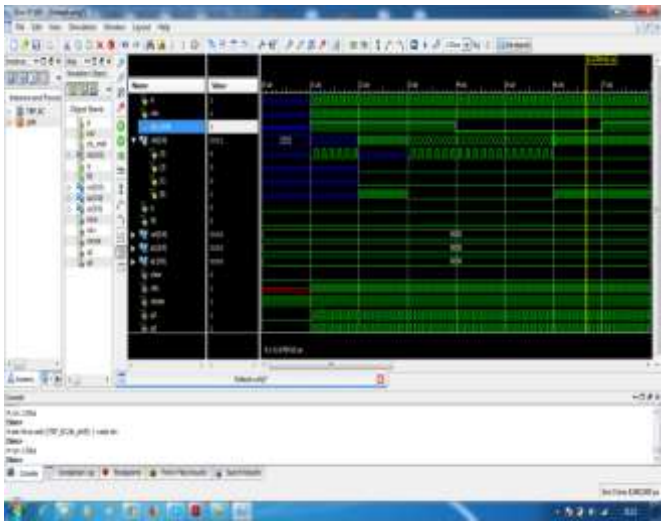


Figure 5: Simulation Result of Timing Error Prevention using Elastic Clocking

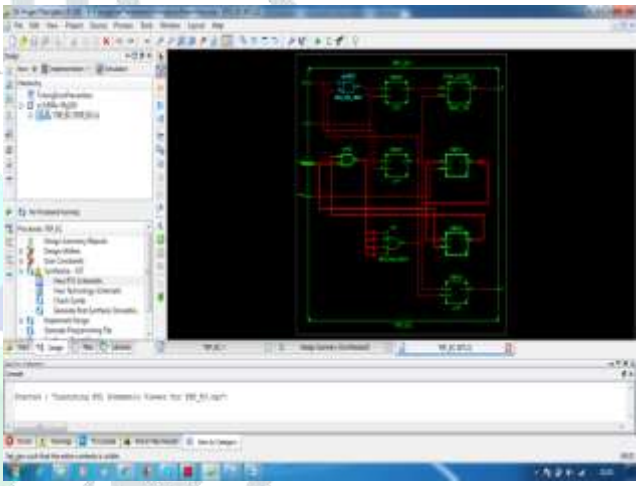


Figure 6: RTL Schematic for Timing Error Prevention using Elastic Clocking

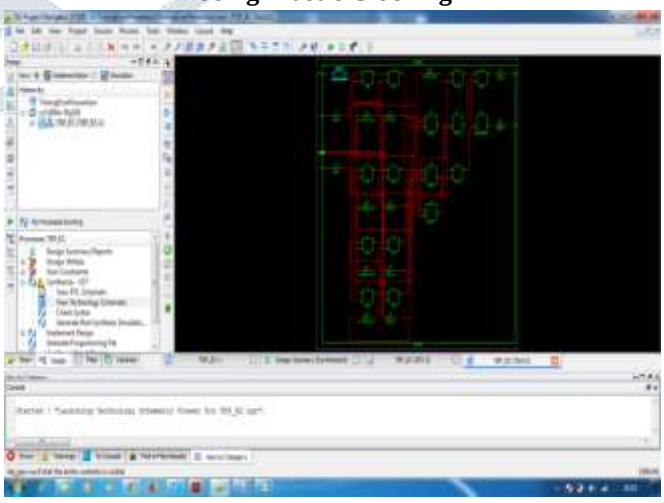


Figure 7: Technology Schematic for Timing Error Prevention using Elastic Clocking

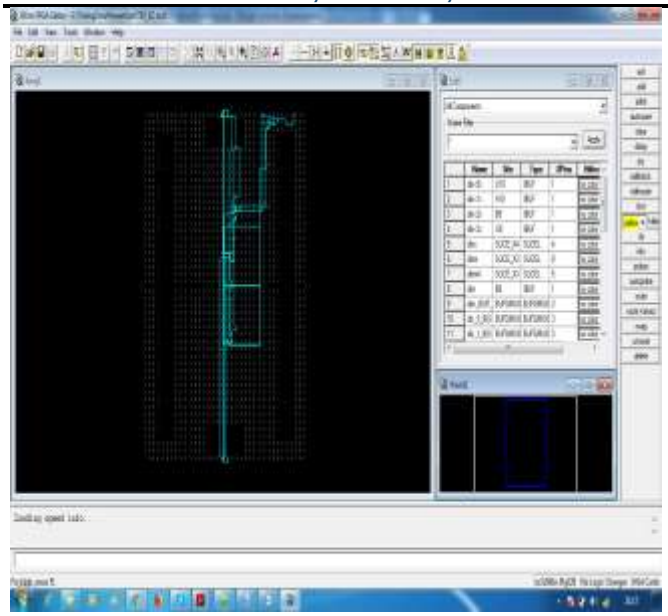


Figure 8: FPGA Implementation of Timing Error Prevention using Elastic Clocking

The simulation waveform for Dynamic Timing Error Avoidance technique is shown in figure 8 where clearly the extracted clock minimizes the timing errors better than the previous design.. The modelled design of Dynamic Timing Error Avoidance technique is converted to register transfer logic by the Xilins synthesizer as shown in figure 9 and to 90nm CMOS technology based LUT mapped schematic as shown in figure 10. The Dynamic Timing Error Avoidance technique design extracted for FPGA along with its sample routing without imposing constraints is shown in figure 11.

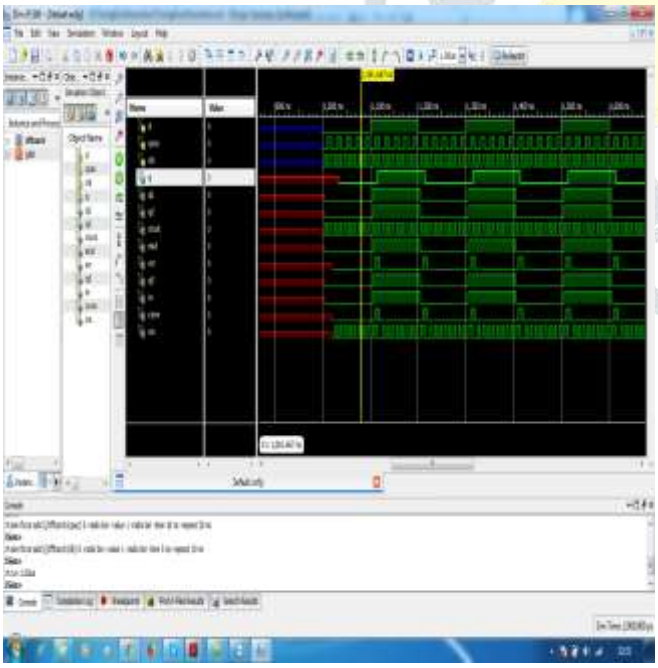


Figure 9: Simulation Result for Dynamic Timing Error Avoidance technique

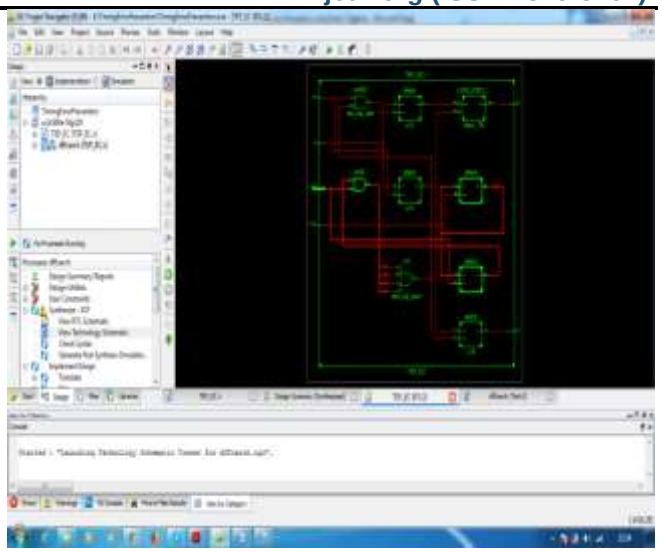


Figure 10: RTL Schematic for Dynamic Timing Error Avoidance technique Technology Schematic

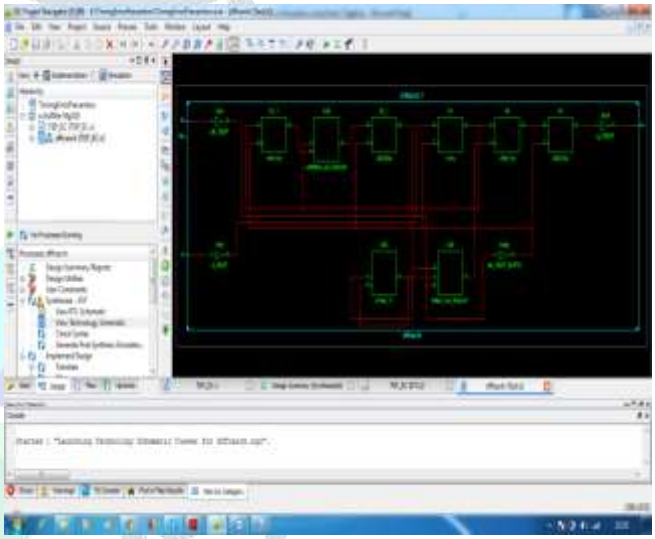


Figure 11: Technology Schematic for Dynamic Timing Error Avoidance technique

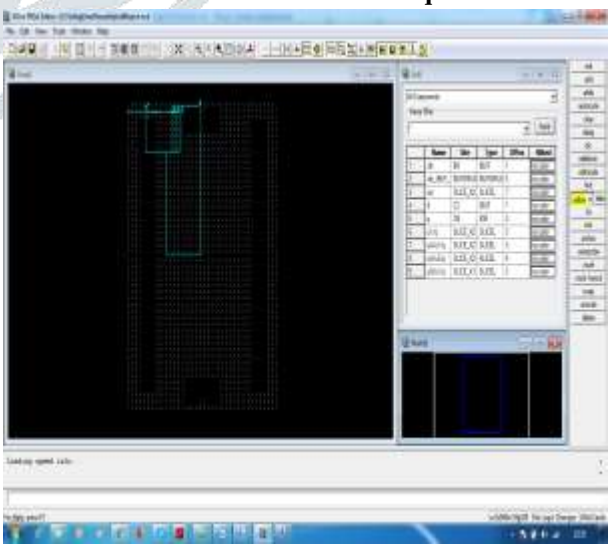


Figure 12: FPGA Implementation for Dynamic Timing Error Avoidance technique

The simulation waveform for timing error prevention by using synchronizer and flip-flops is shown in figure 12 where clearly the extracted clock minimizes the timing errors better

than the previous designs. The modelled design of timing error prevention by using synchronizer and flip-flops is converted to register transfer logic by the Xilins synthesizer as shown in figure 13 and to 90nm CMOS technology based LUT mapped schematic as shown in figure 14. The timing error prevention by using synchronizer and flip-flops design extracted for FPGA along with its sample routing without imposing constraints is shown in figure 15.

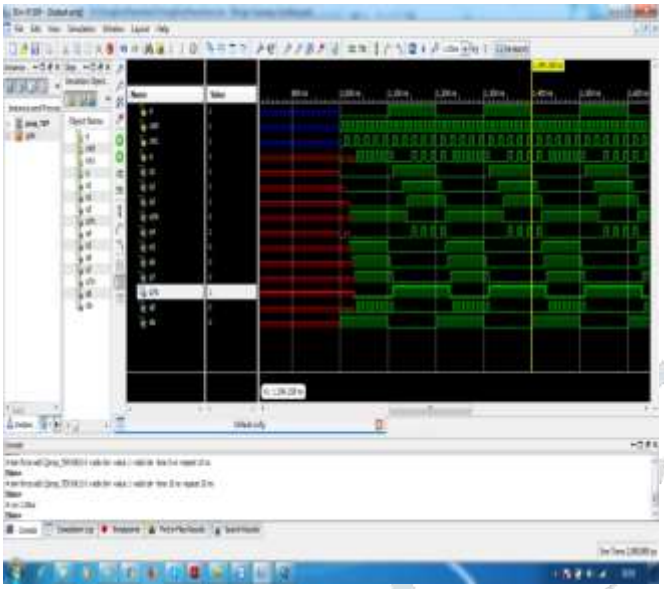


Figure 13: Simulation Result for timing error prevention by using synchronizer and flip-flops

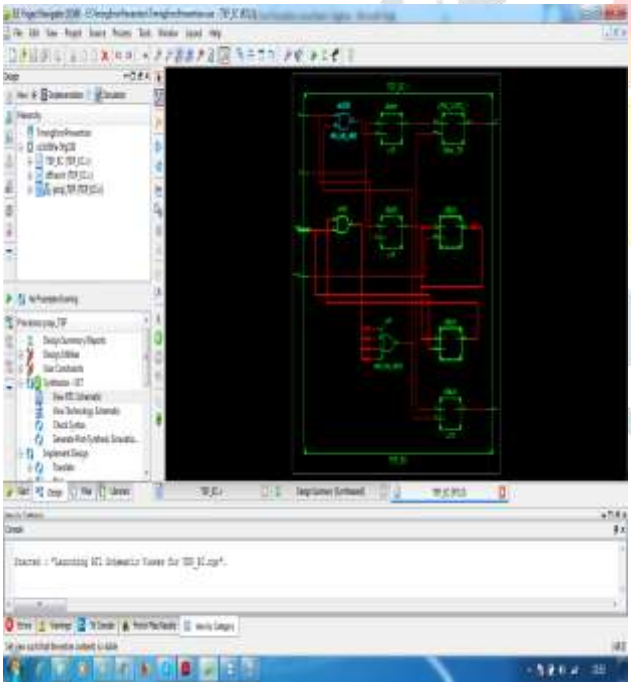


Figure 14: RTL Schematic for timing error prevention by using synchronizer and flip-flops

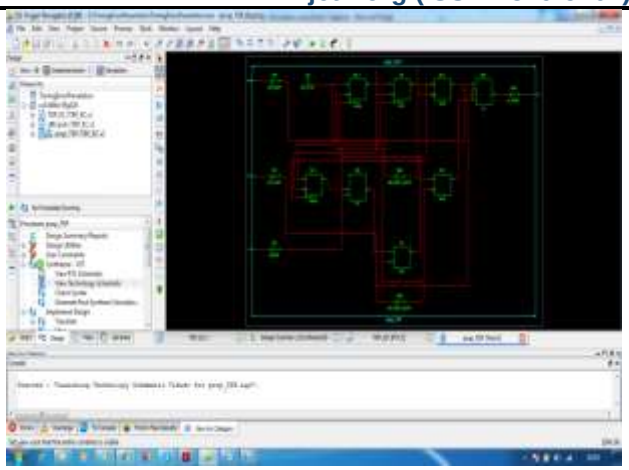


Figure 15: Technology Schematic for timing error prevention by using synchronizer and flip-flops

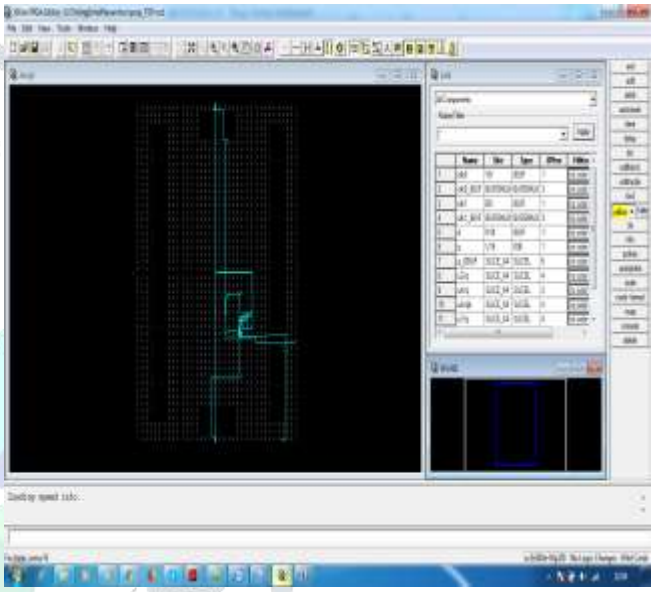


Figure 16: FPGA Implementation for timing error prevention by using synchronizer and flip-flops

Table 1: Comparison Table for area occupied by the designs

Design	Number of Slices	Number of 4-input LUTs
Timing Error Prevention using Elastic Clocking	5 out of 4656	5 out of 9312
Dynamic Timing Error Avoidance technique	2 out of 4656	3 out of 9312
Timing error prevention by using synchronizer and flip-flops	3 out of 4656	2 out of 9312

The table 1 shows that the number of 4-input LUTs used are 33.33% less in proposed design i.e., Timing error prevention by using synchronizer and flip flops but a slightly increase is observed i.e., 33.33% in number of slices when compared to dynamic timing error avoidance technique. The proposed design uses 60% less number of 4-input LUTs and 40% less number of slices when compared to timing error prevention using elastic clocking.

Table 2: Comparison Table for fanout that can be supported by the designs

Design	Average Fanout of Nonclock Nets
Timing Error Prevention using Elastic Clocking	1.57
Dynamic Timing Error Avoidance technique	1.67
timing error prevention by using synchronizer and flip-flops	1.38

The table 2 shows that the average fanout of nonclock nets decreased by 12% when compared to timing error prevention using elastic clocking and 17.4% when compared to dynamic timing error avoidance technique which is actually undesirable for a good design.

Table 3: Comparison Table for Power Dissipation of the designs

Design	Logic Power	Signal Data Power	I/O Power
Timing Error Prevention using Elastic Clocking	0.00001	0.00002	0.00214
Dynamic Timing Error Avoidance technique	0.00000	0.00001	0.00005
timing error prevention by using synchronizer and flip-flops	0.00000	0.00001	0.00109

The table 3 shows that the power dissipation variations are almost negligible for the proposed design. Hence the proposed is well suited for practical applications where timing error predominates than the other errors.

5. CONCLUSION

Time borrowing techniques have been widely used to mitigate the timing errors in high-performance designs. The existing techniques include the timing error prevention by using elastic clocking and dynamic flip-flop conversion technique where flip-flops convert dynamically into transparent latches to grant the time borrowing from the next stage and prevent setup time violation. But these techniques were unable to prevent the timing violation in the successive critical path (SCP) and critical feedback path (CFP) structures. The proposed technique uses glitch free clock switching for unrelated clocks which is more effective in terms of the performance improvement and less area utilization when compared with the best existing technique. The designs are modelled in Verilog HDL and are functionally verified by using Xilinx ISIM Simulation Tool. The designs are synthesized for Spartan3E FPGA by suing Xilinx ISE 14.5 Tools for the device XC3S500E with a package of FG320 and a speed grade of -5. The simulation results prove that the timing errors are almost suppressed by the proposed technique. The synthesis results proved that nearly 33% of area is saved with slight acceptable variations in average fanout of nonclock nets and power dissipated.

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