Reduce Static Power Dissipation in CMOS-DRPTL Adder Topologies

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Abstract: **With the revolution in integrated circuits, great emphasis was given on performance and miniaturization. Speed, area and power became the main criterion upon which a VLSI system is measured in terms of its efficiency. For high performances of the execution cores in the logic and arithmetic logic unit the efficiency of energy is essential. For highest power density of the processor block is a part of the adder. It creates a thermal hot spots and sharp temperature gradients to operate the system with the circuit which have high performance. The multiple ALUs presence in modern superscalar processors and execution cores of chip further associate with aggravates the problem by impacting circuit reliability. It increases the cooling costs for the purposes of design. Basically the adder circuit is designed to achieve low power and less delay and by logic gate of the circuit improves the performances. For speed process high logic circuit is implemented and also to have less propagation. In hybrid CMOS design style various adder cells and transistor is used, but in proposed circuit Dual Rail Signal System (DRPTL) is implemented with the load condition and the clock signal to manage the power flow in the circuit and the process is performed in an efficient way in terms of its gate count and thereby on power and speed.**

Index Terms*: *Dual Rail Signal System, Ripple Carry- Adder.

1. INTRODUCTION

In the past years, many digital applications are designed for scaling down the area of circuitry. Nowadays all the applications like cell phone, laptop have reduced in size tremendously. It is always desirable to reduce area, power and delay for any submicron circuits[1]. Adder circuits are the fundamental element present in most of the digital circuitry. It is used in most of the DSP and microprocessor circuits. Addition is the fundamental operation to perform most of other useful operations like subtraction, multiplication, division, address calculation etc. Adder circuit which is a part of the critical path has vital role is deciding the efficiency of the system.

The total Power dissipation in a CMOS circuit is given as:

Ptotal= Pswitching + Pstatic + Pshortcircuit

Taking into consideration the Static Power dissipation, let us consider a simple CMOS inverter. In ideal cases, when input to the gate terminal is 0, the NMOS is off and PMOS is on and vice versa. So at all times, only one MOS is on and other off. So ideally no leakage current in this operation. But there can be leakage current during this operation, which is a leakage between diffusion region and substrate region of MOS, as per the parasitic diode model. So this leakage current constitutes the static power dissipation and is given by:

*PStatic = VDD * ILeakage*

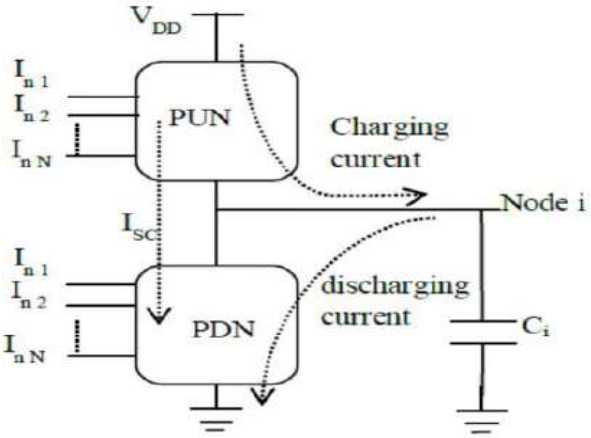


Fig 1: Switching and short-circuit current elements in static CMOS

The Dynamic power dissipation occurs during switching. While switching either from 1 to 0 or from 0 to 1, for a short duration, both NMOS and PMOS are on. At that time a small short circuit current(ISC) flows from VDD to Ground and the dynamic power dissipation occurs.

*PShortCircuit = VDD*ISC*

$$P_{Switching} = \sum_{i=0}^{N} \alpha_i C_i V_{DD} V_{Swing} f_{clk}$$

where αi is the switching activity at node i. i

Propagation delay is how quickly the circuit responds to the change in input and is given by:

$$T_d \alpha \frac{C_L V_{DD}}{k(V_{DD} - V_{TH})^{\alpha}}$$

Where α refer the velocity index saturation.

In well-engineered deep submicron CMOS technologies, the difficult criteria are concentrating on emerging communication process high speed with low

power in digital signal processing chip. In the process of arithmetic division, the multipliers and adder are used widely in VLSI system [2]. Since last decades, the growth of the application in electronics is high and it's major in semiconductor industry. However, reduction of power consumption, delay and area are the critical fear in the logic circuits of any application. [2] The explosive growth and the demands are high in convenient electronic product, high speed, battery life's, area and the reliabilities of the circuits. [3] In various logic circuits and algorithm like parity checker, converter of code, compressors and error correcting code or detector are basically used the building blocks of XOR-XNOR circuit.

The VLSI circuit power consumption is specified as static power, dynamic power and short circuit power. If the transistors of CMOS (NMOS and PMOS) are active for short duration at a time, then this dissipation of power is short circuit power. As well as the static power will be various the technology of process. But dynamic power depends on load capacitance charging and discharging. The dominant dynamic power is given as

Dynamic Power = α (VDD) 2 f CL (6)

Where, α denotes the activities of switching, voltage supply as VDD and frequency of switching the load capacitance as f.

This paper is organized as introduction to design of SRAM and its architecture in section I, Existing Design in section II, power gating techniques in section - III and proposed design i.e., SK-LCT Technique in section-IV. The results are discussed in section -V and finally the paper is concluded.

2. EXISTING METHODS

In existing design use two methods. One method is The hybrid CMOS design uses the Pass transistor logic and Gate Diffusion Technique (GDI) techniques and another method is dual rail pass transistor logic.

(i) Hybrid CMOS Design

The hybrid CMOS design uses the Pass transistor logic and Gate Diffusion Technique (GDI) techniques.

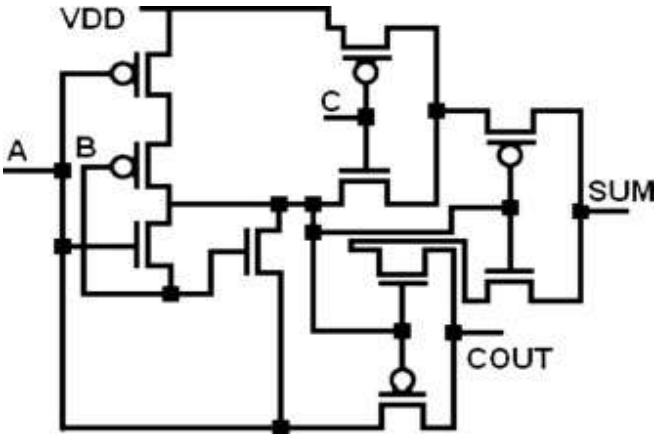


Fig 1: CMOS Design Using Pass Transistor Logic

In this logic, Pass-Transistor is processed with the design of low power circuit. In pass network transistor is generated according to its function and perform sum and carry function as per the signal of a clock. At the end of generating voltage swing of the logic is performed. This logic provides improvement in speed, eliminating short circuit current in the output of inverter and includes voltage level restoration. [10-12] The DRPTL logic leads to have an efficient implementation with a clock signal for efficient dynamic access. It provides fast process and dynamic synthesis of logic functions in transistor network.

(ii) Dual rail pass transistor logic

The dual rail pass transistor logic improves the dynamic circuit speed with the evaluation of clock signal logic with transistor. The supply of voltage is varied based on the charges phases. If the clock signal is equal to 1 in the evaluation phase, then the circuit will be discharged or pre-charge and if equal to 0 in pre-charge phase, then the circuit is charged and applies to voltage supply level from the transistor

The process of dual rail signal and single rail system is shown in Fig.2. The proposed logic improves the dynamic circuit speed with the evaluation of clock signal logic with transistor. The supply of voltage is varied based on the charges phases. If the clock signal is equal to 1 in the evaluation phase, then the circuit will be discharged or pre-charge and if equal to 0 in pre-charge phase, then the circuit is charged and applies to voltage supply level from the transistor. Normally the power density and dissipation are the main objective and rapid growth in portable systems. In VLSI design, the widely used adder component provides better performances in the integrated circuit.

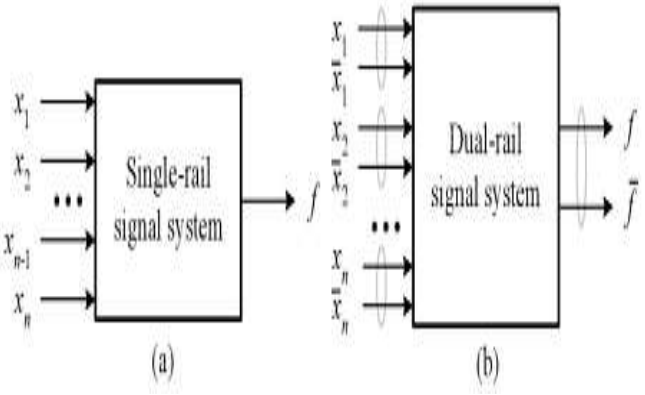


Fig2: (a) Single Rail Signal System, (b) Dual Rail Signal System

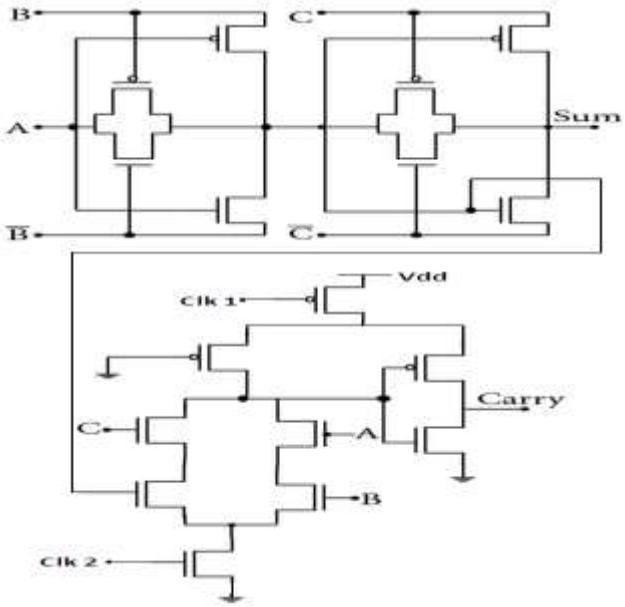


Fig 3: Hybrid Full Adder Topology

With the revolution in integrated circuits, great emphasis was given on performance and miniaturization. Speed, area and power became the main criterion upon which a VLSI system is measured in terms of its efficiency. In any VLSI system, a full adder is widely component, which also decides the performance criteria of the system. Basically the adder circuit is designed to achieve low power and less delay and by logic gate of the circuit improves the performances. For speed process high logic circuit is implemented and also to have less propagation. In hybrid CMOS design style various adder cells and transistor is used, but in proposed circuit Dual Rail Signal System (DRPTL) is implemented with the load condition and the clock signal to manage the power flow in the circuit and the process is performed in an efficient way in terms of its gate count and thereby on power and speed.

3. PROPOSED DESIGN

The optimized Pass Transistor logic as an alternative to reduce static power dissipation and avoids threshold voltage loss.

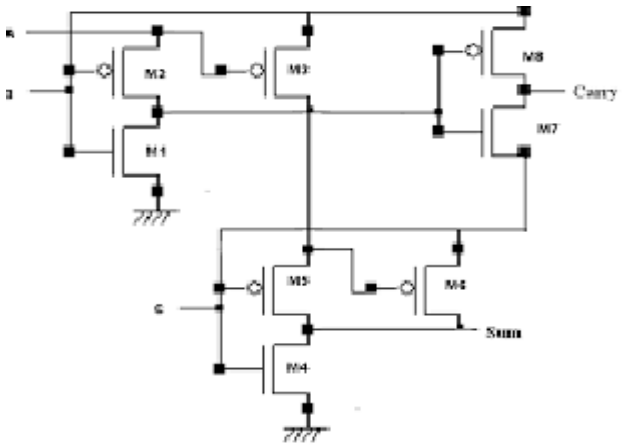
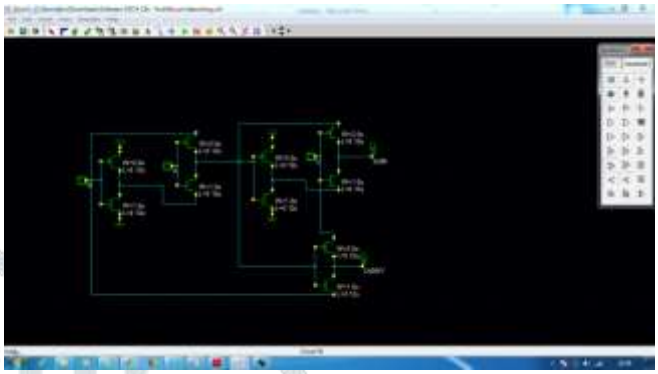


Fig 4: Proposed architecture

Complementary pass transistor logic. ... Other authors use the term "complementary pass transistor logic" (CPL) to indicate a style of implementing logic gates where each gate consists of a NMOS-only pass transistor network, followed by a CMOS output inverter

5. SIMULATION RESULTS

The designs are developed in Digital Schematic, where their functional verification is performed. Also the corresponding Layouts are developed in 120nm technology and are simulated.



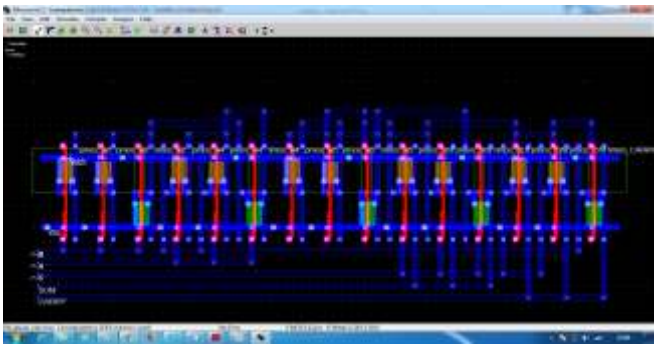
(a)

(b)

Fig.5: The schematic and the corresponding functional simulation of existing CMOS pass transistor logic.

The figure 5 shows the design of CMOS pass transistor logic in digital schematic and the functional verification of the CMOS pass transistor logic Design.

The layout of the schematic developed for existing design is shown in figure 6 (a). this layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 6(b).



(a)

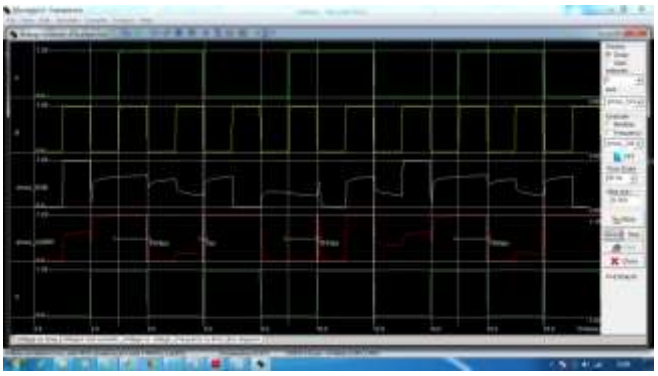
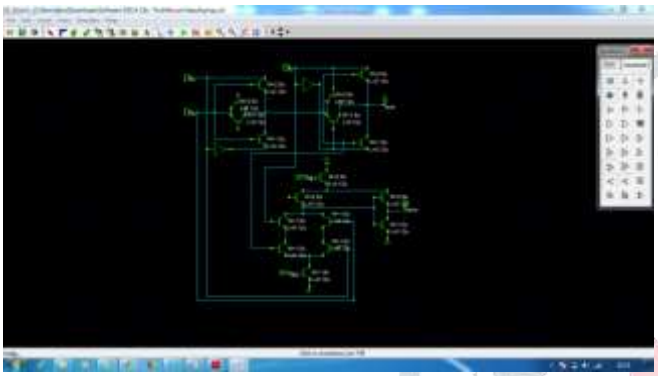
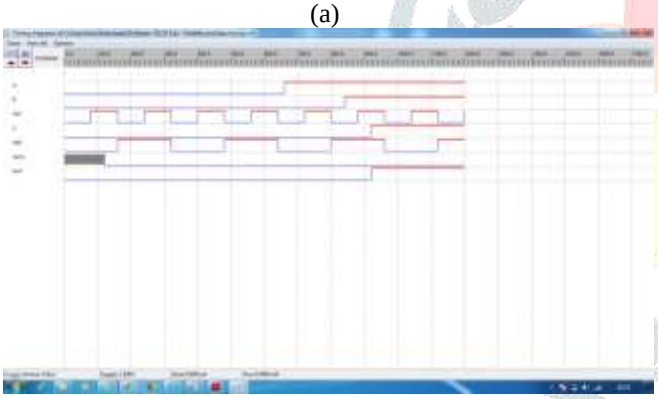


Fig.6: The layout and simulation waveform of the existing CMOS pass transistor logic design for the schematic shown in fig.5.



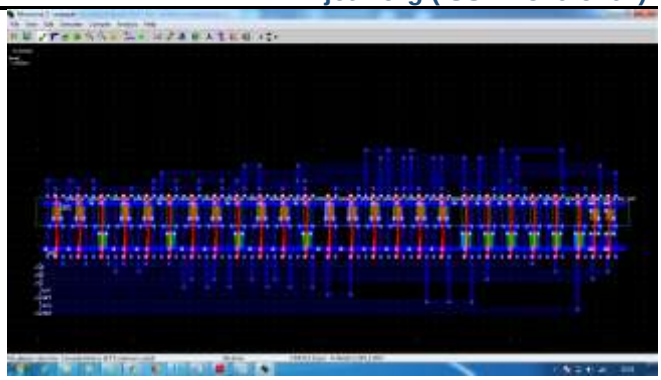
(a)



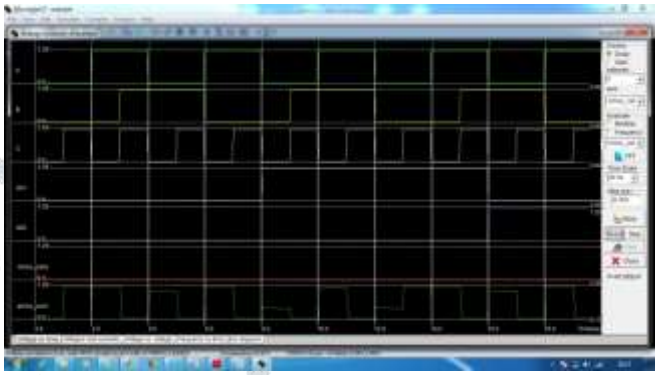
(b)

Fig.7: The schematic and the corresponding functional simulation of existing Dual rail pass transistor logic design.

The figure 7 shows the design of dual pass transistor logic in digital schematic and the functional verification. The layout of the schematic developed for existing dual pass transistor logic design is shown in figure 8 (a). This layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 8 (b).

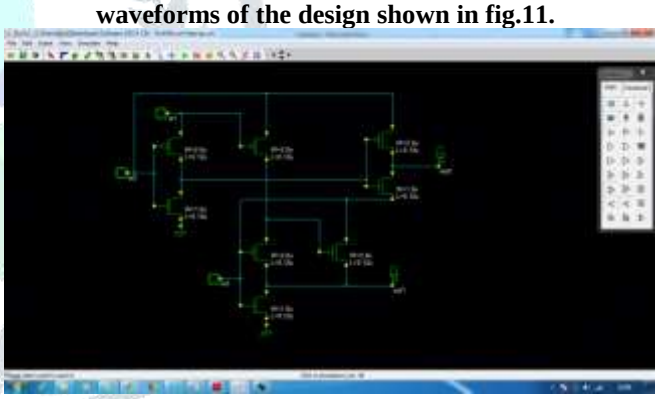


(a)

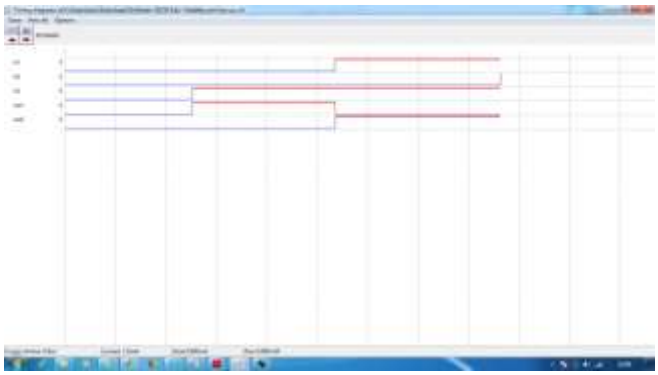


(b)

Fig.8: The layout and the corresponding simulation waveforms of the design shown in fig.11.



(a)

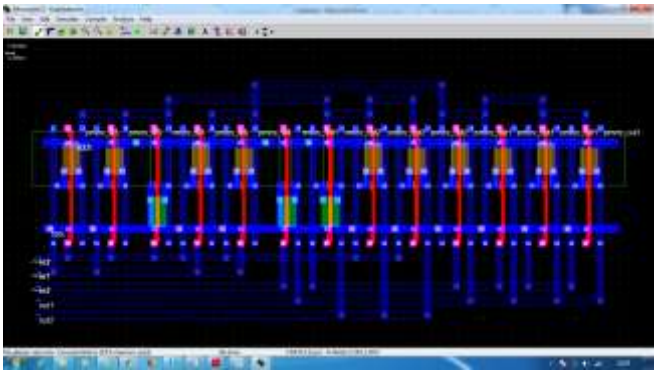


(b)

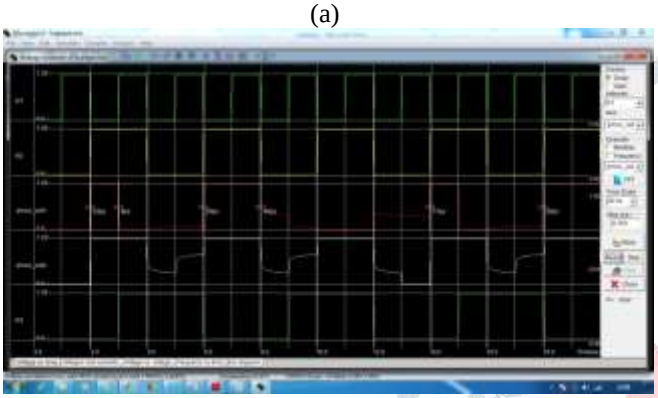
Fig.9: The schematic and the corresponding functional simulation of proposed system.

The figure 9 shows the design of proposed system in alternative form by using digital schematic and the functional verification..

The layout of the schematic developed for proposed system is shown in figure 10 (a). This layout is developed in 120nm and the corresponding waveforms are simulated as shown in figure 10 (b).



(a)



(b)

Fig.10: The layout and the corresponding simulation waveforms of the design shown in fig.9.

Table .I: Comparison Table

Parameters	Existing	Author Proposed	Proposed
Area Occupied	9.7%	5.6%	5.0%
Power Dissipation	8.934µW	40.295µW	≈0nW
No. of Transistors Used	10	21	8
Output	Acceptable	Acceptable	Acceptable

From the tables 1 and 2, The proposed designs i.e., the design of The optimized Pass Transistor logic as an alternative to reduce static power dissipation and avoids threshold voltage loss.

5. CONCLUSION

In digital design of submicron circuits, an internal logic circuit is proposed with the proposed approach to design and implement the circuit for efficient performances and analysis than the existing circuit. The proposed approach of the hybrid circuit provides faster process, less delay propagation, less power consumption and reduction in transistor count than the others. The DRPTL technology performance was with regard to the delay and power consumption of the submicron adder circuits used in digital circuitry. So the modified circuits satisfied VLSI requirements of an efficient submicron adder circuits. In the proposed system using optimized Pass Transistor logic as an alternative to reduce static power dissipation and avoids threshold voltage loss.

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