DESIGNING CLASS E RADIO FREQUENCY POWER AMPLIFIER WITH CMOS TECHNOLOGY

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Abstract : The CMOS technology has been applied in several executions. Its reason is that it is capable to reduce cost & size & at a time without extra power. Several topologies and design strategies are there. These topologies & design strategies work along with amplifiers formulation. In this research paper the work related to power amplifier has been explained. The paper has discussed the class e radio frequency power amplifier with CMOS Technology. The circuit design and its implementation have been represented in this paper. Result and discussion has been simulated finally giving conclusion of work. The design of class e RF has been represented along with design equation.

***IndexTerms* - Power amplifier, CMOS Technology, Class E RF.**

I. INTRODUCTION

PA stands for Power amplifier has been referred last block of transmitter system. It provides the amplification of a weak signal to a power level. It has been done due to its need to send a signal. Such may be defining as big signal amplifiers. It is the fact that there must be huge voltage of input signal to achieve a large signal power at output. PAs has been divided into audio power amplifiers and RF power amplifiers. This categorization has been made on the base of apps. Generally, power amplifiers have been applied to drive antennas within a system of transmitrte. It makes increment in power of signal because it is the last block in a system. Therefore, it has been made easy for antenna to send in a wide area. Linearity and Efficiency are basic factors in a power amplifier. In past decades, power amplifiers are designed applying technology of CMOS. The cause for this may be decreased cost, requirements of low power supply. Better integration as well as the good performance is also considered.

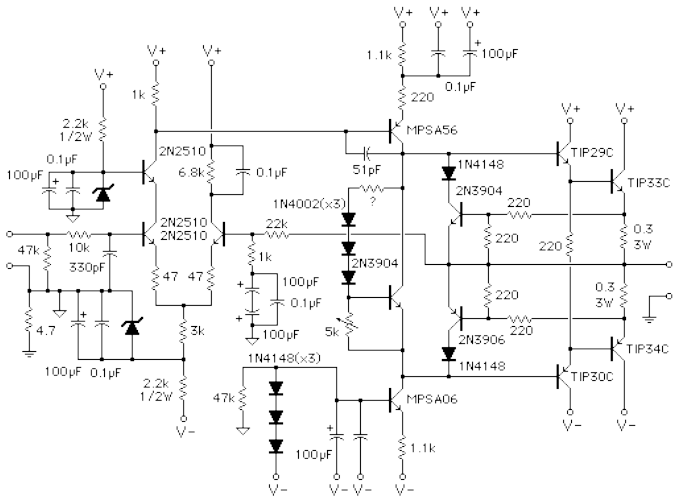

Fig 1. Power Amplifier

A) Related work

There have been several researches that are representing methods to improve the performance of multi-stacked CMOS millimetre wave power amplifiers. Some researchers are representing design of DAC depenent RMS Power Detector for RF Applications. Several research focuses on fully differential D-band CMOS power amplifier. Moreover some of them considered low-power CMOS RF power detector. The chapter has discussed several researches along with these objectives.

In 2018, Mohammad Hassan Montaseri [1] wrote paper to present Performance to improve the Multi-Stacked CMOS mm-Wave Power Amplifiers dependent on Negative Capacitance Phase Compensation.

In 2018, Ivan Sejc[2] made research paper to represent design of DAC dependent RMS Power Detector in cases of RF Applications.

In 2017 Xianghong Gao [3] wrote research on three stage. They consider the fully differential D-band CMOS power amplifier. The research work has provided the design and implementation related to three stage complete differential D-band.

In 2016 Eli Schwartz [4], introduced 20dBm configurable linear CMOS RF power amplifier. It is applicable in multi-standard transmitters. Concept related to PA design in CMOS for 802.11ac. It is able to achieve the -35dB EVM. Here the output power has been considered which is higher than 100mW and EVM floor of -47dB has been explained.

In 2016, Gabor Varga[5] provide the design of an CMOS which is useful RMS RF power detector. It has been used in cognitive radio applications. Dynamic range RMS power detector is made. It is applicable in applications of broadband frequency agile for example cognitive Radio.

In 2015, Aritra Banerjee [6] described high efficiency multi-mode out phasing RF PA. It was discussed with in 45nm CMOS. Performance of P multi-mode class-E outphasing RF PA has been considered here. Along with this, they considered the combine circuit.

In 2015, Soroush Dehghani [7] explained the tracking load for the optimization of power efficiency. This efficiency is related to RF from DC rectifier circuits. Tracking load circuit used in RF rectifiers has been considered here. The tracking load has been formulated for the maximization of RF from the DC conversion.

2 TECHNOLOGIES

A) Power amplifier

Now power amplifiers have been categorized into several classes on the base of operations mode for example Class A, B, AB, C, D. Amplifiers of Class A has been affected in a particular way and these are energetic to participate in input cycle. These amplifiers offer 50% efficiency which is not high. Amplifiers of Class B are efficient to perform in half input cycle. The efficiency of these amplifiers is more than sixty percent. Class AB can be defined as an intermediate of Class A and B. Therefore, it remains active in most of time. Today mostly designers use the Class AB amplifiers. The reason is that it is sufficient to provide the services with comparatively low input power. Therefore, efficiency of Class C amplifiers is able to reach up approximately eighty percent. Generally Class D amplifiers have been applied in case of pulse width modulation. These are designed to perform with digital and signals that is pulse type.

It is not easy to make design of the PA. Previously BJTs that stands for Bipolar Junction Transistor had been utilized to fabricate the amplifiers. Thus with expansion of CMOS methodology, MOSFETs are got large applications to fabricate the analog and digital circuits. On the opposite side, applying MOSFETs, one can use its consequences. For instance, degradation techniques have been connected with MOSFETs. For example; gate-oxide break down, etc., are able to effect the CMOS power amplifiers' operation. In the research work, the comparison of several power amplifiers designs is formulated with use of CMOS technology.

B) Class e radio frequency power amplifier

L1 is a choke with unidentified number of turns on a mallard FX2243 pot core, the wire is 14 SWG enamalled and the core is 50 mm diam 5.4Mh. below figure is representing class E P.A design

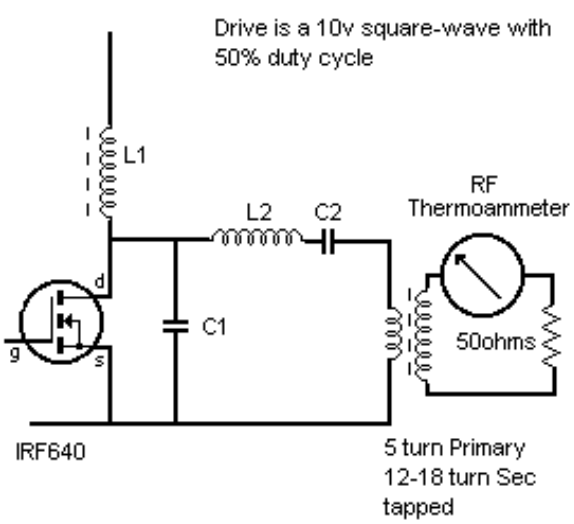

Fig 2 Procedure to design Class E Power Amplifier Design

Class-E conditions are satisfied when switch closes at

$\omega t = 2\pi n$:

$$V(\omega t)|_{\omega t=2\pi n} = 0$$
$$\frac{d}{d(\omega t)} V(\omega t)\Big|_{\omega t=2\pi n} = 0.$$

The voltage across switch has been provided by V (wt) and current via switch is represented by I(wt). it has been made at any instant in normalised time wt. For expediency, a table has been presented here which shows the variables relevant.

C) CMOS technology

CMOS refers to the complementary metal oxide semiconductor. This technology is technology applied for construction of ICs. It also used in digital logic circuits, microprocessors, microcontrollers & static RAM. Along with this, several analog circuits also used this technique. Beside of this CMOS technology is helpful in data converters, image sensors as well as in highly integrated transceivers.

CMOS Working Principle & Applications: Complementary Metal Oxide Semiconductor technology is full form CMOS technology. It is famous methodology used in computer chip design trade. This technique is also applied in order to form integrated circuits when there are several & various applications.

CMOS over NMOS logic carries advantages. The benefit is that **low**-to-high with output transitions which is high-to-**low** have been considered vast. The reason is that PMOS pull-up transistors carry less confrontation at time of switch on. It is not like load resistors in NMOS logic. Additionally, output signal moves backwards & forwards full voltage in **low** and high rails.

The CMOS technology has been considered less power debauchery. This technology is not like NMOS or BIPOLAR circuits. It has lack of static power dissipation. Power is merely debauchery when circuit would be actually switches. It enables integration of more CMOS gates on an IC as compare to NMOS or bipolar methodology. So result would be best in performance. CMOS consist of P-channel MOS (PMOS) and N-channel MOS (NMOS).

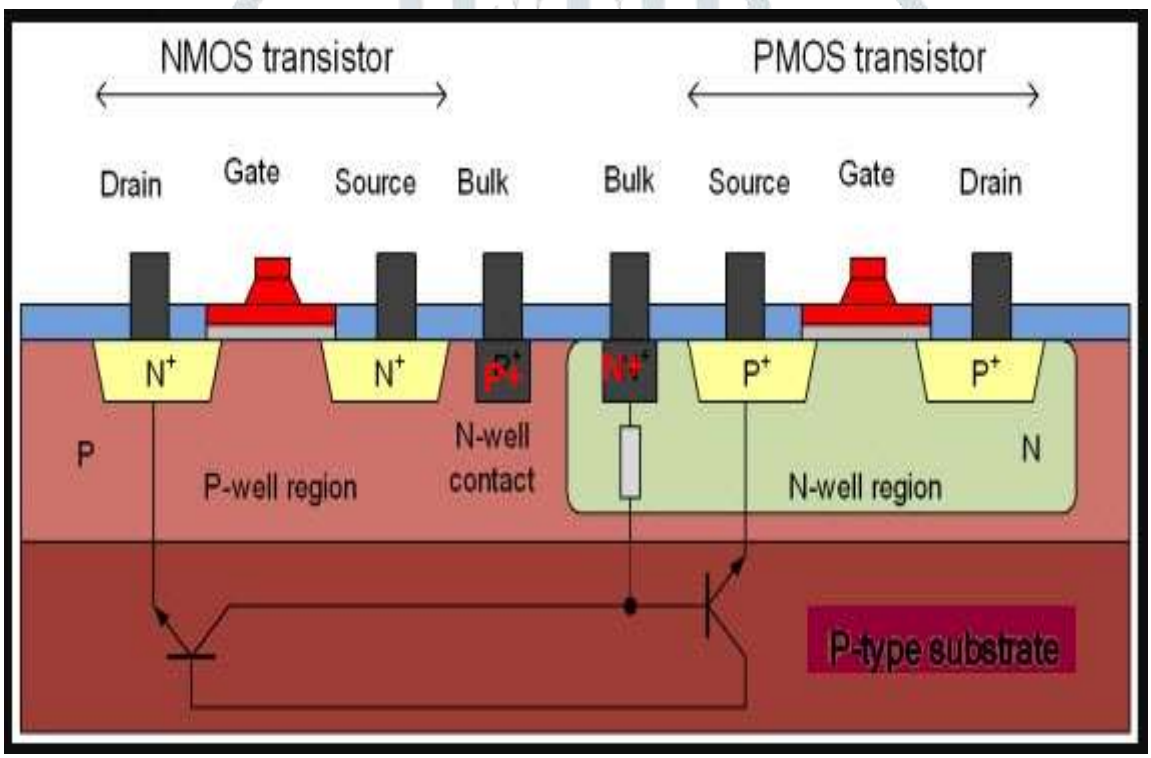

Fig 3 CMOS with PMOS and NMOS

3 CIRCUIT DESIGN AND IMPLEMENTATION

The circuit design of class e amplifier is shown below

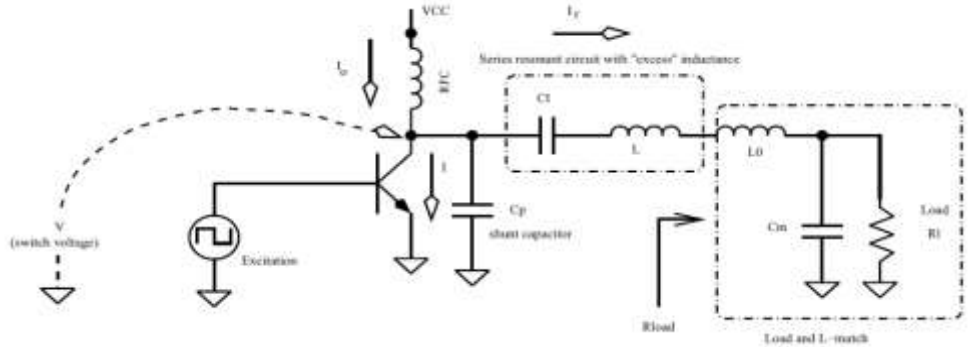

Fig 4 Class E applifier

4 MEASUREMENT RESULTS

Class-E conditions are satisfied at the time of switch close at $\omega t = 2\pi n$:

$$\begin{aligned} V(\omega t)|_{\omega t=2\pi n} &= 0 \\ \frac{d}{d(\omega t)}V(\omega t)\Big|_{\omega t=2\pi n} &= 0. \end{aligned}$$

The voltage across switch has been indicated by V (wt). Current via switch has been indicated by I(wt) at any instant in normalised time wt. For expediency, a table related to variables relevant to evaluation has been presented here..

Using results of 2, current through capacitor immediately after switch closes must be zero, i.e.

$$I_c(\omega t) = \omega C \frac{d}{d(\omega t)} V(\omega t) = 0.$$

Design procedure

1. Choose a Power Supply voltage (Vdd)
2. It ensures Vdd(max) of FET at approximately 3.5 times Vdd
3. Choose the target power level
4. It ensures optimum value related to C1 and optimum load impedance
5. Consider the C2 and L2 values from worksheet of Excel.

DESIGN EQUATION OF HF CLASS E RF POWER AMPLIFIER

```
v=2.4
p=3
w=2*3.14*2.4*1000000000;
Q=12
rl=20
I=p/v;
C=I/(w*3.14*v);
R=(8*power(v,2))/((3.14*3.14 + 4)*p);
Lext= (1.153)*R/w;
Cl= 1/(Q*R*w);
Lres= Q*(R/w);
Cm= (1/(w*rl))* sqrt((rl/R)-1);
Lo= R*rl*Cm;
Cm
Lo
I
C
R
Lext
Cl
Lres
```

Table 1 Design Equations for Class-E LF Power Amplifier

Design Equations for Class-E LF Power Amplifier						
Design Frequency =	136900	Hz				
VRBcev or Vddmax	200	volts				
Vce(sat)	1	volts	Maybe Ic(pk)*rdss is best guess for a FET			
Pout	160	watts				
w =2*pi*F	860170.08					
Ql	7.2	must be greater than 1.8				

Vcc (Vdd) must be less than		56.866929	volts			
Select a value for Vcc (Vdd)		38	volts			
Peak voltage Vcc(pk)		132.79	volts			
Peak current Ic(pk)		12.78	amp			
	Q	R	C1	L2	C2	Resonance
		ohms	nF	uH	nF	L2C2
for selected Q	7.2	4.94	47.76	41.31	39.43	124707.52
	2	4.94	52.00	11.48	734.18	54832.95
	3	4.94	51.33	17.21	150.43	98908.18
	4	4.94	50.25	22.95	88.44	111711.91
	5	4.94	49.29	28.69	63.39	118018.63
	6	4.94	48.50	34.43	49.61	121789.90
	7	4.94	47.87	40.16	40.82	124302.29
	8	4.94	47.37	45.90	34.71	126097.02
	9	4.94	46.96	51.64	30.20	127443.55
	10	4.94	46.61	57.38	26.74	128491.29
	20	4.94	44.98	114.75	12.50	132909.58

5 SCOPE OF RESEARCH

The proposed amplifier is 0.64mm2 chip in size. It offers a gain of 18.4 dB. Although design influenced by parasitic, it contradicts with decoupling capacitors to ground pads. A race is there which offers five Generation technique situated in process. Generally the5G wireless services are executed in Ka-frequency band (18-28GHz). In 2016 Sherif Shakib et al used Source degeneration. It has been applied for constancy in order to make design of highly linear. Here the effective PA has been determined in twenty eight nm technology. Byungjoon Park et al provided the design of a Ka-band linear PA. Two stack deep class AB PA is formulated in order to offer linearity and high gain.

6 CONCLUSIONS

This research has presented PAE% according to frequency. Comparison chart of Tradition researches where frequency was 5.2 to 13 ghz , 4 to 17 ghz, 6.5 to 13 ghz, 0.1 to 65 ghz,0.2 to 2.5 ghz in proposed research frequency 2.4ghz has been represented. Output power & power gain has been simulated in this section. Multi mode class e radio power amplifier has been using thirty nm CMOS technique with programming. This research has proposed updated CMOS RF Power Amplifier system. The proposed system generated for Low Power five generation Wifi Networks.

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