Design and Parameter Enhancement of Ultra-Low Power 18-Transistor Single-Phase Clocked Flip-Flop

Raj Kumar Singh[1], Braj Kishor[2], Ambresh Patel[3]

[1]M.Tech scholar, [2&3]Assistant Professor
Department of Electronics and Communication,
Sri Satya Sai College of Engineering, RKDF University, Bhopal, India.

Abstract : In CMOS, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. The most fundamental sequential circuit type that we will ponder is known as the Flip-Flop. True single-phase clock (TSPC) method of reasoning has found wide use in advanced plan. This paper proposed 18-transistor single-phase clocked (TSPCFF) design at ultra low power with 50nm technology. Simulation is done using microwind software. Simulated result shows that proposed design gives reduced area, time and power than existing design.

IndexTerms -TSPC, VLSI, Flip-Flop, Clock, RAM,ROM, SRAM, DRAM.

I. INTRODUCTION

There are several fundamental types of flip-flops. Here, we shall only consider a type called master-slave flip-flop. In addition to the fundamental types of flip-flops, there are minor variations depending on the number of inputs and how they control the state of the flip-flop. Here, we shall only consider a very simple type of flip-flop called a D-flip-flop. A master-slave D-flip-flop is built from two SR-latches and some gates. True single-phase clock (TSPC) structure also consumes less power and occupies less area than other methods

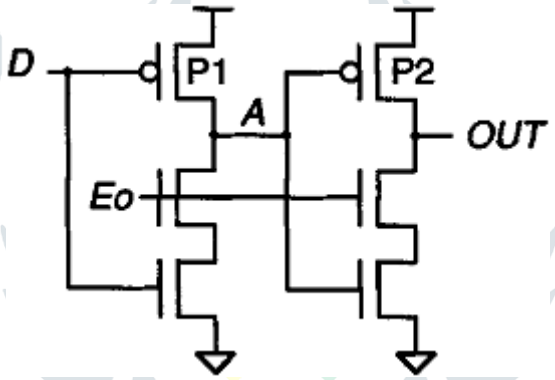

Figure 1: True single-phase clock

A clock signal is conveyed by a clock generator. But progressively complex courses of action are used, the most broadly perceived clock signal is as a square wave with a half commitment cycle, by and large with a fixed, reliable repeat. Circuits using the clock signal for synchronization may wind up powerful at either the rising edge, falling edge, or, by virtue of twofold data rate, both in the rising and in the falling edges of the clock cycle.

Clock signals are regularly stacked with the best fanout and work at the most vital speeds of any signal inside the synchronous structure. Since the data signals are given a transient reference by the clock signals, the clock waveforms must be particularly flawless and sharp. Besides, these clock signals are particularly affected by advancement scaling (see Moore's law), in that long overall interconnect lines become basically logically resistive as line estimations are decreased. This extended line resistance is one of the basic purposes behind the growing significance of clock apportionment on synchronous execution. Finally, the control of any qualifications and defenselessness in the section times of the clock signals can genuinely limit the best execution of the entire system and make calamitous race conditions in which a wrong data signal may snare inside a register.

II. TRUE SINGLE PHASE CLOCK ARCHITECHTURE

Most integrated circuits (ICs) of adequate unpredictability use a clock signal with the true objective to synchronize assorted pieces of the circuit, cycling at a rate slower than the most cynical situation inside inducing delays. Now and again, more than one clock cycle is required to play out a foreseen action. As ICs end up being more astounding, the issue of giving precise and synchronized clocks to all of the circuits ends up being dynamically problematic. The otherworldly instance of such complex chips is the microchip, the central piece of present day PCs, which relies upon a clock from a valuable stone oscillator. The principle uncommon cases are non simultaneous circuits, for instance, strange CPUs. g investigation. A clock signal may in like manner be gated, that is, got together with a controlling signal that engages or debilitates the clock signal for a particular bit of a circuit. This technique is much of the time used to extra control by successfully shutting down bits of a propelled circuit when they are not being utilized, but instead incorporates some noteworthy entanglements of extended multifaceted nature in timing examination.

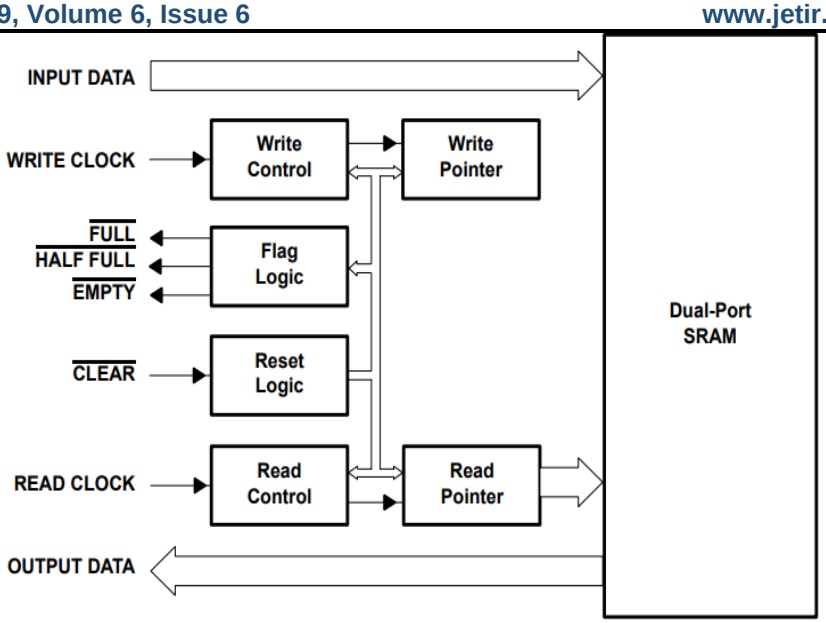

Figure 2: Block diagram of FIFO with storage

In figure 2, a long fall-through time in long FIFOs, the designing ought to never again move the data words through all memory zones. The issue is understood by an indirect memory with two pointers. In an indirect FIFO thought, the memory address of the moving toward data is in the make pointer. The area of the primary data word in the FIFO that will be examined out is in the scrutinized pointer. After reset, the two pointers exhibit a comparative memory zone. After each make task, the form pointer is set to the accompanying memory territory. The examining of a data word sets the read pointer to the accompanying data word that will be scrutinized out. The read pointer ceaselessly seeks after the form pointer. Right when the read pointer goes to the make pointer, the FIFO is empty. If the form pointer gets up to speed with the read pointer.

III. PROPOSED METHODOLOGY

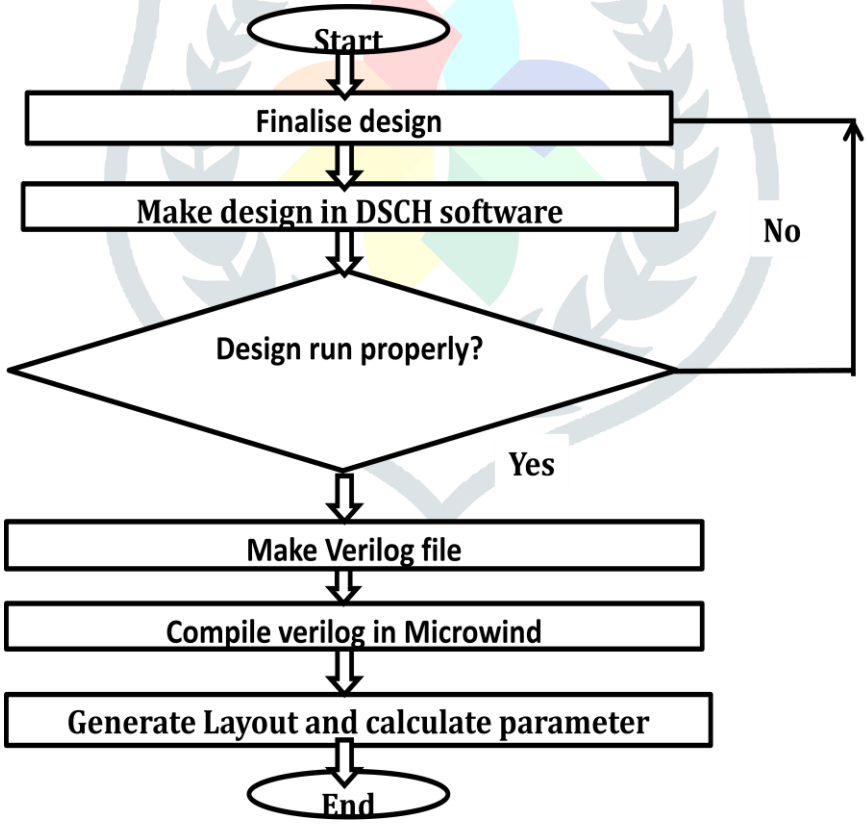

Figure 3: Flow Chart

Algorithm-

Step 1- Firstly make design in DSCH software using available component then make connection between them as per requirement.

Step 2- Now press run simulation and see output in terms of LED glow or not, if input and clock is on and led glow then designed circuit give proper output otherwise there are some errors in circuit.

Step 3- Now save this design and make verilog file, then a verilog file will be generated automatic.
Step 4- Open Microwind software and compile verilog file. Then generate CMOS layout. Now calculate parameters and compare result.
This work proposes 18-transistor SPC (18TSPC), a SPC FF with only 18 transistors (the lowest reported for a fully static contention-free SPC FF) with a novel master-slave Fig. 3. Simulation results show TCFF internal node voltages at (a) VDD = 1.2 V and (b) VDD = 0.6 V when D rising at CK = 0. topology With a simplified topology, it delivers a 20% reduction in cell area compared to TGFF. Unlike SoA designs, 18TSPC meets all ultra-low power FF design requirements. It has been implemented in 65-nm CMOS along with a TGFF. This proves EDA compatibility and demonstrates circuit and system-level benefits. The design was first simulated then experimentally validated at 0.7 V, 25 ◦C, at various data activity rate (α), showing that the proposed 18TSPC achieves reductions of 68% and 73% in overall (Pα=10%) and clock dynamic power (Pα=0%), respectively, and 27% lower leakage compared to TGFF. Furthermore, unlike TCFF, the measurements indicate superior 18TSPC in performance.

IV. SIMULATION AND RESULT

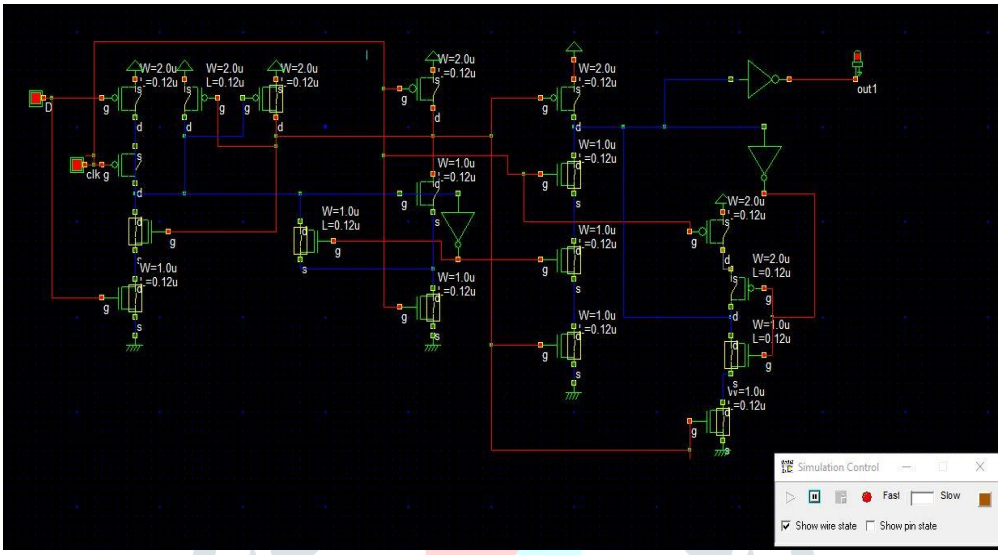

Figure 4: Proposed 18-transistor single-phase clocked (TSPCFF)

Figure 4 showing design of transistor single-phase clocked. AND gate, PMOS and CMOS component are using to design this circuit. To check result, when clk=1 d=1 then output=1.

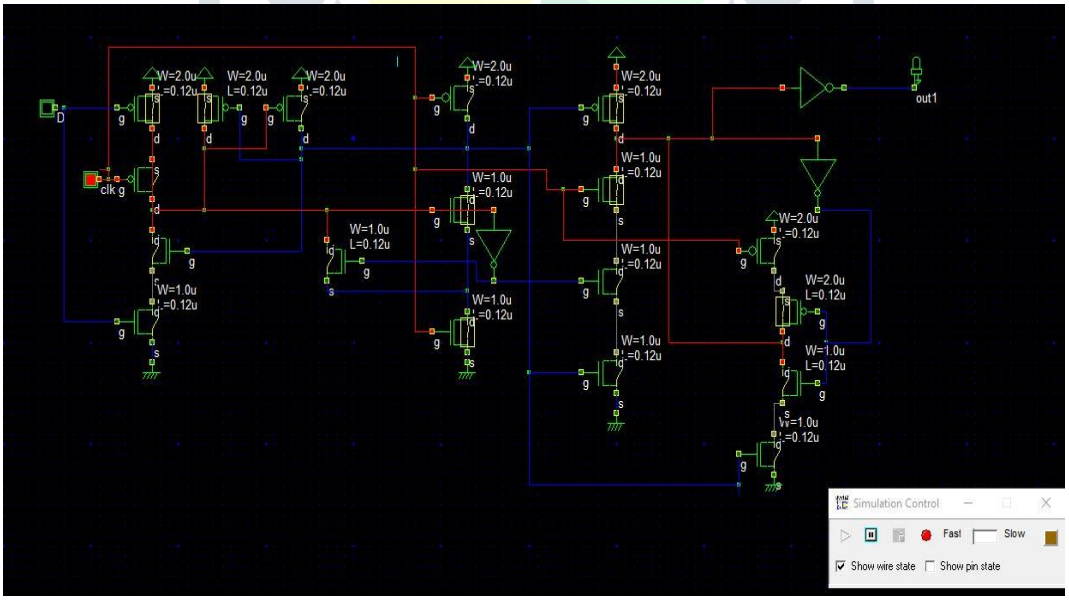

Figure 5: Proposed 18-TSPCFF

Figure 5 presenting, 18-TSPCFF when clk=1 d=0 and out=0, and when clk=0 d=1 and output=0

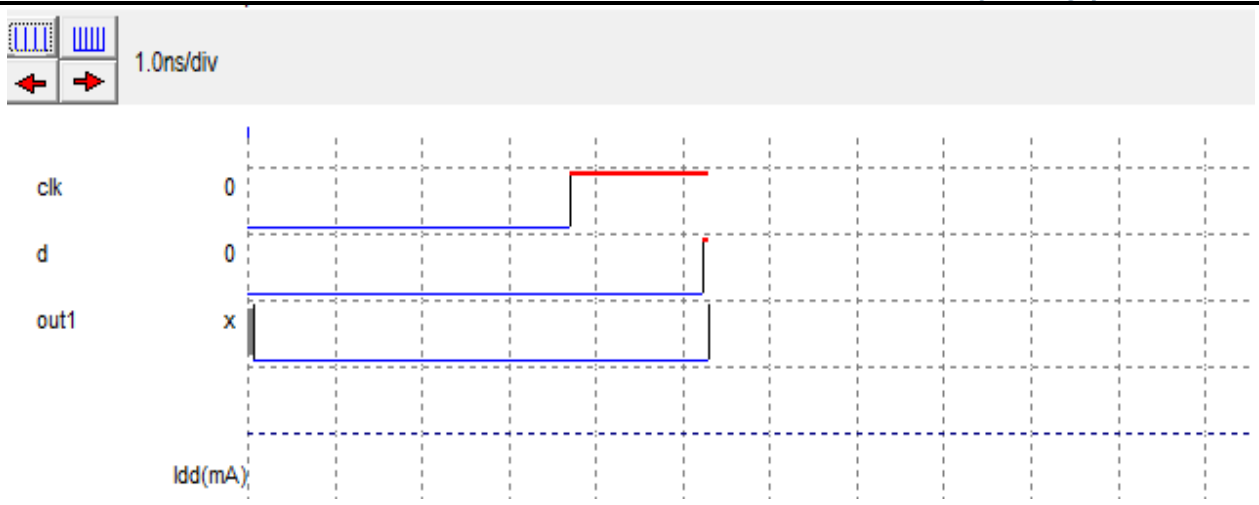

Figure 6: Timing diagram of 18-TSPCFF

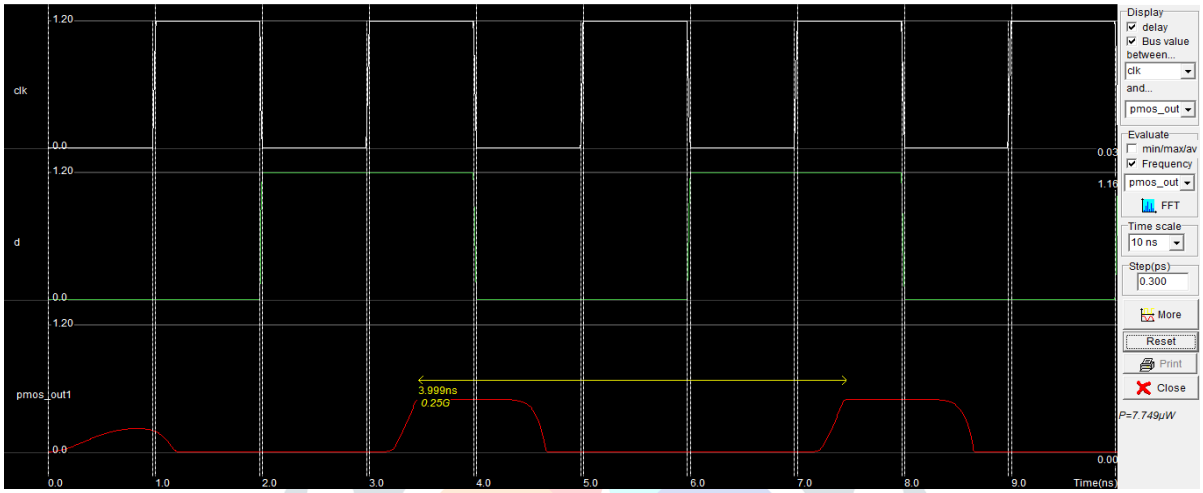

Figure 7: Voltage vs time of 18-TSPCFF

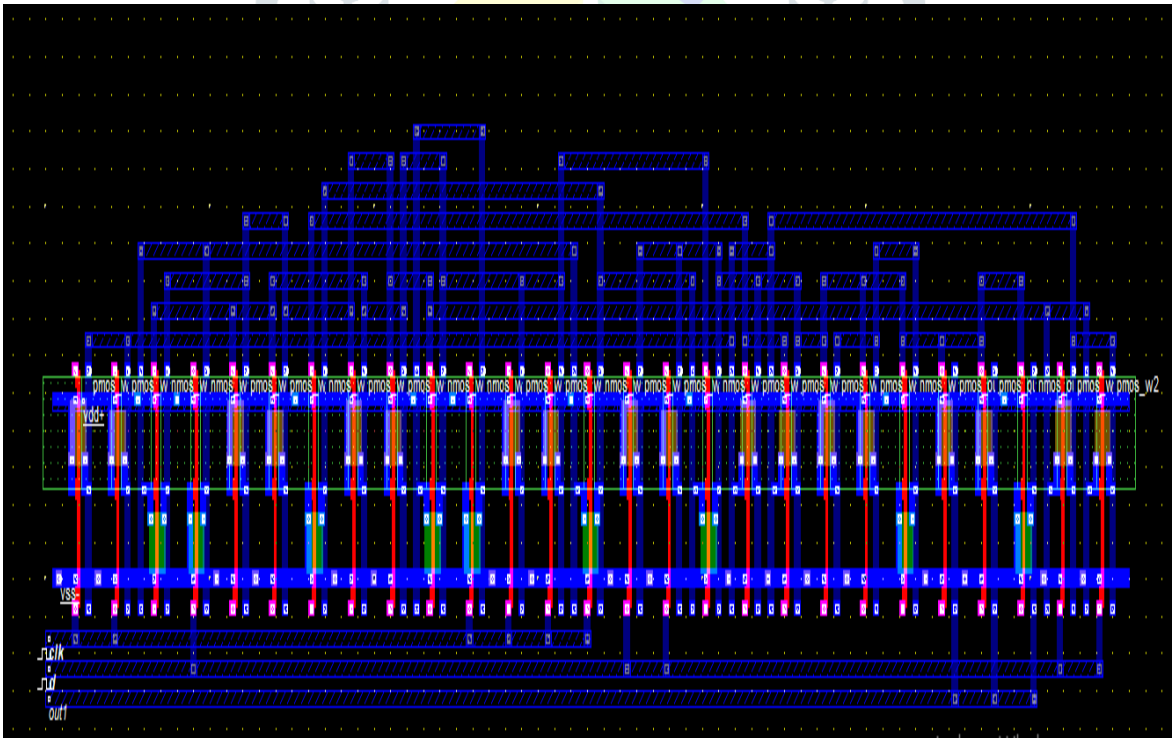

Figure 8: Layout of 18-TSPCFF

Table 1: Simulation Parameter of 18-TSPCFF

Sr No.	Parameters	Value
1	Area	374.0µm
2	Power	7.749µW
3	Delay	7ns
4	Power Delay Product (PDP)	542.43
5	Rise time	0.025ns
6	Fall time	0.025ns

Table 2: Compare of previous work and proposed design of 18-TSPCFF

Sr No.	Parameters	Previous Work	Proposed Work
1	Area	599.20 μm^2	374.0μm^2
2	Power	10 µW	7.749µW
3	Delay	13.28ns	7ns
4	Power Delay Product (PDP)	1328	542.43
5	Rise time	0.028ns	0.025ns
6	Fall time	0.028ns	0.025ns
7	Software	SPICE	DSCH and Microwind

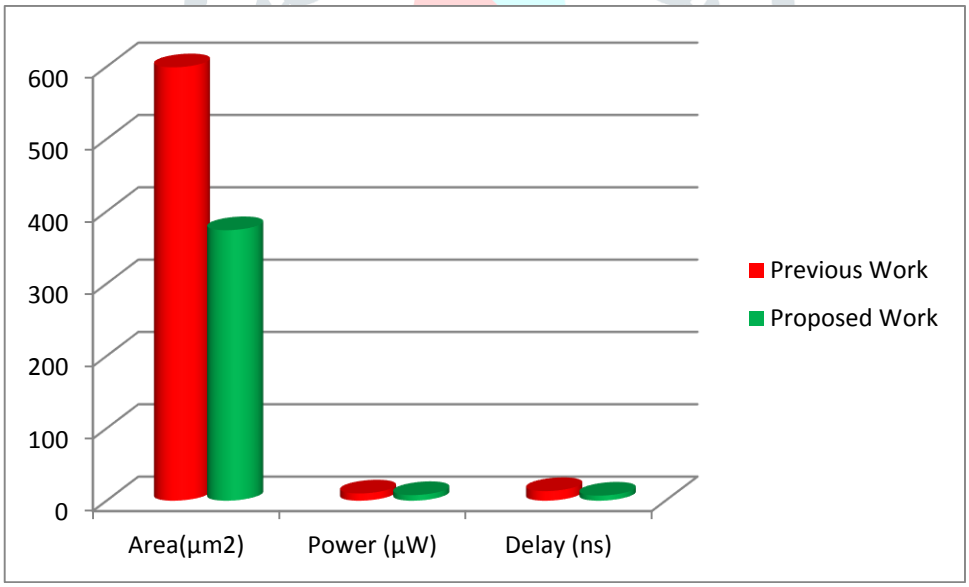

Figure 9: Comparison of previous design with proposed design

Therefore to see all simulated result and parameter values, it is observed that proposed design performance is better than previous designs.

V. CONCLUSION

This paper proposed 18- Transistor True Single Phase Clock, a fully static and contention free TSPC FF with the lowest reported number of transistors(18), demonstrating a significant cell area reduction with respect to the conventional TGFF. Although a performance penalty is observed, thanks to the low-power characteristic of the proposed design, 18TSPC achieves more. A brief summary of the proposed 18TSPC and comparison with prior works is presented. Therefore proposed 18TSPC has better power, area and time than existing design.

REFERENCE

1. Y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell and T. J. Kazmierski, "Ultra-Low Power 18-Transistor Fully Static Contention-Free Single-Phase Clocked Flip-Flop in 65-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 550-559, Feb. 2019.

2. W. Wang, S. Jia, Z. Wang, T. Pan and Y. Wang, "Low Voltage Dual-Modulus Frequency Divider Based on Extended True Single-Phase Clock Logic," *2018 IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC)*, Shenzhen, 2018, pp. 1-2.
3. J. Shaikh and H. Rahaman, "High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop," *2018 International Symposium on Devices, Circuits and Systems (ISDCS)*, Howrah, 2018, pp. 1-4.
4. P. Xu, C. Gimeno and D. Bol, "Optimizing TSPC frequency dividers for always-on low-frequency applications in 28nm FDSOI CMOS," *2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Burlingame, CA, 2017, pp. 1-2.
5. F. Stas and D. Bol, "A 0.4V 0.08fJ/cycle retentive True-Single-Phase-Clock 18T Flip-Flop in 28nm FDSOI CMOS," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, 2017, pp. 1-4.
6. J. Lin, M. Sheu, Y. Hwang, C. Wong and M. Tsai, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 11, pp. 3033-3044, Nov. 2017.
7. H. Ashwini, S. Rohith and K. A. Sunitha, "Implementation of high speed and low power 5T-TSPC D flip-flop and its application," *2016 International Conference on Communication and Signal Processing (ICCSP)*, Melmaruvathur, 2016, pp. 0275-0279.
8. S. Jia, Z. Wang, Z. Li and Y. Wang, "A novel low-power and high-speed dual-modulus prescaler based on extended true single-phase clock logic," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, QC, 2016, pp. 2751-2754.
9. S. S. Varma, A. Sharma and B. Anand, "An efficient methodology to characterize the TSPC flip flop setup time for static timing analysis," *2016 13th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Lisbon, 2016, pp. 1-4.
10. S. Jia, S. Yan, Y. Wang and G. Zhang, "Design of low-power high-speed divide-by-2/3 prescalers with improved true single-phase clock scheme," *2014 Asia-Pacific Microwave Conference*, Sendai, Japan, 2014, pp. 241-243.
11. X. Tang, J. Zhang, P. Gaillardon and G. De Micheli, "TSPC Flip-Flop circuit design with three-independent-gate silicon nanowire FETs," *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne VIC, 2014, pp. 1660-1663.
12. M. Jung, J. Fuhrmann, A. Ferizi, G. Fischer, R. Weigel and T. Ussmueller, "A 10 GHz low-power multi-modulus frequency divider using Extended True Single-Phase Clock (E-TSPC) Logic," *2012 7th European Microwave Integrated Circuit Conference*, Amsterdam, 2012, pp. 508-511.
13. F. Stas and D. Bol, "A 0.4-V 0.66-fJ/Cycle Retentive True-Single-Phase-Clock 18T Flip-Flop in 28-nm Fully-Depleted SOI CMOS," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 3, pp. 935-945, March 2018.
14. J. Lin, M. Sheu, Y. Hwang, C. Wong and M. Tsai, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 11, pp. 3033-3044, Nov. 2017.