A Switched-Capacitor DC-DC Converter Cascaded with H-bridge Inverter System

Priyanka Maheshkar
Post Graduate Student, Department of Electrical Engineering, Government College of Engineering, Amravati, PIN: 444 604.

P. P. Gajbhiye
Assistant Professor, Department of Electrical Engineering, Government College of Engineering, Amravati, PIN: 444 604.

Abstract— This paper proposes a multilevel inverter using switched-capacitor multilevel inverter system. The structure consisting switched-capacitor DC-DC converter gives asymmetric DC voltage sources as input and H-bridge inverter produces different voltage level at the output. The common feature in all SCMLI topologies is the back-end H-bridge inverter. Therefore, the key is to design the front-end SC DC-DC converter that can produce multiple levels. This topology is beneficial where asymmetric DC voltage sources are available e.g. in case of renewable energy farms based AC micro-grids and modern electric vehicles.

Keywords--H-bridge, HFAC power distribution system, switched-capacitor multilevel inverter, high frequency DC/AC Inverter.

I. INTRODUCTION

Now a days High Frequency AC power distribution system (HFAC PDS) is very much popular. HFAC PDS was first discovered by NASA for its early development of space power distribution. NASA shows fewer power-conversion stages and lower number of component counts using this application. In HFAC PDS mostly a resonant inverter, a high-voltage low-current ac bus and a number of HFAC voltage-regulation modules (VRM) has been used. The resonant inverter is used to generate the high-frequency sinusoidal waveform, differing from the traditional sinusoidal pulse width-modulated (PWM) inverters. Hence, the HFAC bus frequency is the switching frequency of the resonant inverters.

The early work on HFAC has gave many potential benefits like flexibility at load for different voltage levels, with the help of compact high frequency transformers electrical isolation is calculated. For elimination of dynamic response of the system and acoustic noise HFAC is also been used. There is one drawback of HFAC PDS system. There are multiple loads at HFAC bus which can be further distributed at their point of use. The HFAC PDS has several advantages over dc power sources. It can give more efficient performance, great reliability, better power distribution than dc, higher power density and gives potential for connector less power transfer.

And HFAC PDS includes a front-end HFAC source, a High Frequency distribution track and point-of-load converters.

There is also an additional advantage of High Frequency Alternating Current Power Distribution Systems (HFAC PDS) over conventional Direct Current (DC PDS) is that, in conventional DC PDS additional rectifiers and filter stage is required in input and output side of system, this can neglected by HFAC PDS [1]. After these significant advantages of the HFAC power distributions systems over the dc power distribution systems, HFAC power distribution was later also proposed for high-power density telecommunication and computer applications. HFAC power distribution concept has also been applied in lighting, motor auxiliary loads in electric vehicle, and many other applications [5]. On the behalf of these information paper conclude that HFAC solves the problem of power delivery.

In this proposed topology HFAC PDS is made up of two stages

1) A high frequency (HF) multilevel inverter (MLI) or a resonant inverter in the source side and
2) ac/ac or ac/dc voltage-regulation modules in load side.

Whenever greater power capacity is required, multiple resonant inverters are connected in series or parallel to the inverter. The proposed topology of this paper is using switched-capacitor multilevel inverter to the input of the system and reduces extra dc sources.

Multilevel inverters is nothing but an power electronic device which able to provide high alternating voltage level as required using multiple DC sources as an input. So that, now it is in hug demand in industry and academia as one of the preferred choice of electronic power conversion for high-power applications.

For two level inverter is used for conversion of DC voltage to AC voltage. If we take V_{DC} as an input it will give $+V_{DC}/2$ at positive half and $-V_{DC}/2$ at negative half at output. In order to build an AC voltage, these voltages can be switched using PWM. But it creates high Harmonic Distortions. To avoid this drawback multilevel inverter concept established. It gives lower dv/dt and Harmonic Distortions. This system is already taken as compressors, extruders, pumps, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, high-voltage direct-current (HVDC) transmission, hydro-pumped storage, wind energy conversion and railway traction.

II. PROPOSED TOPOLOGY AND OPERATING PRINCIPLE OF SCMLI

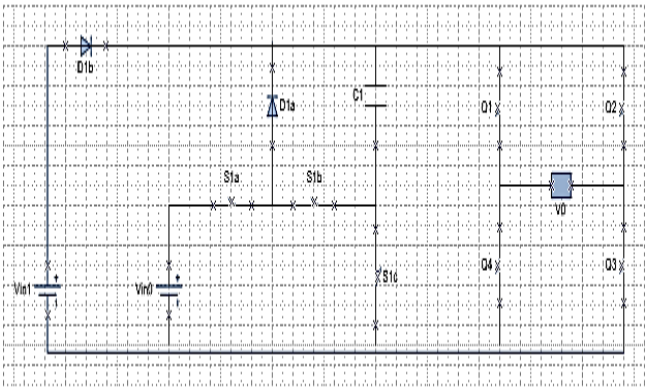


Fig. 1: Proposed model of SCMLI topology

A Switched-Capacitor Multilevel Inverter (SCMLI) topology is used as a source in this paper. This can help in increasing efficiency, power factor and energy density [3]. The SCMLI has tendency to give multiple output voltage level from single input voltage source. In today's world industries highly demanding Multilevel Inverters (MLI) which can generate output voltage waveform which can later be easily filtered to obtain fundamental amplitude with extremely low total harmonic distortion (THD) content [4]. This paper, focuses on novel SCMLI topologies with multiple input voltage sources which sharing a common ground is useful in areas like micro grids and electric vehicle networks where asymmetric input sources are available in high frequency AC power distribution [1].

$$n_l = 2^{i+1} - 1 \quad (1)$$
$$n = i - 1 \quad (2)$$
$$n_T = n_{gd} = 3i + 1 \quad (3)$$
$$n_D = 2(i - 1) \quad (4)$$

Where,
$'n_T'$ = the number of transistors,
$'n_D'$ = the number of diodes,
$'i'$ = the number of individual input voltage sources employed in the MLI,
$'n_l'$ = the number of output levels.

In a Proposed methodology, Switched–Capacitor based multilevel inverter is used as front end and H-bridge inverter at the back end. In that, DC-DC converter is used at primary side which is nothing but the multiple unsymmetrical DC sources of low voltage level that can give multiple Six levels voltage outputs without using inverter and the H-bridge inverter produce zero voltage level and bipolar level at output. The number of output levels is directly proportional to number of input voltage sources, Switched-Capacitor (SC) and power switches of SC DC-DC converter. There are three transistor switches has used which are S_{1a}, S_{1b}, and S_{1c} which can used to switch capacitor C_1 in series and parallel in order to generate output voltage levels, four H-bridge transistors present i.e Q_1, Q_2, Q_3, Q_4 gives positive and negative half cycles, two diodes D_{1a}, D_{1b} is present.

The circuit operation consist of four different mode

1. $V_0 = \pm V_{IN1}$ state

Transistor S_{1c} and input voltage V_{IN1} is turned ON. Voltage source V_{IN1} alone supplies power to the load.

2. $V_0 = \pm V_{IN0}$ state

Transistor S_{1a} is turned ON. Proposed inverter value is $V_{IN0} > V_{IN1}$. Voltage source V_{IN0} supplies power to the load.

3. $V_0 = \pm(V_{IN0} + V_{IN1})$ state

Transistors S_{1a} and S_{1b} is turned ON. Voltage source $V_{IN0} + V_{IN1}$ supplies power to the load.

4. $V_0 = 0$V state

Transistor Q_1 is turned ON for positive half cycle. Similarly, transistor Q_4 is turned ON negative half cycle. The switches in the front-end converter remain in previous states.

The operational waveforms shown in Fig.2 working on specific values of SCMLI components which are V_{IN0} = 48V and V_{IN1} = 24, the output voltage waveform would have 0, ±24V, ±48V and ±72V, capacitor C_1 voltage = 24 V would always constant.

TABLE I: Switching logic for proposed SCMLI topology

SC switches (ON condition)			H-bridge switches (ON condition)				Output Voltage
S_{1a}	S_{1b}	S_{1c}	Q_1	Q_2	Q_3	Q_4	V_0
0	0	1	1	0	1	1	V_{IN1}
1	0	0	1	0	1	1	V_{IN0}
1	1	0	1	0	1	1	$V_{IN0}+V_{IN1}$
0	0	1	1	0	0	1	0
0	0	1	0	1	0	0	- V_{IN1}
1	0	0	0	1	0	0	- V_{IN0}
1	1	0	0	1	0	0	$-(V_{IN0}+V_{IN1})$
0	0	1	0	0	0	0	0

III. MODULATION OF SCMLI

Selective Harmonic Elimination (SHE) is a specific technique is used in this topology for elimination of specific harmonics present in output and help to give smoother output waveform. For getting waveform at fundamental and harmonic frequency Fourier analysis is done by considering an 'm' level staircase waveform.

a_0 and a_n= the coefficients equal to zero, applying for half and quarter wave symmetry.

z = (m−1)/2 capacitors value and

θ_1 to θ_z = the conducting angles

The waveform can be mathematically represented as:

$$v(\omega t) = \sum_{x=1,3,5} \left(\frac{8}{T} \int_0^{\frac{T}{4}} f(wt) \sin(xwt)\, dwt \right) \sin(xwt)$$

$$= \sum_{x=1,3,5} \frac{4V_{IN}}{x\pi} \{cosx\theta_1 + \cdots + cosx\theta_z\} \sin(xwt) \qquad (5)$$

The fundamental voltage in terms of switching angles is given by:

$$v_1(\omega t) = \frac{4V_{in}}{\pi} \{cosx\theta_1 + \cdots cosx\theta_z\} \sin(xwt) \qquad (6)$$

V_{1p} = maximum obtainable fundamental amplitude

The diode rectifies the incoming signal and it allows only one-half of the signal waveform pass through it. Here all the switching angles $(v_1(\omega t))$ must be equal to zero. Then V_{1p} is calculated by:

$$V_{1p} = \frac{4z}{\pi} V_{IN} \qquad (7)$$

Modulation index is nothing but the ratio of fundamental component amplitude of the inverter output voltage to the maximum value of fundamental voltage. SHE is calculating the angles for eliminating special harmonics.

$$M_I = \frac{V_1}{V_{1P}} = \frac{\pi V_1}{4zV_{IN1}} \qquad (8)$$

M_I = Modulation index

V_1 = desired fundamental voltage

The 3rd, 9th and 11th harmonic are very small in magnitude. For elimination of 5th and 7th harmonic equations are given below:

$$\begin{cases} \cos\theta_1 + \cos\theta_2 + \cos\theta_3 = 3M_I \\ \cos5\theta_1 + \cos5\theta_2 + \cos5\theta_3 = 0 \\ \cos5\theta_1 + \cos5\theta_2 + \cos5\theta_3 = 0 \end{cases} \qquad (9)$$

Where,

$0 < \theta_1 < \theta_2 < \theta_3 < \frac{\pi}{2}$

The total harmonic distortion (THD) is the harmonic distortions present in system and it is defined as the ratio of sum of all harmonic component power to the fundamental frequency power. THD be given by:

$$T.H.D = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1} = \sqrt{\sum_{n=3,9,11,13..}^{\infty} \left(\frac{V_n}{V_{1rms}}\right)^2} \quad (10)$$

IV. CHARACTERISTIC EQUATION PERFORMANCE AND ANALYSIS OF CIRCUIT

For the proposed SCMLI with i-input voltage sources, n_l voltage levels can be produced. Under ideal case, each staircase voltage level (V_A, V_B,..) and capacitor voltage (V_{C_i}) can be expressed using the following set of generalized equations:

$$\begin{cases} V_A = V_{IN_i} \\ V_B = V_{IN_{i-1}} \\ V_C = V_{IN_i} + V_{IN_{i-1}} \\ V_D = V_{IN_{i-2}} \\ V_E = V_{IN_{i-2}} + V_{IN_i} \\ V_F = V_{IN_{i-2}} + V_{IN_{i-1}} \\ \cdots \\ \cdots \\ \cdots \\ V_U = V_{IN_i} + V_{IN_i} + \cdots + V_{IN_0} \\ V_{C_i} = V_{IN_i} \end{cases} \quad (11)$$

General expression for RMS value of the m-level staircase waveform is given by:

$$V_{0_{RMS}} = \sqrt{\frac{2}{\pi}(V_A^2\delta_A + V_B^2\delta_B + \cdots + V_N^2\delta_N)} \quad (12)$$

When the magnitude of input voltage sources are integral multiples of magnitude of the least value of input voltage source then the output waveform is symmetric in nature. For a seven level output if V_{IN0} = kV_{IN1}, $V_{0_{RMS}}$ is given as:

$$V_{0_{RMS}} = V_{IN_1}\sqrt{\frac{2}{\pi}(\delta_A + k^2\delta_B + (k+1)^2\delta_N)} \quad (13)$$

k = any constant (greater than 1)

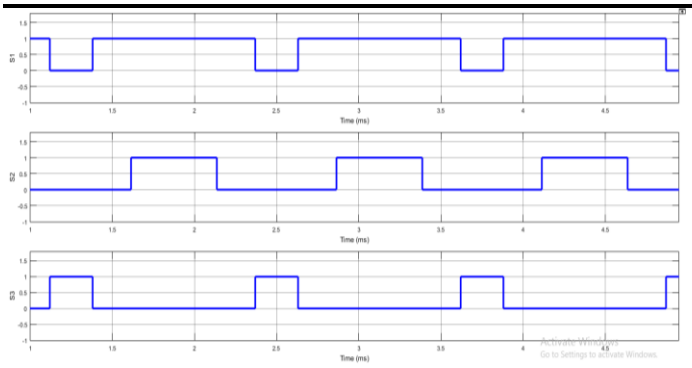
Considering non-idealitiesR_{in},V_F, $R_{ds_{ON}}$ and ESR of the SC, each voltage step and the V_{C1} of the seven level inverter can be represented as –

$$\begin{cases} V_A = V_{IN_1} - V_F - I_0(2R_{ds_{ON}} + R_{in}) \\ V_B = kV_{IN_1} - V_F - I_0(3R_{ds_{ON}} + R_{in}) \\ V_C = kV_{IN_1} + V_{c1} - I_0(4R_{ds_{ON}} + R_{in} + ESR) \\ V_{C1} = V_{IN_1} - V_F - I_{C1}(R_{ds_{ON}} + R_{in} + ESR) \end{cases} \quad (14)$$

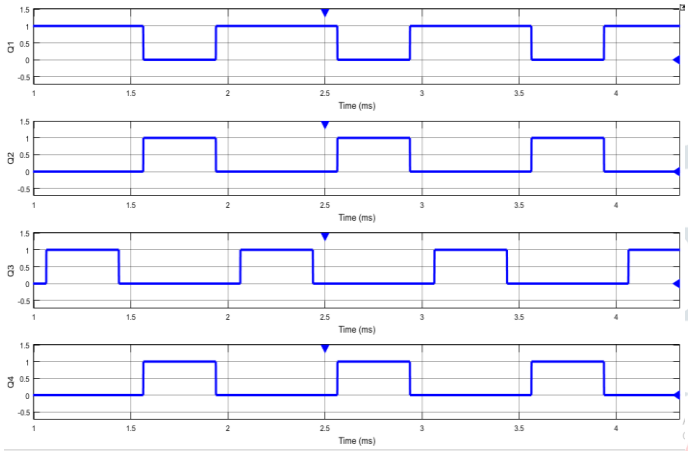
I_0 = average output current of the front-end converter

I_{C1} = average capacitor charging current.

$R_{ds_{ON}}$, diodes with V_F and ESR values must be taken as low. With the help of these, there are efficiency of system get improved and available voltage sources also perfectly used.



(a)



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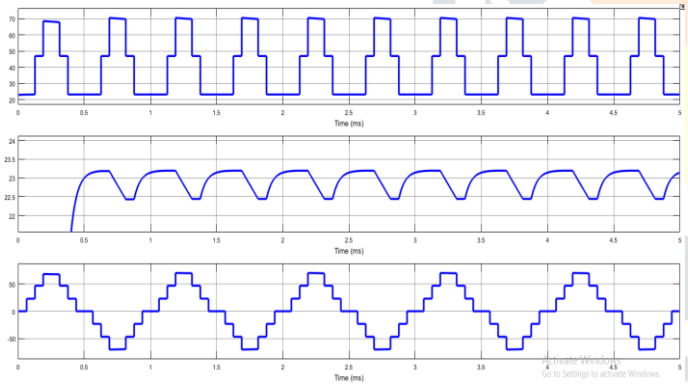

(c)

Fig 2: Simulation Waveform of SC output voltage and current.

V. SIMULATION AND EXPERIMENTAL RESULTS

As the number of output level increases, the diodes connected in MLI not proceeding to implement that level. But in case of SCMLI such problem not arises. Hence SCMLI topology to generate higher number of output levels compared to the traditional MLI. Voltage at the capacitor terminals are measured different than required voltage unbalance problem may arise. These problems are overcome in the proposed SCMLI by using $(2^{(n+2)}-1)$ output levels [1]. Below table shows SCMLI component values for simulation.

TABLE II: Proposed SCMLI values used for simulation

V_{IN0}	40V
V_{IN1}	20V
SC	470µF
R_{in}	0.1Ω
ESR	0.1Ω
V_F	0.42V
R_d	10mΩ
$R_{ds_{ON}}$	9mΩ
θ_1	15.6◦
θ_2	18.7◦
θ_3	52.4◦

In reference [4], a Switched-Capacitor Inverter Using Series/Parallel Conversion with Inductive Load is performed. There are two SCs are required for getting a seven output voltage level and it uses two SC voltage to output out of seven-level. According to that, system shows higher voltage rating factor and efficiency is measured poor. This is one of the reasons for modification in system required. In proposed system these problem is overcome. Here only one Switched-Capacitor is sufficient for enhancing seven output voltage level and it uses five SC voltages to output out of seven-level. Hence voltage ripple factor and smaller SCs helps to save cost and space [1].

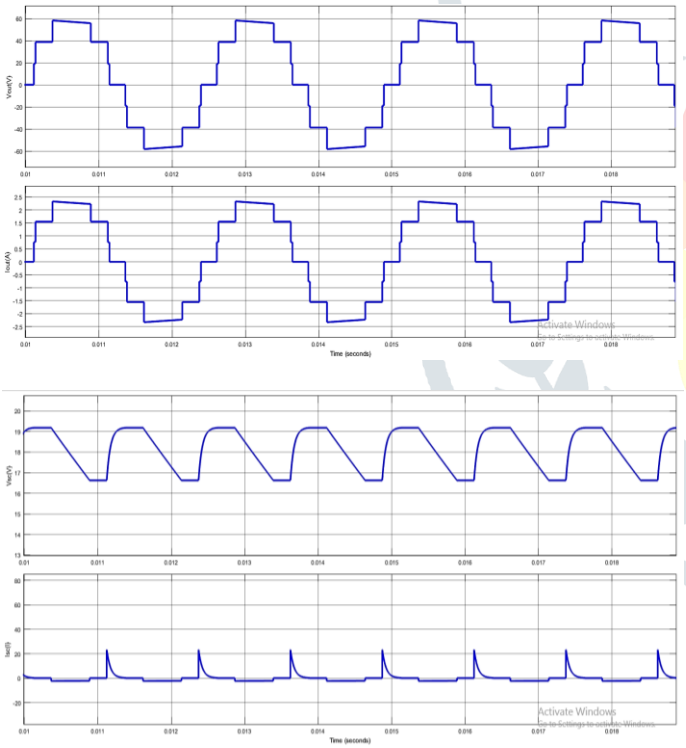

Fig. 3: Simulation waveforms of output voltage (V_{out}), current (I_{out}) and SC voltage (V_{dc}) and current (I_{dc}) at 400 Hz when resistive load is 25 Ω

VI. CONCLUSION

A simple topology of a SCMLI employing two asymmetric voltage sources is proposed. Also their working and different modes of operation are presented. This multilevel inverter is used in micro-grids where several numbers of asymmetric DC sources available. Benefit of MLI is asymmetric DC sources connected as inputs for a single inverter works as equal to connecting several inverters in parallel.
The proposed topology obtains higher number of voltage levels compared to several existing topologies performed before. The developed model is simulated in MATLAB/Simulink Library and results are shown in paper. This topology can be used for any number of levels.

REFERENCES

1) S. Raghu Raman, Student Member, IEEE, K.W.E. Cheng, Senior Member, IEEE, and Ye Yuanmao, Member, IEEE, "Multi-Input Switched-Capacitor Multilevel Inverter for High-Frequency AC Power Distribution," IEEE Transactions on Power Electronics, 2017.

2) S. Raghu Raman et al., "Switched-Capacitor Multilevel Inverters for High Frequency AC Microgrids", 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017.

3) S. Raghu Raman et al., "A Seven Level Switched Capacitor Multilevel Inverter with Asymmetric Input Sources for Microgrids", The 20th International Conference on Electrical Machines and Systems (ICEMS), Sydney, NSW, Australia, Aug 2017.

4) Y. Hinago and H. Koizumi, "A Switched-Capacitor Inverter Using Series/Parallel Conversion With Inductive Load," in IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 878-887, Feb. 2012.

5) P. Jain, M. Pahlevaninezhad, S. Pan, and J. Drobnik,"A review of high frequency power distribution systems: For space, telecommunication, and computer applications," IEEE Trans. Power Electron., vol. 29, no. 8, pp. 3852–3863, Aug. 2014.