Design & Optimization of FinFET based Schmitt Trigger using Dual Stack Techniques

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***Abstract*—**This paper deals with proposal of a new dual stack techniques for reducing leakage current. The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density .Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Today leakage power has become an increasingly important issue in processor hardware and software design. It can be used in various applications like digital VLSI clocking system, buffers, registers, microprocessors etc. The leakage power increases as technology is scaled down. In this paper, we propose a new dual stack approach for reducing both leakage and dynamic powers. Moreover, the novel dual stack approach shows the least speed power product when compared to the existing methods. All well known approach is "Sleep" in this method we reduce leakage power. The proposed Dual Stack approach we reduce more power leakage. Dual Stack approach uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the Dual Stack portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit. The dual stack approach shows the least speed power product among all methods. The Dual Stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product.

Keywords—Leakage current, Dual Stack, Sleep transistor, Low power.

I. INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit; Static power: Includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling. Among these, sub threshold leakage is the most prominent one. Dynamic power: Includes charging and discharging power and short circuit power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower. So it is becoming more and more important to reduce leakage power as well as dynamic power[1]. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dynamic power. We summarized and compared the previous techniques with our new approach. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower. So it is becoming more and more important to reduce leakage power as well as dynamic power. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dynamic power. We Summarized and compared the previous techniques with our new approach.

AIM OF THE PAPER

Today leakage power has become an increasingly important issue in processor hardware and software design. The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. In this paper, we shall describe a number of critical Considerations in the sleep transistor design and implementation including header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dynamic power. We Summarized and compared the previous techniques with our new approach. We provide novel circuit structure named "Dual stack" as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product.

A .SIGNIFICANCE OF WORK

There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dyamic power. The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the

geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Today leakage power has become an increasingly important issue in processor hardware and software design. In 45 nm and below technologies, leakage accounts for 30-40% of processor power.

II. CIRCUIT DESCRIPTION OF FinFET BASED SCHMITT TRIGGER

Schmitt Trigger [2] is a comparator that compares the input signal with some certain chosen threshold value. In this circuit, when the input goes higher than the certain chosen higher threshold value, the output goes high. Similarly, when the input goes lower than lower chosen threshold value, the output goes low. But the important thing to be noticed in this design is that when the inpu two chosen threshold values, the o value because of this dual action widely used in memories. The system has becoming a limiting Leakage power consumption technology is scaled down. FinFET based Schmitt trigger basically the cascade of two FinFET output of first inverter is the input inverter which produces some output is again positive feedback section of the design. FinFET based Schmitt Trigger Leakage power dissipation in any volt be alleviated when the standby turnoff . For this reason sub-circuit to connect by one pmos and one nm form virtual power supply and the above scheme is for theoretical As nmos transistor offers lower on pmos transistor practically single nm used.

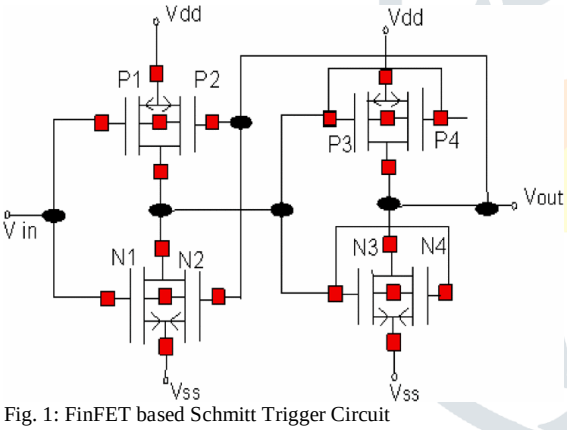

Fig. 1: FinFET based Schmitt Trigger Circuit

III .TECHNIQUES FOR LEAKAGE POWER REDUCTION

Techniques for leakage power reduction can be grouped into two categories: state-preserving techniques where circuit state is retained and stated estructive techniques where the current Boolean output value of the circuit might be lost. A state preserving technique has an advantage over a state destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to some how regenerate state. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power. They are:

1. Sleep Transistor Method
2. Dual Sleep Method
3. Dual Stack Approach Method

A- SLEEP TRANSISTOR METHOD

In the sleep approach, a "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and a "sleep" NMOS transistor is placed between the pull-down network and Ground. These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage.

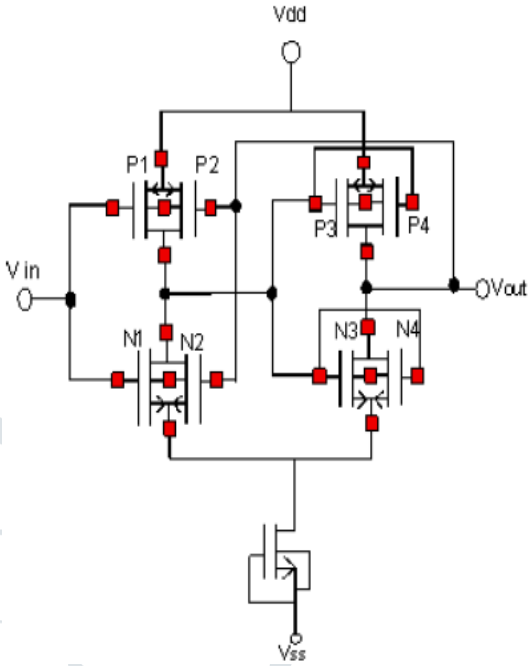

Fig. 2: FinFET based Schmitt Trigger using sleep transistor approach

B. Dual Sleep Method

Another technique called Dual sleep approach uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry [3], less number of transistors is needed to apply a certain logic circuit. The circuit is connected as shown in the figure below.

C- DUAL STACK APPROACH METHOD

We propose a novel dual stack technique that reduces not only leakage power but also dynamic power. We Summarized and compared the previous techniques with our new approach. We provide novel circuit structure named “Dual stack” as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. In this section, the structure and operation of our novel low-leakage-power design is described. It is also compared with well-known previous approaches, i.e., the sleepy stack, dual sleep and sleep transistor method. Here we use 2 PMOS in the pull-down network and 2 NMOS in the pull up network [4]. The transistors are held in reverse body bias. As a result their threshold is high. High threshold voltage causes low leakage current and hence low leakage power.

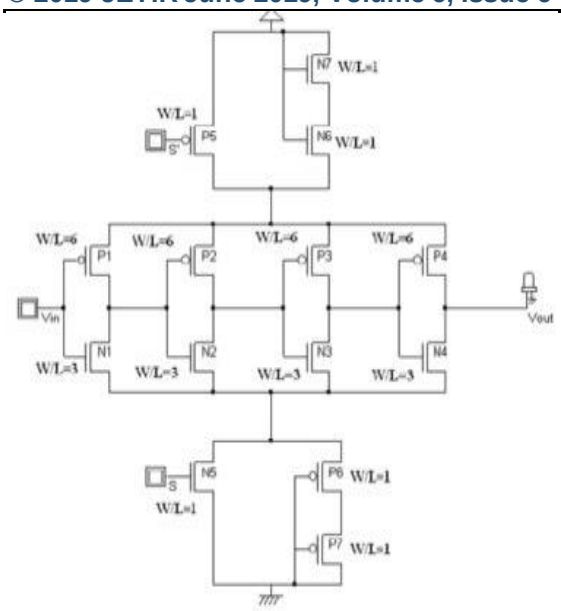

Fig 3: dual stack technique

IV SIMULATION AND RESULTS:

A-Simulation of FinFET based Schmitt Trigger at 45nm technology.

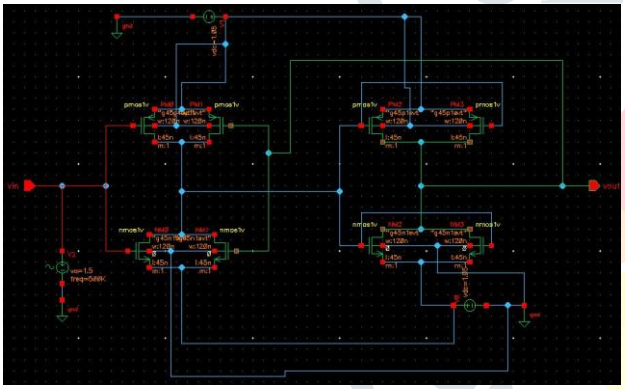

Fig 4: Circuit diagram of Finfet based schmitt trigger

Output of FinFET based Schmitt Trigger circuit at 45nm technology is shown in fig 5.

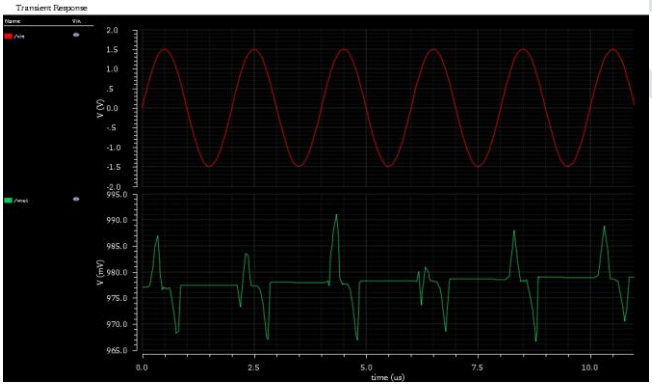

Fig 5: Output of Finfet based schmitt trigger

B- Simulation of FinFET based Schmitt Trigger using Dual Sleep technique at 45nm technology.

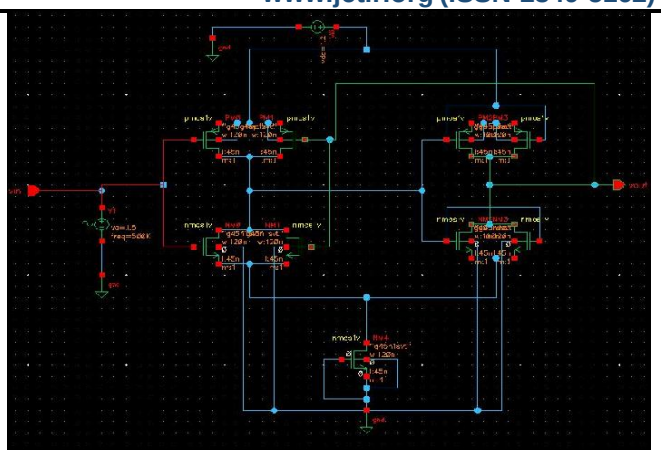

Fig 6: Circuit diagram of Finfet based schmitt trigger using Dual Sleep Technique

Outpur of FinFET based Schmitt Trigger using Dual Sleep Technique at 45nm Technology.

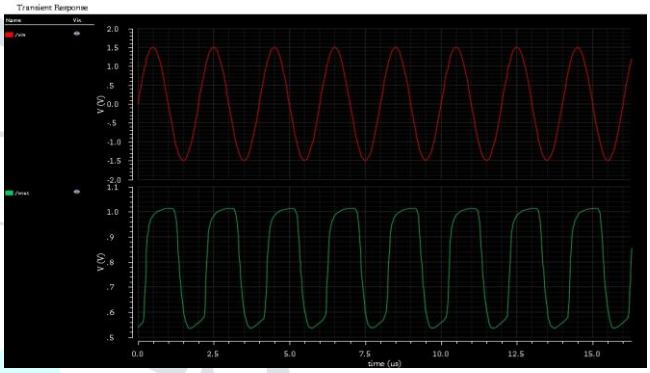

Fig 7: Output of Finfet based schmitt trigger using dual sleep technique

From Fig 5 and Fig 7 we can observe that the Schmitt trigger using dual sleep technique has smooth graph curves as compared to the graph of finfet based Schmitt trigger without using any modified techniques. This shows that adding a sleep transistor to the pull down network helps in providing a cleaner square wave on giving a sine wave input.

C-Simulation of FinFET based Schmitt Tigger using Dual Stack Technique at 45nm Technology

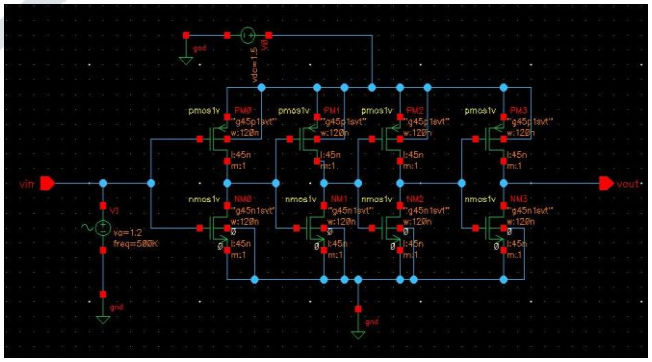

Fig 8: Circuit of Finfet based schmitt trigger using dual stack technique

Output of FinFET based Schmitt Trigger using Dual Stack Technique at 45nm Technology.

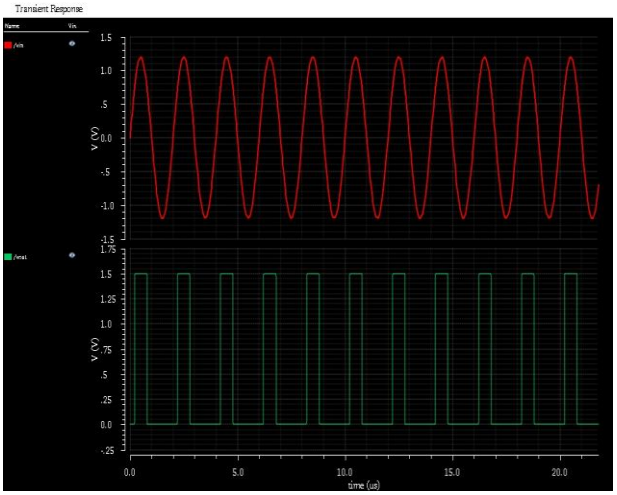

Fig 9: Output of Finfet based schmitt trigger using dual stack technique

COMPARISION TABLE

Table shows the comparison of sleep transistor method with dual stack approach method. I will reduce the leakage current by the help of dual stack method at 45nm cadence tools.

Factors	Sleep Transistor	Dual Stack
CMOS Technology	70nm	45nm
Power Consumed	6.669µW	4.280µW
Leakage Current	2.907pA	2.733pA

Table 1: Comparison between Sleep transistor and Dual Stack Technique

CONCLUSION

In nanometer scale CMOS technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. We provide novel circuit named "Dual Stack" as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistors technique, the dual stack technique retains the original state [5]. The dual stack technique shows the least speed power product among all methods. Therefore, the dual stack technique provides a new ways to designers who require ultra-low leakage power consumption with much less speed power product.

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