Design and Implementation of n-bit Linear Feedback Shift Register for SS-CDMA

[1]Prafful Lashkari, [2]Dr. D. K. Mishra, [3]Mr. Rajesh Khatri
[1]M.Tech Scholar, [2]Professor, [3]Associate Professor
[1]Department of Electronics and Instrumentation,
[1]SGSITS, Indore, India.

Abstract : This paper has examined the idea of PN sequence and design of linear feedback shift register as applicable to spread spectrum code division multiple access technique. Maximum length sequence arrangements were presented, and utilized as a prologue to some difficult strategies for PN code generation with the assistance of LFSR. In linear feedback shift register, the feedback is used to modification on every clock cycle. In this paper we have implemented n-bit LFSR and achieved maximum frequency upto 1300 MHz, which can be used in SS-CDMA. Different parameters are discussed and compared with few existing research papers. Overall parameters were obtained with the help of Xilinx 12.1i by using VHDL.

IndexTerms **- Shift Registers, LFSR, PN Sequence, CDMA, and VHDL**

I. INTRODUCTION

Considerable interest has developed during the past two decades in the binary feedback shift registers. These devices are capable of generating cyclic sequences possessing statistical properties which closely approximate those of binary random noise. Such, apparently random, but deterministic, sequences may be used, therefore, in place of this noise) and the results which are thus obtained are much more accurate than those obtained using binary noise. The ease and simplicity in generating and processing the sequences are further responsible for this development.

The arena of mobile communication is presently developing at very uncommon rate. This development provoked to a limited extent by the increasing rate, broadband communication, has prompted the requirements for high determination, broadband mobile measurement hardware. The wireless communication structure is one of most significant method in the entire existence of media transmission which has enhanced human development and mankind by uniting business and network. A pseudo noise sequence (PN sequence) is assigned to each user in the spread spectrum code division multiple access schemes for the purpose of grouping and dispreading. In this way PN sequence is viewed as the core of CDMA/SS-CDMA systems. The maximal length pseudo noise sequence is best depicted sequence whose length is same with its period. Linear feedback shift register i.e. LFSR is used to generate multiple PN sequence. In this shift register feedback is provided by essential feedback taps. By VLSI technology, the implementation of LFSR circuit can be used in less delayed communication system designs.

The objective of this work is to evaluation of n-bit Linear Feedback Shift Register using memory element. Also designing the LFSR for the application of CDMA, where PN sequence is multiply with input message to add the security while transmitting the codeword into wide range of frequency. Bascially CDMA works in the frequency range of 900 MHz to 1.9 GHz so the objective of this thesis is to design and implement LFSR for this frequency range..

II. LITERATURE REVIEW

Wherever **Mishra Shivshankar et al. [1],** in this paper author suggested and implemented the configurable linear feedback shift register. They assess the results in terms of logic, memory and speed requirements using Xilinx ISE 9.2i tool. Their targeted device for implementation is Vertex-4 FPGA board. The implemented 8 bit and 16 bit CLFSR completes the output sequence cycle in 51000 ns and 13107000 ns. Author also suggested various applications of CLFSR like PN sequence generator, Gold code generator and CRC generator.

R Saraswathi et al. [2], in this paper author described the design and implementation of linear feedback shift register (LFSR) for low power test pattern generator. They modified the existing design of linear feedback shift register by utilizing transition controllers. Their simulation and results are achieved through Altera Quartus 16.0. They compared their results for power consumption and Number of test pattern generated.

Tejas Thubrikar et al. [3], in this research manuscript author designed and implemented 32 bit low power test pattern generator using linear feedback shift register. Their whole design is implemented in Xilinx ISE 13.1i using VHDL language. By using extra combinational circuit in the existing design of LSFR they achieved 50% reduction in power consumption. Also they attained less number of slice register used and less number of LUT's.

Roshni Jamgade et al. [4], in this paper the author suggested new method for designing of linear feedback shift register. They used vedic multiplication which is the oldest method for multiplication using vedic formulas. Author suggested the application of linear feedback shift register for generation of PN sequence which is used in CDMA for multiplication with original sequence of message to add the security in transmission over a wide frequency. Area and delay analysis is done in this existing work.

Debarshi Datta et al. [5], this paper suggested the design and implementation of multibit linear feedback shift register to generate PN sequence codes which are very useful in CDMA. They designed the circuit using pseudo random number generator (PRNG) in HDL language. Their targeted device for implementation is Vertex-4 FPGA board for implementing 8 bit, 16 bit and

32 bit LFSR. They compared the results for various parameters like number of slice registers, occupied slices, and number of input output blocks, delay and power consumed.

Table 1: Comparison of various parameters of some research papers

S.No	Name of the Author	Year	No of Bits	Parameter	FPGA Used	Tool Used
1	Mishra Shivshankar	2016	8/16	Timing	Vertex 4	Xilinx
2	R. Saraswathi	2017	8	Power		Altera Quartis
3	Tejas Thubrikar	2017	8	Power		Xilinx
4	Roshni Jamgade	2015	8	Power	Virtex 7	Xilinx
5	Debarshi Dutta	2017	8/16	Delay	Spartan 6	Xilinx
6	**Proposed**	**2019**	**8, 16, 32 and 64**	**Power/Delay/Frequency**	**Artix 7**	Xilinx

III. METHODOLOGY

There are many applications of linear feedback shift registers, and it is commonly used in mobile communications where pseudo random sequence is required. These are the basic blocks of many circuits like PN sequence generator, gold code producer which is used in spread spectrum code division multiple access techniques. Linear feedback shift registers are extensively used for binary counters to generate random number sequences. Maximum time the generated sequence is pseudorandom in nature. These patterns may repeat over period, as longer the shift registers. This repetition is depends on the number of taps present in the registers. For large pattern generation, the size of hardware may be increased. Conservatively, for the older architectures of FPGA, flip flops were used. LFSR sequences are generated through $2^N - 1$ state, where N is the number of flip-flops/taps in the LFSR. After every edge of clock, the data of flip flop is shifted right. The feedback path is provided from previous register to the left most register through an XOR or XNOR gate. Value of 0's is illegal for XOR feedback path similarly value of 1's is illegal for XNOR feedback path. These illegal states may cause the shift register to present in its present state [13].

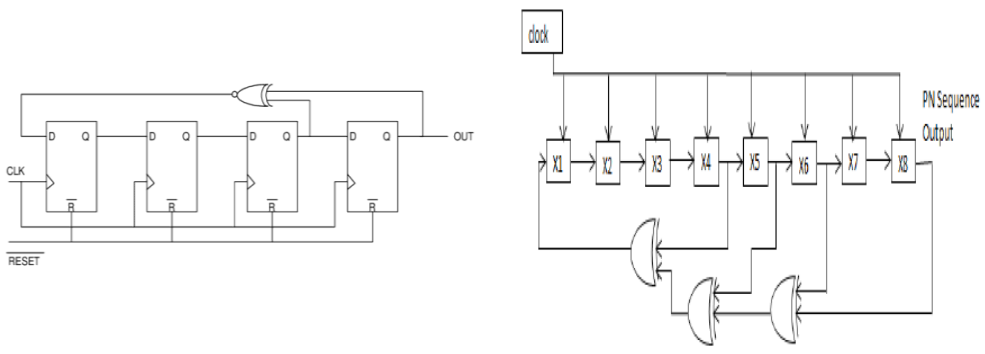
A 4-bit LFSR sequences generated through $(2^4 - 1)$ is having 15 states (the state 1111 is in the illegal state) from the feedback taps 4 and 3. At the same time, a 4 bit binary counter may generate the sequence by 2^4 i.e. 16 states without any illegal stages. Still linear feedback shift register are faster than normal counter because they don't have carry signal. Linear feedback shift register are the substitute of normal binary counters in perilous applications where the counted sequence is not that much important. Linear feedback shift register are also used as pseudo random sequence generators. These are the basic blocks of many circuits like PN sequence generator, gold code producer which is used in spread spectrum code division multiple access techniques. The tap sequence is responsible to affect the bits positions of next bits.

The n bit LFSR whose maximum feedback polynomial is represented as follows:

Table 2: Generator polynomial for LFSR

Number of Bits	Generator Polynomial
4	x^4+x^3+1
8	$x^8+x^6+x^5+x^4+1$
16	$x^{16}+x^{15}+x^{13}+x^4+1$
32	$x^{32}+x^{22}+x^2+x+1$
64	$x^{64}+x^{63}+x^{61}+x^{60}+1$

The general block diagram for 4, 8, 16 and 32 bit is shown as below:



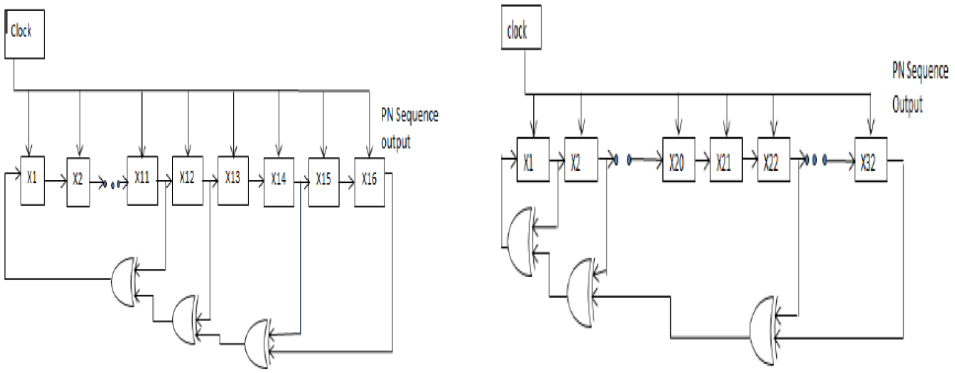


Figure 1: General block diagram of LFSR

IV. Simulation and Result

All the experiment analysis is done by 14.1i in Vertex device family. The significant benefit of this software is low-memory with high-speed analysis of any complex circuit. Simulation and synthesize of Linear Feedback Shift Register circuit may be improved by Xilinx design suit 14.1i Vertex device family series and device.

The RTL view, simulation waveform, schematic layout and device utilization summary for 4 bit, 8 bit, 16 bit, 32 bit and 64 bit is shown as below:

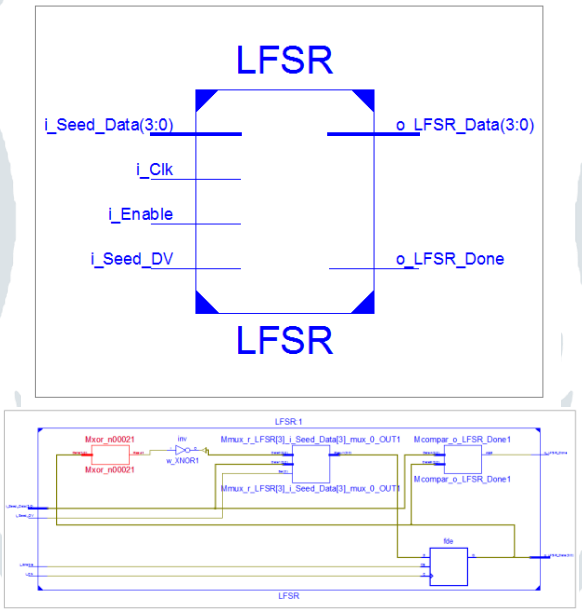


Figure 2: RTL view of 4 bit LFSR

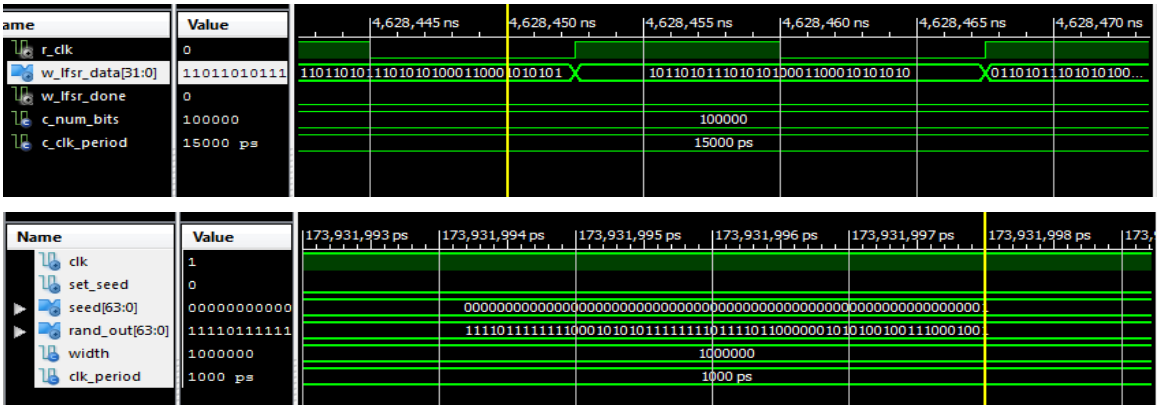


Figure 3: Simulated waveform for 4, 8, 16, 32 and 64 bit LFSR

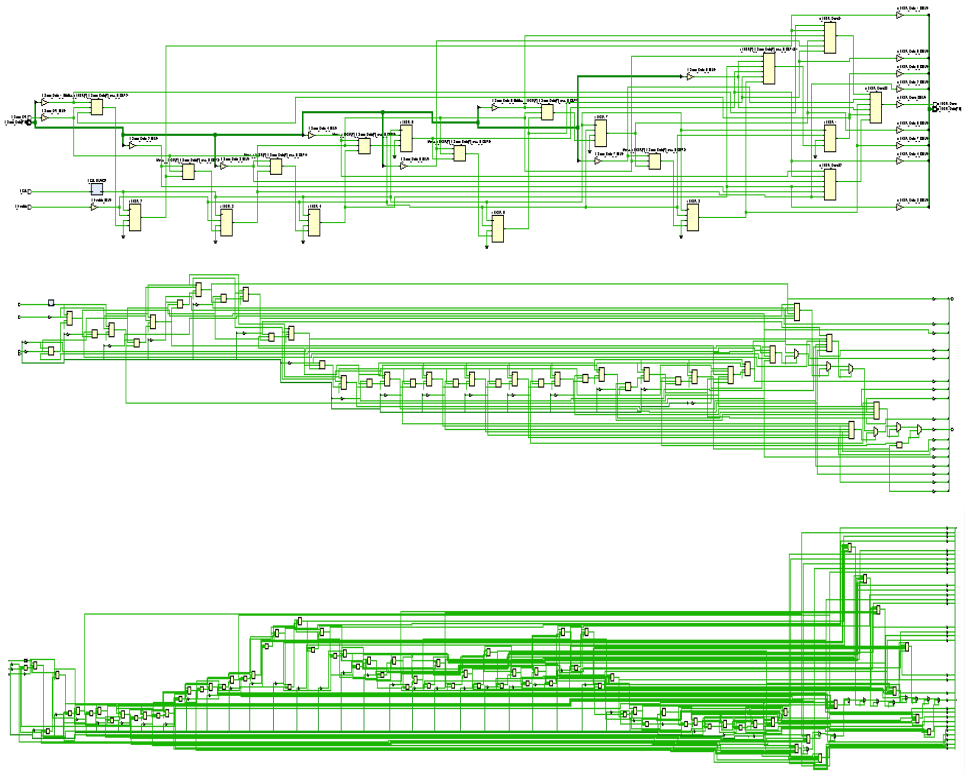


Figure 4: Schematic view of 8, 16 and 32 bit LFSR

Table 3: Device utilization summary

Synthesis Parameter	4 bit	8 bit	16 bit	32 bit	64 bit
Number Slice Registers	4	8	16	32	64
Number of Slice LUT	5	11	22	43	86
Number of occupied Slice	2	4	6	13	
Number of LUT Flip Flop pairs used	5	11	22	43	64
Number of IOBs	12	20	36	68	132
Max Freq (MHz)	1169.45	964.971	964.971	964.971	1296.849
Time Delay (ns)	0.855	1.036	1.036	1.036	0.771
Power (mW)	83	100	152	246	316

This paper basically deals with the design of linear feedback shift register using XOR gates. Above device utilization summary mentioned in table 3 shows the parameters used by the design. The following comparison table 4 shows the result of proposed LFSR with existing design:

Table 4: Comparison between different LFSR architectures

LFSR Architecture	Number of Bit	Number of Slices (Area)	Max. Frequency in MHz (Speed)	Time Delay in ns
Debarshi Dutta [5]	32	32	663.46	1.507
A. K. Panda [9]	32	18	137.532	7.27
S. Hathwalia [10]	32	32	476.872	2.09
K. C. Sekhar [11]	32	9	153.045	6.534
Proposed Design	**4**	**4**	**1169.454**	**0.855**
	8	**8**	**964.971**	**1.036**
	16	**16**	**964.971**	**1.036**
	32	**32**	**964.971**	**1.036**
	64	**64**	**1296.849**	**0.771**

V. CONCLUSION

To full fill the objective of this work, we have implemented linear feedback shift register using xor gates for 4 bit, 8 bit, 16 bit, 32 bit and 64 bit. Eventually, in this paper we have structured a LFSR which is used to generate PN sequence in various applications like Counters, CDMA, cryptography, test pattern generation and digital broadcasting etc. Our proposed design has very less output delay as compare to other designs. In the previous research work maximum frequency achieved is 664 MHz, and our proposed design will work up to 1300 MHz which can be used in CDMA.

REFERENCES

[1] Shivshankar Mishra, Ram Raksha Tripathi and Devendra Kr. Tripathi, "Implementation of Configurable Linear Feedback Shift Register in VHDL", International Conference on Emerging Trends in Electrical, Electronics and Sustainable Energy Systems (ICETEESES–16).

[1] R. Saraswathi, R.Manikandan, "Design of LFSR for low Power Test Pattern Generator", IEEE NetACT 2017

[2] Tejas Thubrikar et. al. "Design and Implementation of Low Power Test Pattern Generator Using Low Transitions LFSR" International Conference on Communication and Signal Processing, IEEE 2017

[3] Roshni Jamgade et. al. "Design and Implementation of PN Sequence Generator using Vedic Multiplication" International Conference on Advances in Computer Engineering and Applications (ICACEA) IEEE 2015

[4] Debarshi Dutta et. al. "Design and Implementation of Multibit LFSR on FPGA to Generate Pseudorandom Sequence Number" Devices for Integrated Circuit (DevIC), IEEE 2017

[5] Katti, R.S. Srinivasan, S.K., "Efficient hardware implementation of a new pseudo-random bit sequence generator," IEEE International Symposium on Circuits and Systems, 2009.

[6] K. Panda Amit, P. Rajput, B Shukla, "Design of Multi Bit LFSR PNRG and Performance comparison on FPGA using VHDL," International Journal of Advances in Engineering & Technology (IJAET), Mar 2012, Vol. 3, Issue 1, pp. 566-571.

[7] Sewak K, Rajput P, Panda Amit K, "FPGA Implementation of 16 bit BBS and LFSR PN Sequence Generator: A Comparative Study," In Proc. of the IEEE Student Conference on Electrical, Electronics and Computer Sciences 2012, 1-2 Mar 2012, NIT Bhopal, India.

[8] A. K. Panda, P. Rajput and B. Shukla, "FPGA Implementation of 8, 16 and 32 Bit LFSR with Maximum Length Feedback Polynomial using VHDL," IEEE Int. Conference on Communication Systems and Network Technologies, DOI 10.1109, 2012.

[9] S. Hathwalia and M. Yadav, "Design and Analysis of a 32 Bit Linear Feedback Shift Register Using VHDL", Int. Journal of Engineering Research and Applications, ISSN: 2248-9622, Vol. 4, Issue 6(Version 6), pp.99-102, June 2014.

[10] K. C. Sekhar and K. S. Raj, "An Efficient Pseudo Random Number Generator for Cryptographic Applications", Int. Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-4 Issue 1, October 2014