Design and Analysis of Low Power 9T SRAM cell using DG FINFET

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***Abstract*-This paper compares the performance of low power 9T SRAM cell, which includes performance parameters such as the Average write delay and writes power product delay, read the behavior of each SRAM cells are examined. Low power 9T SRAM cell at 90nm technology always consumes lowest Average power; improve read stability as compared to the conventional 6T SRAM cell. The aim of this paper is to reduce the low power, improve the reading behavior of the different SRAM cell structures using cadence tool at 90nm technology. DG FINFET techniques have been employed to reduce the power consumed by the SRAM cell. The results show that the DG FINFET based SRAM cell is the best performer in terms of power consumption. We investigate the use of Double Gate FINFET technology provides low leakage and high-performance operation by utilizing high speed and low thresh hold voltage transistors for the logic cell.**

***Keywords*- CMOS, 9T SRAM cell, Low Power, Average write delay, write power product delay, Cadence.**

I. INTRODUCTION

SRAM stands static random access memory. SRAM is volatile in nature; it means that it holds the data as long as the power supply is not cut off. Semiconductor memories, particularly SRAMs are widely used in electronic system [1-2-3]. Due to their higher speed, SRAM based Cache memories and System-on-chips are commonly used. Due to device scaling, there are several design challenges for nanometer SRAM design. Now we are working with very low threshold voltage and ultra-thin gate oxide due to which leakage energy consumption is getting increased. Besides this data stability during reading and write operation is also getting affected.

A significant percentage of the total area and power of many digital chips are due to SRAMs. For these chips, the SRAM leakage dominates the total chip leakage. Lowering the supply voltage (*VDD*) for SRAMs may reduce the leakage and switching power consumptions [4]. Static Random Access Memory is mainly used in various kinds of portable devices/systems. SRAM plays an important role in modern mobile phones, microprocessors, microcontrollers, and computers, etc. SRAM (Static RAM) and DRAM (Dynamic RAM) both hold the data but in different manners. DRAM requires the data to be refreshed periodically in order to retain the data. SRAM does not need to be refreshed as the transistors inside would continue to hold the data as long as the power supply is not cut off. The additional circuitry and timing are needed to refresh the DRAM periodically, which makes DRAM memory slower and less desirable than SRAM. One complication is the much higher power used by DRAM memory. With the advantages of high speed and ease of use, static random access memory (SRAM) has been widely used in system-on-chips (SoC). According to the International Technology Roadmap for Semiconductors (ITRS) forecast, memory is going to occupy 90% of the SoC area by 2013 [5].On the contemporary, the size of the transistor and SRAM bit cell can be reduced by the technology scaling technique, this has also made it even more challenging to maintain a sufficient cell stability margin while keeping the same scaling pace of access time and cell size as the mismatching of threshold voltage (Vt) between cross-coupled inverter pairs becomes larger and larger [6-7-8].

II. MEMORY SRAM CELL DESIGN

To overcome the problem of data storage destruction during the read operation, an 8T-cell implementation was used, for which separate read/write bit and word signal lines are used to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation [9]. A 9T SRAM cell is used for simultaneously reducing leakage power and enhancing data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The read static-noise-margin of the used circuit is thereby enhanced as compared to a conventional 6T SRAM cell. The idle 9T SRAM cells are placed into a super cut-off sleep mode, thereby reducing the leakage power consumption [10].

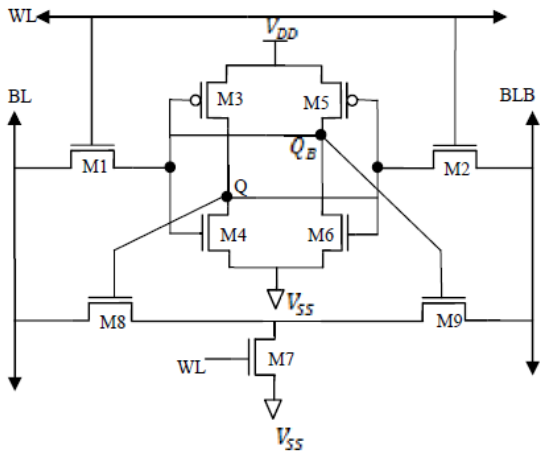


Fig.1 Schematic of 9T SRAM Cell

Figure 1 the schematic diagram of 9T SRAM Cell However in case of SRAMs, switching OFF the circuit would lose the data, and regrettably, it is a compulsion to keep the cell ON even if it is in idle state. This situation becomes a major challenge to reduce the leakage current as we have no option but to keep the circuit ON. To overcome the limitations mentioned above, the proposed SRAM cell has been equipped with a different read process which limits the time required to read the cell and helps in prohibiting the data corruption of cell by isolating it from the external read circuitry [11]. The cell has been designed to work with lower supply voltages, which helps in further reduction of the leakage power thus making the cell more efficient.

III. SIMULATION OF 9T SRAM CELL

9T SRAM cell uses two cross-coupled inverters and two access transistors as shown in Figure 2. These access transistors connect the cell to the outside world. The inverters are the storage element and reinforce the data bit within the cell as long as the power is supplied (VDD).

PM0, PM1 are PMOS transistors and NM0, NM1, NM2, NM3 are NMOS transistors. NM3 and NM4 are the access transistors (or pass transistors) connecting the cell to the Bit Lines are BL and BLB.

The two write access transistors (NM2 and NM3) are controlled by a write signal (WR). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (NM4 and NM5) and the read access transistor (NM6). The operations of NM4 and NM5 are controlled by the data stored in the cell (Q and QBAR). NM6 is controlled by a separate read signal (RD). Transient Response is shown in Fig.3

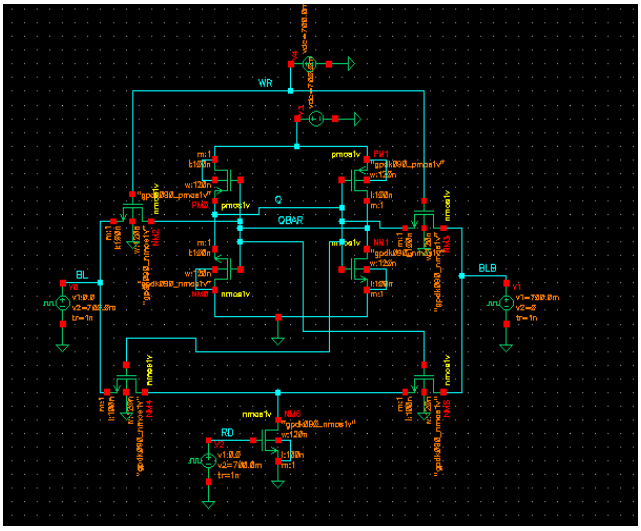


Fig.2 Schematic of 9T SRAM Cell

Transient response:

Here we discuss the transient response of the above-explained cells. This shows the write and holds modes of SRAM cell. When WL signal is high, the data on BL and BLB are written into the storage nodes Q and QB respectively. And when WL signal is low the Q and QB nodes store the recently written data before WL going to low as shown in fig. 3.

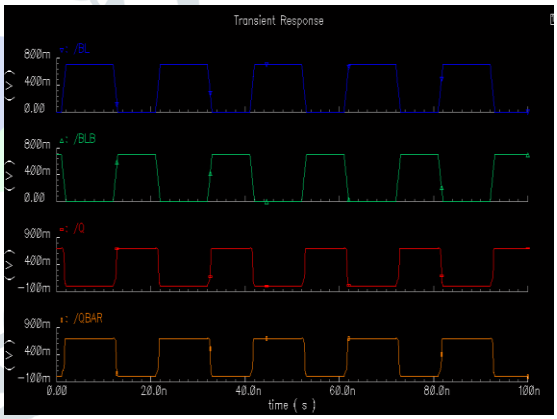


Fig.3 Transient Response of 9T SRAM Cell

IV. FINFET DEVICE STRUCTURE

The continuous downscaling of the bulk MOSFET creates many short channel effects, leakage currents, and device variations. But the non-planner FinFET has better control on short channel effects, better yield, low leakage currents and decreases the obstacle in scaling down of transistors [12]. In Double Gate (DG) FinFET the second gate is added opposite to the traditional gate as in MOSFET. The operation of FinFET depends upon its two gates. When the two gates are at same potential then the mode is said to be Shorted Gate (SG) operation. When both the gates are at the different potential then one gate is used for switching the device and another gate is used to control the threshold voltage of the transistor, this mode is said to be Independent Gate (IG) operation [12]. The gates of the FinFET are created on the vertical side of the fin,

whereas the source and drain are on the horizontal side as shown in figure 4.

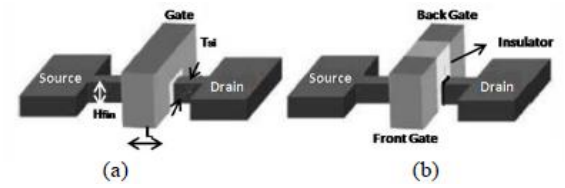


Fig 4: 3D view of (a) shorted gate FinFET (b) independent gate FinFET

The quantized width (W) is the multiple factors of the height of the fin (Hfin). The quantized width of the Shorted Gate (SG) FinFET can be estimated as:

$$W = 2 \times Hf_{in} + T_{si} \quad \text{.....(1.1)}$$

Whereas for Independent Gate (IG) FinFET the fin thickness (T_{si}) can be neglected for quantized width estimation:

$$W = 2 \times Hf_{in} \text{.....(1.2)}$$

In both, the cases to increase the width of the device number of fins are increased [13].

Two types of FinFET are described Shorted-gate (SG) and Independent-gate (IG) FinFET. SG FinFET is three-terminal devices with shorted gates whereas; IG FinFET is four-terminal devices with physically isolated gates. IG FinFET is more flexible than SG FinFET [12].

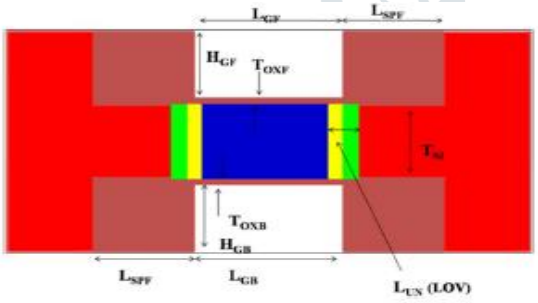


Fig.5 FINFET Structure

9T SRAM cell Using DG FINFET Technique

Double gate FINFET technique is applied on 9T SRAM Cell. Here self-determining control of the front and back gate in DG FINFET can be efficiently used to develop performance and reduce power consumption. In non-critical paths, self-determining gate control can be used to join together parallel transistors. A parallel transistor pair consists of two transistors with their source and drain terminals tied together. The second gate is added opposite to the conventional gate in Double-Gate (DG) FINFETS, which has been predictable for their prospective to superior control short channel effects, as well as to control leakage current. The operations of FINFET is recognized as short gate (SG) mode with transistor gates attached together, the independent gate (IG) model where self-determining digital signals are used to drive the two device gates, the low power and optimum power mode where the back gate is attached to a reverse-bias voltage to reduce leakage power and the hybrid model, which employs an arrangement of low power and self-determining gate modes. In due to its base material the uninterrupted down in scaling of bulk CMOS creates key issues. The crucial obstacles to the scaling of bulk CMOS nano-meter gate lengths include short channel effects, optimum current, gate-dielectric leakage, and device to device variations. The schematic of DG FINFET applied on 9T SRAM Cell is shown in Fig.6. The output waveform of 9T SRAM Cell using DG FINFET technique is shown in Fig.7.

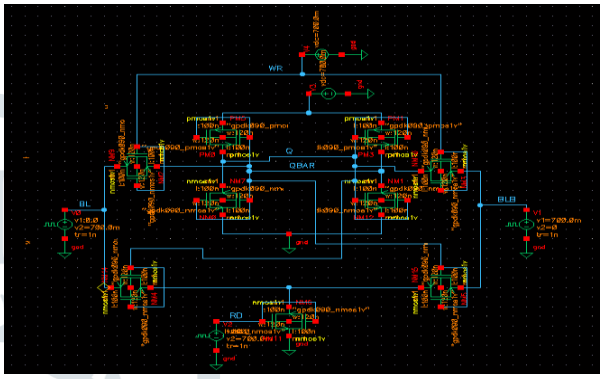
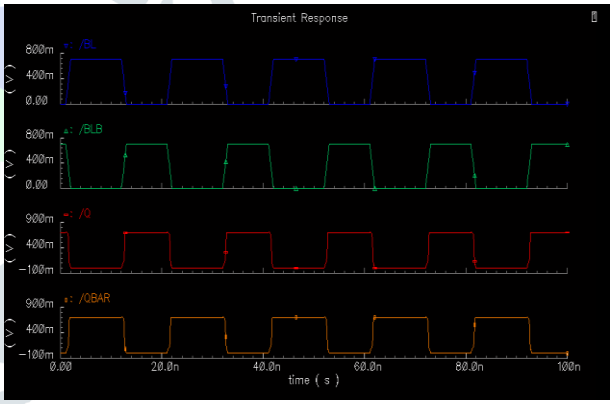


Fig.6 Schematic of DG FINFET applied on 9T SRAM Cell



The fig.7 Output waveform of 9T SRAM Cell using DG FINFET technique

V. RESULT AND DISCUSSION

9T SRAM Cell Simulation has been done on cadence tool using the 90nm technology with a nominal supply voltage 0.7 V. The gate leakage being the only dominant mechanism at room temperature 27°C, DG FINFET techniques applied on 9T SRAM Cell used for reduction of power consumption and maintaining the performance of 9T SRAM cell, the parameter like for power consumption, Average write delay and write power product delay.

Comparison Result Summary of 9T SRAM Cell is shown below table1.

Table 1 Simulated Result Summary

Performance Parameter	9T SRAM Cell	9T SRAM Cell using DG FINFET
Technology Used	90nm	90nm
Supply Voltage	0.7V	0.7V
Transistor Size	W=120 nM and L=100nM	W=120 nM and L=100nM
Low Power	16nW	14nW
Average Power	9.1 µW	7.7 µW
Average Write Delay	20ns	19.1ns
Write Power Product Delay ($e^{\wedge 13}$)	1.82	1.42

VI. CONCLUSION

The low power 9T SRAM cell at 90nm technology always consumes lowest leakage power and leakage current; improve read stability as compared to the conventional 6T SRAM cell. All the simulations were carried out in 90nm CMOS technology. In this paper, low power SRAM cell designs have been analyzed for power consumption, Average write delay and write power product delay. DG FINFET techniques have been employed to reduce the power consumed by the SRAM cell. The results show that the DG FINFET based SRAM cell is the best performer in terms of power consumption. The future work of this project can be the optimization of the SRAM cell and making it robust and reliable to the noise in the environment.

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