NOVAL 1-BIT FULL ADDER DESIGN IN QUANTUM DOT CELLAR AUTOMATA

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Abstract

In the near future, it is expected that the CMOS technology reaches to the end of its road map because of many serious challenges such as short channel effect, impurity variations, high cost of lithography and more importantly, the heat. So, many technologies such as Single Electron Transistor (SET), Resonant Tunneling Diode (RTD), and Carbon Nano tube Field Effect Transistor (CNFET) and Quantum dot Cellular Automata (QCA) have been emerged to solve the mentioned problems. According to the international technology road map for semiconductors (ITRS) report which offers an accurate summary of future technologies, QCA is one of the promising future solutions.

It has been found that the existing 3-input XOR gate are not only efficient and the structures are not well optimized in this way. To overcome this, and try to find new progressive structural optimization to generate desired full adder result. We have proposed a new low-complexity repulsive geometry structural gate DUT, which consumes less Area compared to prior designs. To evaluate the usefulness of proposed design a new one bit full adder circuit is presented. Our design achieves good improvement in cell count and consumes less area in comparison to the best single layer design. QCADesigner tool is used to validate the layout of the proposed designs. The usefulness of exhibited plans has been performed in QCADesigner form 2.0.3

Keywords: - Quantum Dot Cellular Automata, Nano Technology' QCA full adder, QCADesigner.

INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) has anticipated that size point of confinement of CMOS innovation will be constrained to around 5 nm to 10 nm and trusts this cutoff will be come to as ahead of schedule as 2017 [3]. The cutting edge processing devices are quantum PCs which depend on quantum mechanics. Quantum PCs depend on energy of photon and electron properties for performing figuring handling. They are parallel preparing that is a great many operations at any given moment. So the preparing velocity of a 30 qubit quantum PC will be in the scope of TeraHertz (THz). The latest advances that is being examined. The circuits engaged with quantum based PCs can be produced from the quantum dot gates and circuits.

John von Neumann, a Hungarian mathematician presented the idea of cell automata. The possibility of quantum calculation is by and large included to Feynman who proposed a computational model in view of quantum mechanical laws. The discrete idea of cell mechanization and quantum mechanics prompts the development of nanoscale circuits to perform calculation. One conceivable approach to keep up the development in circuit density is to change from CMOS based worldview to nanoscale extends. The primary favorable circumstances of such circuits high speed, high design density, little measure of energy utilization and there by energy saving. A quantum dot cell automata (QCA) is a rising nanotechnology.

In QCA, a cell binds two free electron and the logic values '0', '1'depends on position of electrons inside the quantum-dot cell, which are driven by Coulombic interaction. Different QCA based digital circuits have been investigated in recent years; structures for 5-input majority gate [5-13], designs for a one bit full adder [6, 9, 11, 52], QCA based memory cells, flip flops have also been studied. In most of the work, designs are not robust and vulnerable to fabrication defects due to wire crossing between the QCA components. So, an efficiently design of crossover wires can reduce the overall costs (i.e., both cell count and implementation complexity). Multilayer crossing is not favorable, due to its area overhead and fabrication issues [17]. However, coplanar crossover is achieved by the use of 450 rotated QCA cells [16], but end up with problems, such as reduce robustness and high implementation cost [17], due to two types of QCA cells. The idea behind this work is to devise area efficient and robust QCA circuits using single type cell, and analyze the power dissipation of existing and proposed majority gates. The proposed full adder design requires a lesser number of cells and draws little power compared to the best reported one in literatures. Further, an optimal single layer one bit full adder is designed by considering majority gate, which is based on single type cell.

The paper is organized giving a review on QCA logic, structures, elementary concern about full adder design and opportunity with QCA repulsive behavior to use in design aspect. Provides detail analysis about existing full adder mechanism. A new design of full adder and its simulation along with physical proof, and. we present a glimpse of available full adder circuits and based on new architecture design, an efficient one bit full adder is proposed. Simulated results of proposed designs and comparison to previous works are inspected and finally paper concludes.

QCA FUNDAMENTALS

Quantum-Dot Cellular Automata (QCA) is another nano technology worldview which encodes twofold data by charge setup inside a phone rather than the regular current switches. There is no present stream inside the cells since the columbic cooperation between the electrons is adequate for calculation. This worldview gives one of numerous conceivable answers for transistor-less calculation at the nanoscale. The standard QCA cells have four quantum dots and two electrons [16]. There are different dots of QCA cells proposed which incorporate a six-dot QCA cell and an eight-dot QCA cell. In a QCA Cell, two electrons possess askew inverse spots in the cell because of shared shock of like charges. A case of a basic unpolarized QCA cell comprising of four quantum dots masterminded in a square is as appeared in Fig.1 dots are basically puts where a charge can be limited. There are two additional electrons in the cell those are allowed to move between the four dots. Burrowing in or out of a cell is smothered. The numbering of the dots in the cell goes clockwise starting from the dot on the top right.

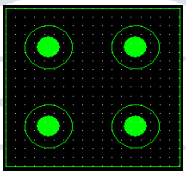

Figure: - 1 Simple 4-dot Unpolarized QCA cell.

A polarization P in a cell, that measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}$$

Where **ρi** is the electronic charge in each dot of a four dot QCA cell. Once polarized, a QCA cell can be in any one of the two possible states depending on the polarization of charges in the cell. Because of columbic repulsion, the two most likely polarization states of QCA can be denoted as P = +1 and P = -1 as shown in Fig.2. The two states depicted here are called most likely and not the only two polarization states because of the small (almost negligible) likelihood of existence of an erroneous state.

Figure:-2 P = +1 Binary Logic1 P = - 1 Binary Logic 0

LOGICAL DEVICES IN QCA

As found in the past areas, the data in QCA cells is exchanged due to columbic cooperation's between the neighboring QCA cells; the condition of one cell impacts the condition of the other. The essential rationale gadgets in QCA are:

- ✓ Binary Wires.
- ✓ Inverter.
- ✓ Majority Gate Voter

Binary Wire

A paired wire can be seen as an even arrangement of cells to transmit data starting with one cell then onto the next. A case of a QCA wire is as appeared in Fig. 3. A parallel wire is regularly separated into different clock zones, to guarantee that the flag doesn't fall apart as signs for the most part have a tendency to debase with a long chain of cells in a similar timing zone.

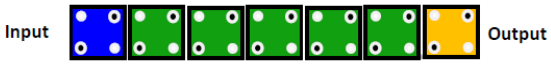

Figure: - 3 A QCA binary wire Realization

Inverter

Two diagonally aligned cells will have the opposite polarization. Henceforth, inverters can be implemented with lines of diagonally aligned cells. An example of a QCA Inverter is as shown in Figure

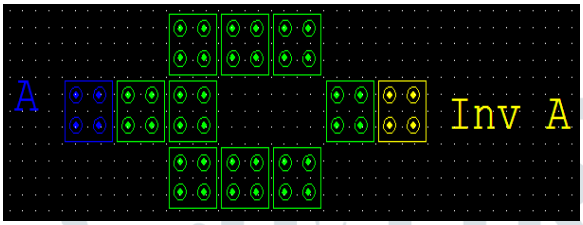

Figure: - 4 QCA designed inverter circuits

Majority Gate

Majority Gate (MV) is the fundamental logic block in any QCA design. A majority gate can be built with the help of five cells. The top, left and bottom cells are inputs. The device cell in the centre interacts with the three inputs and its result (the majority of the input bits) will be propagated to the cell on the right. An example of an MV representation in QCA is as shown in Figure 5. The logic function implemented by the MV is

$$f(A,B,C) = A.B + B.C + C.A$$

Consider the Coulombic cooperation between cells 1 and 4, cells 2 and 4, and cells 3 and 4. Coulombic connection between electrons in cells 1 and 4 would typically bring about cell 4 changing its polarization in light of electron aversion (accepting cell 1 is an info cell). Notwithstanding, cells 2 and 3 additionally impact the polarization of cell 4 and have polarization P=+1. Therefore, on the grounds that most of the cells impacting the gadget cell have polarization P=+1, it too will likewise accept this polarization on the grounds that the powers of Columbic collaboration are more grounded for it than for P=-1.

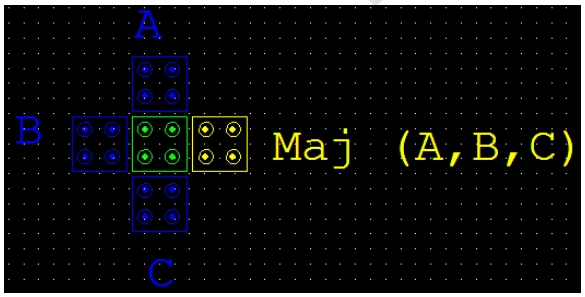

Figure:-5 A three input majority gate

THE QCA CLOCK

This section will clarify and talk about how the QCA clockworks. Not at all like the standard CMOS clock, has the QCA clock had more than a high and a low stage. The periods of the QCA clock and illustrations are talked about underneath.

The check in QCA is multi-staged. Individual QCA cells are not planned independently. The wiring required to clock every phone exclusively could without much of a stretch overpower the disentanglement won by the natural neighbourhood interconnectivity of the QCA design [8]. Four phase switching realized in each clocking phase for different clock zones. Information flows in a pipelined fashion from inputs towards outputs during four clock zones.

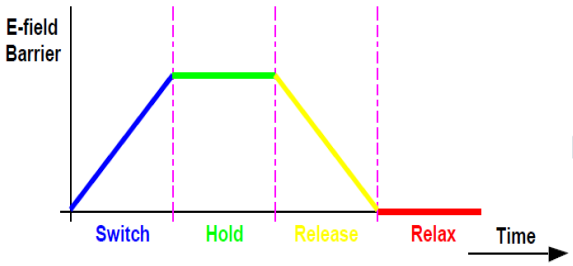

Figure: - 6 the four phases of the QCA clock

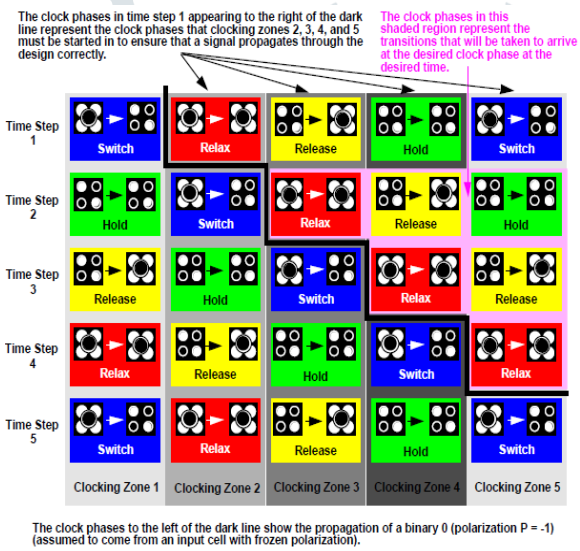

Figure: - 7 Clocking phases in different clock Zones

Now and time it merits specifying that there is some characteristic pipelining incorporated with the QCA innovation. After each 4 time steps, it is conceivable to put another esteem onto a QCA wire.

CROSSING

In QCA structures fabrication of interconnection between components needs to be handled efficiently for a better stability. Till now, there are two different types of crossover are available. These are coplanar and multilayer. In multilayer crossover, multiple layers are used as in CMOS circuit design for interconnection between components. In coplanar crossover strategy, wire crossing is done by two different cells. These cells are orthogonal to each other, so they operate without affecting neighboring cells. The first wire consists of cells of 90^0 orientations and second wire has only 45^0 orientations as shown in Figure 8. The main drawback of this scheme is that any misalignment of cells during fabrication may cause a cross coupling between the two wires. Works have been done to mitigate such effects, and also to increase the robustness of the circuits, but all these end up with large area overhead [14, 19]. Another type of coplanar wire crossing is addressed in S. H. Shin [21]. In this method wire crossing is based on interference of clocking phases as depicted in Figure.

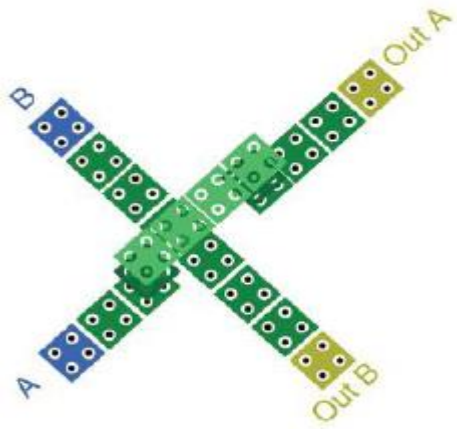

Figure: - 8 Crossover diagram different orientation

LITERATURE REVIEW

Various QCA full-adders have been presented to date. The first one (presented in 1994) is composed of five three-input majority gates and three inverters (Tougaw and Lent, 1994). This full-adder uses QCA coplanar wire.

Hashemi et al. 181 crossing scheme. It is implemented in one layer using 192 QCA cells. In this design QCA clocking concepts are not considered. In Vetteth et al. (2002) another QCA full-adder using the same logical structure and coplanar wire crossing scheme is presented. In contrast to the previous design, this full-adder incorporates QCA clocking scheme and takes 14 clock phases (3.5 clock cycles) to generate outputs. This full-adder was used in designing a 4-bit CLA (Vetteth et al., 2002). A simpler QCA full-adder is presented in (Wang et al., 2003). This full-adder is composed of three three-input majority gates and two inverters (Wang et al., 2003). It uses QCA coplanar wire crossing scheme and takes 5 clock phases (1.25 clock cycles) to produce outputs. Hence, it is faster than presented design in (Vetteth et al., 2002). The schematic of this full-adder is shown in Figure 10. Different layouts for this schematic have been presented to date (Cho and Swartzlander, 2007, 2009; Cho, 2006; Hänninen and Takala, 2010; Kim et al., 2007; Zhang et al., 2005). The presented QCA full-adder in (Zhang et al., 2005) utilizes QCA multilayer wire crossing scheme and is simpler than previous design (Wang et al., 2003) in terms of cell count. It produces outputs in 4 clock phases (1 clock cycles); hence, it is faster than the previous designs. In the study of Cho and Swartzlander (2007) another QCA full-adder using the same logical structure and multilayer wire crossing scheme is presented. It takes 5 clock phases (1.25 clock cycles) to produce outputs. This full-adder was used to implement three kinds of adders (Ripple carry adder, carry look ahead adder and conditional sum adder) with large word sizes (Cho and Swartzlander, 2007). These adders were compared in terms of area, complexity (cell count) and delay (Cho and Swartzlander, 2007). Two other QCA full-adders (presented as Type I and II) using five gates (three majority gates and two inverters) are introduced in (Cho, 2006). These designs utilize QCA multilayer wire crossing scheme. The presented adder as Type II is more efficient in designing large adder circuits (Cho and Swartzlander, 2009; Cho, 2006). It is constructed using 86 QCA cells and takes only 3 clock phases (0.75 clock cycles) to produce outputs. This full-adder dominates all the previous designs in terms of area, complexity (cell count) and delay. In Hänninen and Takala (2010); Kim et al. (2007) robust QCA full-adders are presented. These designs use the coplanar wire crossing scheme for crossover wires. The presented design in (Hänninen and Takala, 2010) surpasses the presented design in (Kim et al., 2007) in terms of area, delay and complexity (cell count). Another QCA full-adder design is presented in (Rahimi et al., 2007). This adder is constructed using unconventional form of QCA cells. It is composed of two majority gates and one inverter. In this design in contrast to the previous structures, implemented using three-input majority gates, one of the majority gates is a five-input voter. In order to implement this schematic, a cubic design for QCA cells is presented in (Rahimi et al., 2007). This cubic cell has six sides and can be used to implement a five-input majority gate (Rahimi et al., 2007).

Finally the last one design based A novel 3-input XOR gate based on the cellular interaction is first proposed which consists of 10 cells and requires two clocks. To demonstrate the efficiency of the proposed XOR gate, an optimized single layer full-adder is designed here which contains only 20 cells and requires three clock phases.

PROPOSEED DESIGNS

In this section, a novel efficient full adder circuit in QCA nanotechnology is proposed. Our proposed design is implemented in one layer and has significantly lower number of quantum cells, lower energy consumption and smaller area even in comparison with its multilayer and complex design counterparts. This exploration could clear path for custom circuit designs which were not attainable in other processing advances.

As observed towards the fruition of the past portion, the measure of agents who have worried upon the utilization of reconfiguration for centrality beneficial enrolling are not a great deal of at any rate the examination that has been done by them have given an obvious sign

that there are lanes for control theory holds. Full adder is the most important building block of arithmetic units and Improving the efficiency of this circuit leads to improvement of the efficiency of the whole processor. Due to the importance of the reversible computation based on QCA some researchers have already been done for designing QCA-based reversible logic gates as the building blocks of QCA-based reversible computational circuits such as full adder cells [11]. However, they lead to cell count and area redundancy for designing full adder circuit which is the most fundamental block of the arithmetic unit in each digital processor. In addition, they require rotated cells or multilayer wire crossings which lead to lower manufacturability and robustness. Our point is to happen upon with a reconfigurable design utilizing QCA which influences utilization of the dominant part to gate logical and the timing system which lessens the power significantly in contrast with the current models. The proposed technique recommends a viable answer for intelligent wiring with a lessened number or without of external fixed input cells giving certain values of info. In a run of the nano QCA circuit, both 0 and 1 fixed input are expected to execute functionality. The proposed strategy introduces certain value equipment which can lessen the quantity of required fixed inputs. In the same we avoid the multi layer and crossover circumstances in the design and all design are contracted in the single layer and single type of cells.

PROPOSED 1-BIT FULL ADDER

In this paper, we propose QCA full adder design there, we use a similar quantum cell technology to generate full adder desire result in a single layer formation with Boolean function satisfaction as per as full adder algorithm. Furthermore, a similar time we lessen the outer settled esteem contribution to ad lib our plan as indicated by our future extension.

Accordingly, by using this methodology, we design a new propose full adder design we have inputs A,B and C two output Carry and Sum who produce the two Boolean function, that is Carry = AB+BC+AC and second one is Sum = $A \oplus B \oplus C$, As we seen in the diagram.

Design of one bit full adder, even larger bits and incorporating with least quantum cell uses because before this work many researchers to the great work on this, that's by it is a challenging task for us. For such systems, the complexity increases in terms of number of quantum cell and wires crossing, so more prone to defects that occurs due to QCA fabrication of single layer crossing using two different cells (90˚ and 45˚) in a single layer layout. an optimal single layer QCA based full adder is designed and implemented using proposed geometric design, which incorporates the robust single layer crossing method using single cell (90^0). For implementation, it requires only 17 cells and spreads over a lesser area. It consumes two clock phases to produce valid carry output and Sum. The layout of the proposed full adder is shown in Fig. 10, which utilizes a coplanar 3-input majority gate and separate geometric design for generate Summing output. The QCADesigner based simulation result for the proposed full adder. This indicates the correct operation of proposed structure and a valid output immediate clock cycle.

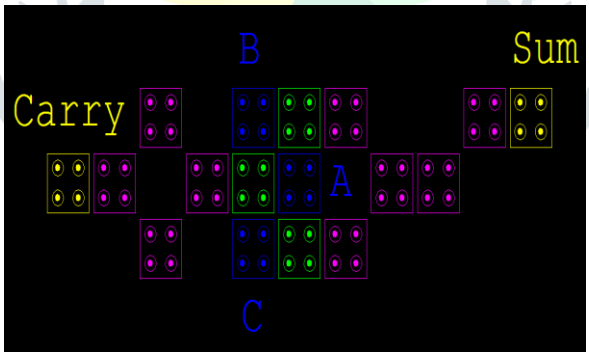

Figure 10 Layout of Propose Full Adder Design

SIMULATION RESULT AND ANALYSIS

The simulation setup has been developed for two different functionality circuits design. The simulation has been performed on QCADesigner form 2.0.3 device these proposed circuits simulate and analyze the outcome on different parameters of quantum Dot cell automata technology.

The measure of each QCA cell is set 18x18 nm with 5 nm width quantum dots. The parameters for a bistable estimate are as per the following: 0.001 convergence tolerance, 12.9 relative permittivity, 9.8e-22 J clock high, 3.8e-23 J clock low, 11.5 layer separation, and 100 maximum iterations per sample. The circuit design, generate the minimum supply voltage required to the tread-off between power and delay. The simulation results authenticate the correct operation of the proposed circuits. The reproduction comes about verify the right operation of the proposed circuits with all possible combination of full adder algorithm.

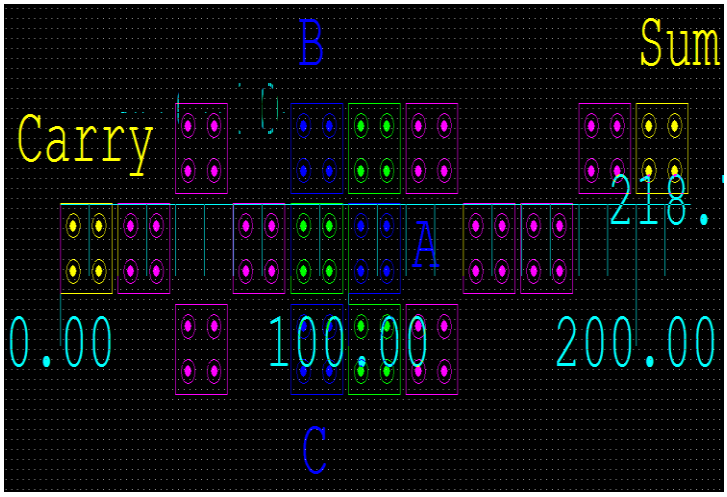

Figure 11 Grid view Layout of propose Full Adder with Area Calculation

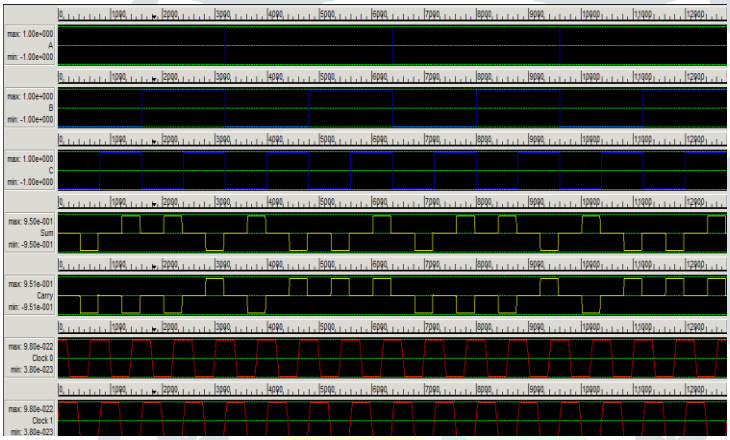

Fig. 12 Simulation Wave form of Full Adder Design

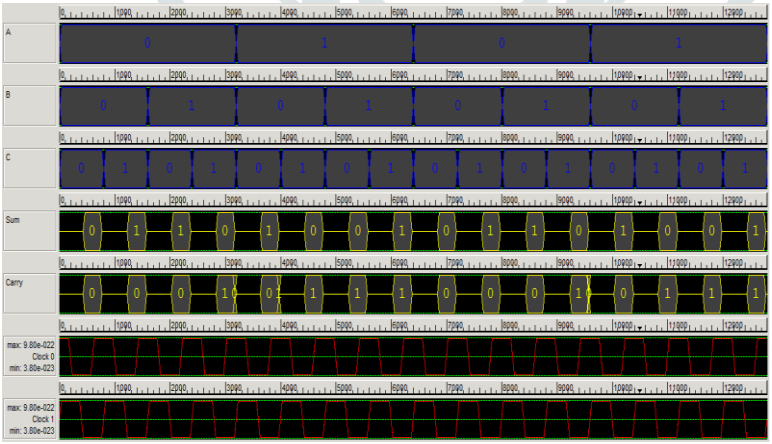

Fig. 13 Simulation Bus Wave form of Full Adder Design

AREA AND CELL COUNT

DESIGN	AREA (μm^2)	CELL COUNT	LAYER USED	Clock Delay
Previous Full Adder [51]	0.06	38	Single	1
Previous Full Adder[9]	0.02	33	Single	0.5
Previous Full Adder[51]	0.03	31	Multi	0.75
Previous Full Adder[11]	0.02	29	Single	0.5
Previous Full Adder[15]	0.01	23	Multi	0.75
Previous Full Adder[8]	0.01	22	Multi	0.75
Previous Full Adder[1]	0.016	20	Single	0.75
PROPOSE FULL ADDER	0.0126	17	Single	0.5

In the past few sections, we have clearly explained how the proposed 1-bit full adder performs computation without any requirement of external fixed inputs compare to the previous designed digital full adder circuits. This gives us an enormous advantage with regard to power consumption and area as the number of QCA cells remains the less. For our proposed full adder design cells are only 17 cells. QCA cells are extremely area efficient for digital circuits and beneficiary for next generation designs. It typically has an area of 0.0126 µm2 with a normal cell dimension. A table depicting the area advantage posed by our design in comparison to existing adder is as shown in Table.

CONCLUSION

In this work, an efficient full adder design has been proposed with physical and analytical proofs of design. To support this, a detailed analysis of structural, geographical and power issues of all prior ones and proposed full adder performed. To investigate area, fixed external inputs and clock used using QCADesigner 2.0.3 tool. To showcase the efficacy of the proposed design, a new one bit full adder structure was introduced, which inculcates coplanar non-crossover wires, via clock phasing. It is observed that these coplanar structures are robust for considerable variation in temperature and yield more compact digital circuits with respect to existing designs. The results confirmed that the presented structures have outperformed all prior designs and shows significant improvements in terms of power consumption, complexity, area occupation and input to output clock delay. Proposed optimal structures can lead to designing of more complex and high performance QCA nanoscale circuits in the future.

As example is towards the nano-scale organization edge voltage of QCA is generally used for reduction of delay and power yet to perform complete limit of circuit continually we vanish the requirement of fixed Input signal for the propose 1-bit full adder. The proposed circuit is getting less conspicuous as the supply voltage is downsized. In this work a superior QCA neno-technology has been displayed which diminishes outer settled contribution to change plan engineering perspective edge voltage additionally conspicuous pretend in QCA neno-technology.

Correlation examination of successful zones utilized and control use ultra low power Quantum Dot Cell with scaled cut-off voltage decreases latency delay and power usage with extensive sum. Impact of data vectors, Delay, power and supply voltage.

Research is also needed for using the proposed custom wire crossing techniques in more complex circuits and the principal of using the less computation time in clocking scheme should be exploited. Circuits that make use of clocking scheme can be designed and tested for efficiency in terms of area, power and performance.

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