Efficient 2:1Multiplexer Designing using Quantum dot Cellular Automata

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Abstract

As CMOS scaling faces a technological barrier in these days, novel design paradigms are being proposed to keep up with the ever growing need for computation power and speed. Most of these novel technologies have device sizes comparable to atomic and molecular scales. At these levels the quantum mechanical effects play a dominant role in device performance, thus inducing uncertainty. The wave nature of particle matter and the uncertainty associated with device operation make a case for probabilistic modeling of the device. As the dimensions go down to a molecular scale, functioning of a nano-device will be governed primarily by the atomic level device physics. Modeling a device at such a small scale will require taking into account the quantum mechanical phenomenon inherent to the device.

The Quantum-Dot Cellular Automata (QCA) is a radical nanotechnology, which works at nano-scale. In this paper, an optimal design of 2n:1 Multiplexer (MUX) is presented. A new approach has been devised to implement efficient digital logic gates using the proposed 2n:1 multiplexer. To verify the functionality of the proposed structures and Boolean proofs are performed. A detailed comparison, structural evaluation of the proposed multiplexer with recently robust designs is analyzed. This evaluates the performance of the proposed multiplexer in terms of cell count, area clock delays as compared to traditional approaches. The usefulness of exhibited designs has been performed in QCADesigner form 2.0.3 tool

Keywords: - Quantum Dot Cellular Automata, 2:1 multiplexer, QCA, CMOS, VLSI, Nano-technology.

INTRODUCTION

The microelectronic industry is experiencing new challenges for continuing the Moore's law [1]. Therefore, new alternatives are introduced to overcome the physical problems of CMOS [2]. New technology Quantum-dot Cellular Automata (QCA) neglects the physical problems of CMOS [3]. It has attained considerable worldwide attentions due to its attractive characteristics such as ultra-high speed (THz), high device density, and low power consumption. QCA circuits are made up of QCA cells; each cell consists of four quantum-dots, in which two electrons are loaded in antipodal sides [4]. The binary information is encoded by these two electrons rather than current or voltage levels (Transistors are current based devices).

QCA is a new digital system for next generation [3−4]. Majority gate [4] and Inverter cell [4] are two main primitive logic gates for circuit designs in QCA nanotechnology. Till now various QCA based logic

Circuits have been implemented [4−15]. Majority gate and Inverter cell has desirable features to implement logic for QCA. However, still the logic is not competent and research is continuous due to the current trends of complexity, power and area constraints. Majority gate & Inverter cannot reduce the circuit complexity and maximizes the device density in QCA circuits alone. These gates are not functionally complete to design all logic circuits. The main focus of all new techniques is to reduce circuit parameters and excels these major issues. Multiplexer is the most frequent combinational component used in digital logic systems. The multiplexer is a very useful electronic circuit that has uses in many different applications such as signal routing, data communications and data bus control applications. Based on this various arrangements of the QCA cells widespread range of QCA multiplexers designs are realizable [5−15]. Efficient QCA Multiplexer (MUX) design is a problem that has been brought the attention of the research community. Many research works have been carried out to design an efficient multiplexer [5−15]. Multiplexer are used in various fields where multiple data need to be transmitted using a single line.

This paper presents the simple and efficient 2:1 Multiplexer using QCA technology. The proposed 2:1 Multiplexer have enhanced the performance of several conventional designs in terms of power, area, clock delays and circuit complexity. The detailed comparison is of the proposed and conventional Multiplexers with regards to various characteristics are presented in the discussion.

QCA PRELIMNARIES

Quantum-Dot Cellular Automata (QCA) is another nano technology worldview which encodes twofold data by charge setup inside a phone rather than the regular current switches. There is no present stream inside the cells since the columbic cooperation between the electrons is adequate for calculation. This worldview gives one of numerous conceivable answers for transistor-less calculation at the nanoscale. The standard QCA cells have four quantum dots and two electrons [16]. There are different dots of QCA cells proposed which incorporate a six-dot QCA cell and an eight-dot QCA cell. In a QCA Cell, two electrons possess askew inverse spots in the cell because of shared shock of like charges. A case of a basic unpolarized QCA cell comprising of four quantum dots masterminded in a square is as appeared in Fig.1 dots are basically puts where a charge can be limited. There are two additional electrons in the cell those are allowed to move between the four dots. Burrowing in or out of a cell is smothered. The numbering of the dots in the cell goes clockwise starting from the dot on the top right.

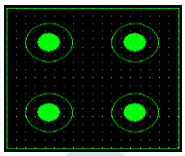


Figure 1 Simple 4-dot Unpolarized QCA cell.

A polarization P in a cell, that measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}$$

Where **ρi** is the electronic charge in each dot of a four dot QCA cell. Once polarized, a QCA cell can be in any one of the two possible states depending on the polarization of charges in the cell. Because of columbic repulsion, the two most likely polarization states of QCA can be denoted as P = +1 and P = -1 as shown in Fig.2. The two states depicted here are called most likely and not the only two polarization states because of the small (almost negligible) likelihood of existence of an erroneous state.

Figure 2 P = +1 Binary Logic1 P =- 1 Binary Logic 0

LOGICAL DEVICES IN QCA

As found in the past areas, the data in QCA cells is exchanged due to columbic cooperation's between the neighbouring QCA cells; the condition of one cell impacts the condition of the other. The essential rationale gadgets in QCA are:

- Binary Wires.
- Inverter.
- Majority Gate Voter

Binary Wire

A paired wire can be seen as an even arrangement of cells to transmit data starting with one cell then onto the next. A case of a QCA wire is as appeared in Fig. 3. A parallel wire is regularly separated into different clock zones, to guarantee that the flag doesn't fall apart as signs for the most part have a tendency to debase with a long chain of cells in a similar timing zone.

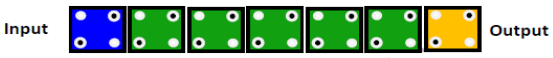


Figure 3 a QCA binary wire Realization

Inverter

Two diagonally aligned cells will have the opposite polarization. Henceforth, inverters can be implemented with lines of diagonally aligned cells. An example of a QCA Inverter is as shown in Figure

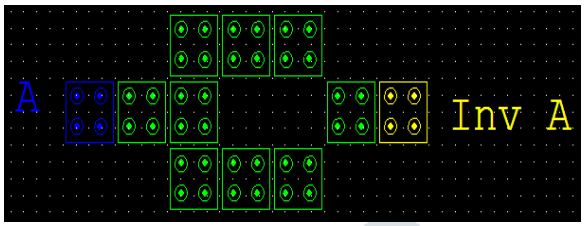


Figure 4 QCA designed inverter circuits

. **Majority Gate**

Majority Gate (MV) is the fundamental logic block in any QCA design. A majority gate can be built with the help of five cells. The top, left and bottom cells are inputs. The device cell in the centre interacts with the three inputs and its result (the majority of the input bits) will be propagated to the cell on the right. An example of an MV representation in QCA is as shown in Fig. 5. The logic function implemented by the MV is

Consider the Coulombic cooperation between cells 1 and 4, cells 2 and 4, and cells 3 and 4. Coulombic connection between electrons in cells 1 and 4 would typically bring about cell 4 changing its polarization in light of electron aversion (accepting cell 1 is an info cell). Notwithstanding, cells 2 and 3 additionally impact the polarization of cell 4 and have polarization P=+1. Therefore, on the grounds that most of the cells impacting the gadget cell have polarization P=+1, it too will likewise accept this polarization on the grounds that the powers of Columbic collaboration are more grounded for it than for P=-1.

$$f(A,B,C) = A.B + B.C + C.A$$

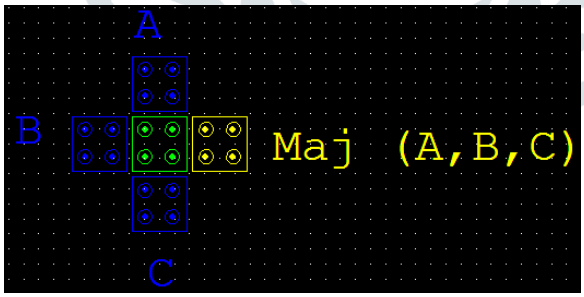


Figure 5 A three input majority gate

THE QCA CLOCK

This section will clarify and talk about how the QCA clockworks. Not at all like the standard CMOS clock, has the QCA clock had more than a high and a low stage. The periods of the QCA clock and illustrations are talked about underneath.

The check in QCA is multi-staged. Individual QCA cells are not planned independently. The wiring required to clock every phone exclusively could without much of a stretch overpower the disentanglement won by the natural neighbourhood interconnectivity of the QCA design [8]. Four phase switching realized in each clocking phase for different clock zones. Information flows in a pipelined fashion from inputs towards outputs during four clock zones.

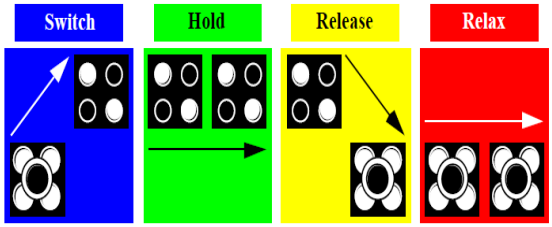


Figure 6 the four phases of the QCA clock

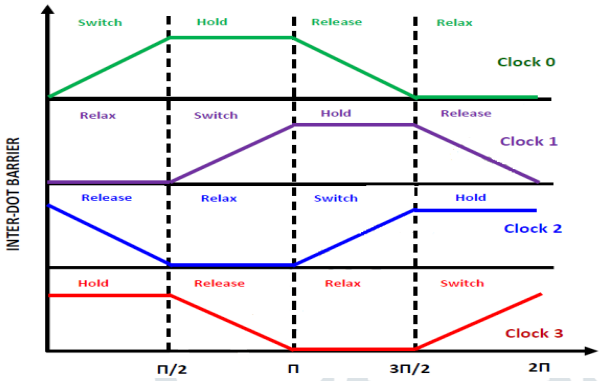


Figure 7 Clocking phases in different clock Zo

Now and time it merits specifying that there is some characteristic pipelining incorporated with the QCA innovation. After each 4 time steps, it is conceivable to put another esteem onto a QCA wire.

LITERATURE REVIEW

Based on various arrangements of the QCA cells widespread range of QCA multiplexer designs have been reported in [5–15]. Kim et al. have analyzed the causes of the failure of QCA circuits and have proposed an adder circuit which utilizes a multiplexer with proper clocking scheme [5]. Multiple input QCA design depends on all the inputs which result in a variety of sneak noise paths in QCA [5]. They systematically analyzed the sneak noise paths in QCA- based design by using the concept of kink energy. And this analysis is significant due to its influence as the design size grows. They have also analyzed the failure of majority gates, and then they used the coplanar clocking technique in the design of full adder to overcome the errors. The multiplexer which has been used by them uses clock gating which is faster and smaller. Mardirisi and Karafyllid [6] have proposed modular 2n: 1 multiplexer which is formulated to increase the circuit stability. They have used the concept of crossover design for signal propagation and have shown each logic gate with blocks. Each block consists of two pairs of cells serially connected which produces signal delay equal to the number of included cell pairs. Hashemi et al. [25] have proposed multiplexer in three layers in which the first layer is the backbone of the circuit. This new design is denser with four clocks latency and faster. In [10] Roohi et al. have designed 2:1 multiplexer using three clock zones due to this delay have been increased. In [10] Sen et al. have proposed a modular design of 2:1 MUX, with less delay involved.

Due to its abundant use, it has become necessary to implement a multiplexer circuit which is area efficient and results in the reduction of the cost of designing. Various QCA based Multiplexers have been implemented [7–11]. However, still the circuit is not competent and research is continuous with the current trend of complexity, power and area constraints. This motivates to think and develop an efficient design of 2:1 MUX, which can be further used to design any complex logic. Hence, in this paper a new 2:1 MUX is proved to be efficient in terms of clock delays, complexity, and area constraints. In addition, the power dissipation analysis of the proposed 2:1 MUX is done to check the power consumption.

PROPOSEED DESIGNS

A new approach has been devised to implement the 2:1 multiplexer. It is a universal circuit. Any Boolean function can be implementing using the proposed MUX. It has 2n inputs, one output and n=1 select lines, which transfers one of input to the output based on the value of the select lines. The proposed MUX has been constructed using the modified Majority Gate. The proposed promising structure is less complexity and powerful in terms of implementing logic.

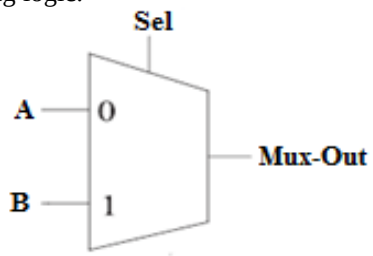


Figure 8 basic block diagram of multiplexer

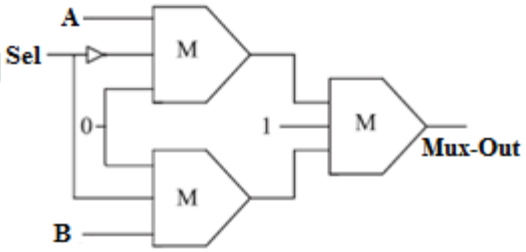


Figure 9 functional diagram of multiplexer

The schematic representation of the 2:1 MUX is shown in Figure 9. It has two data inputs **A** and **B**, one select line **Sel** and one output (**Mux-Out**). The block diagram is shown in Figure 8. The output logic expression for 2:1 MUX is worked out as:

$$\textbf{Output} = A.\overline{Sel} + B.Sel$$

The layout and simulation results of the proposed design are shown in Figure 10 respectively. As is obvious, the output (MUX) generate meticulous highly polarized signals (shown inside the rectangles) leading to provide a high drivability for the circuit. The proposed MUX consists of an area 3888 nm2, circuit complexity of 12 cells and latency of 0.5 clock delays. The QCA majority output logic expression of the proposed 2:1 MUX is worked out as:

$$\overline{\text{Output}} = Mj\,(Mj\,(A, Sel, 0), Mj\,(B, Sel, 0), 1)$$

Use recommends a viable answer for intelligent wiring with a lessened number of external fixed input cells giving settled sources of info. In a run of the nano QCA circuit, both 0 and 1 fixed input are expected to execute a capacity. The proposed strategy introduces settled esteem generator equipment which can lessen the quantity of required fixed inputs.

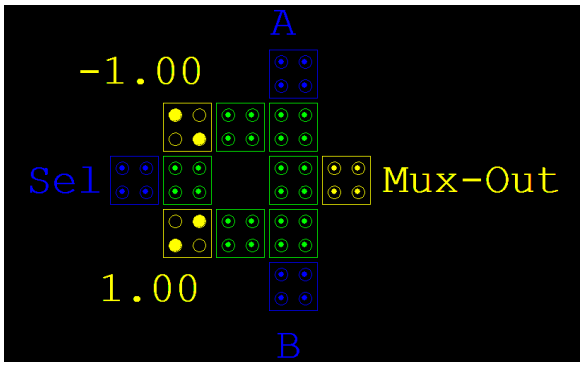


Figure 10 Layout of Propose Multiplexer Design

SIMULATION RESULT AND ANALYSIS

QCADesigner ver. 2.0.3 [26] is used for verifying the proposed circuit. QCADesigner tool, with default parameters have been used for verified the functionality of the proposed QCA-circuits. The default parameters are listed as: QCA cell size=18 nm, diameter of quantum dots = 5 nm, number of samples = 12, 8000, convergence tolerance = 0.001, radius of effect = 65 nm relative permittivity = 12.9, clock low = 3.8e−23 J, clock high = 9.8e-22 J, clock amplitude factor = 2.000, layer separation = 11.5 nm and maximum iterations per sample = 100.

The construction of the proposed 2:1 MUX is simple, it is composed of rotating two 2-input AND, using a common fixed polarized QCA cell and a two-input OR gate. The main focus of this implementation is to reduce circuit complexity and increase efficiency. To procure highly integrated QCA layouts, several new methods have been used to propose multiplexers [5–15]. Multiplexer circuits, presented in references [9–14] have reduce maximum number of cell counts, reduced clock delays and consists of less area in comparison to [5–8]. Accordingly, MUX presented in [15] consists of less cell counts, reduced clock delays and less area occupation in comparison to [9–14]. However, in contrast, the proposed MUX shown in Fig. 10 has an influential role in overall circuit performance in terms of area occupation and cell counts as shown in Table 1. It is implemented using explicit QCA fixed cells. The proposed MUX has been testified for designing several multi-bit ultrahigh speed MUX.

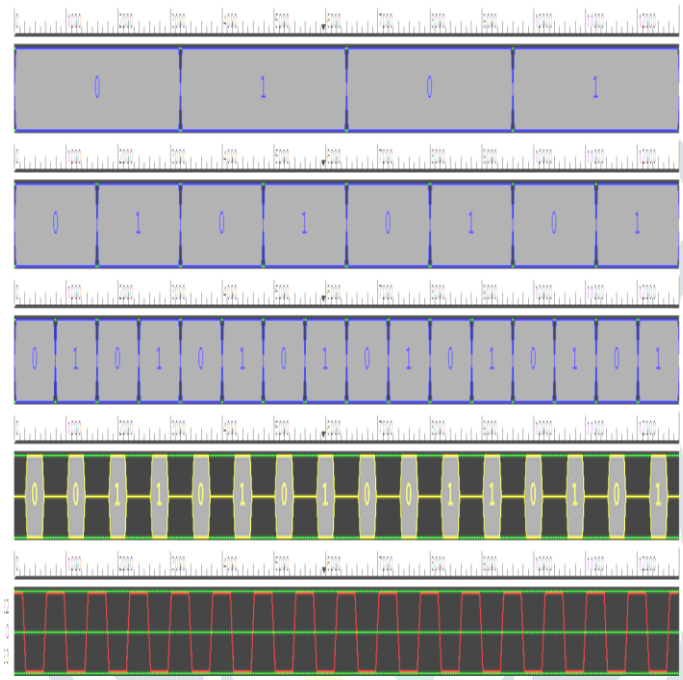


Figure 11 Simulation Bus Wave form multiplexer design

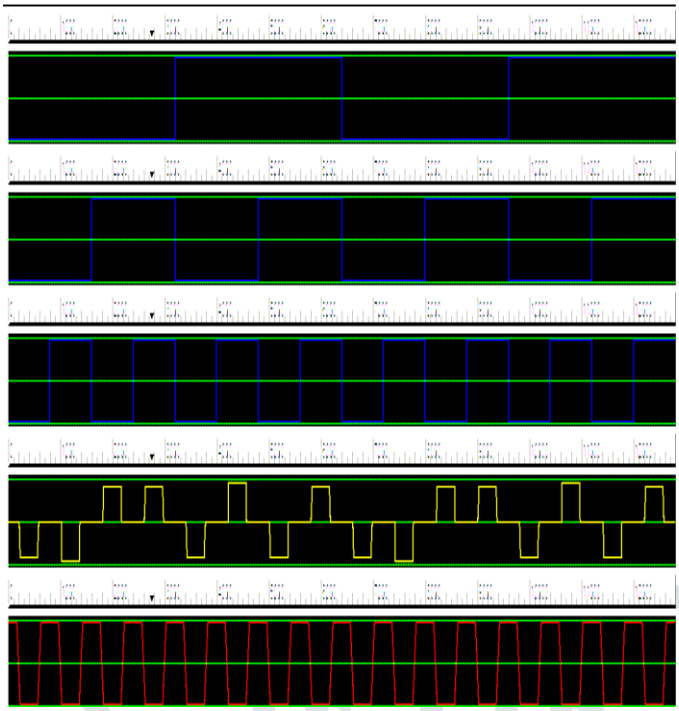
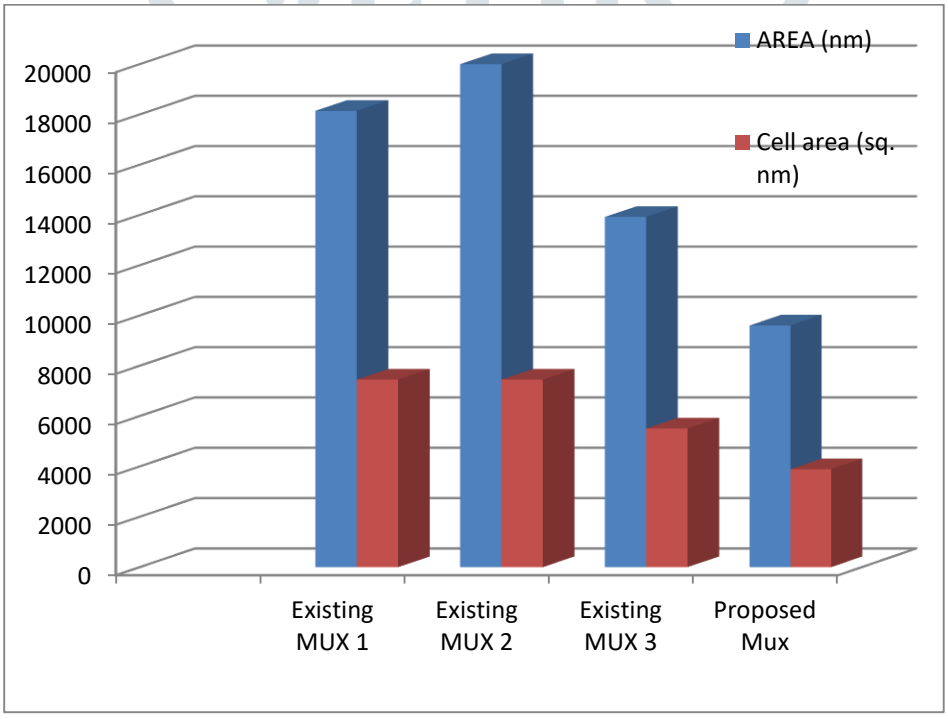


Figure 12 Simulation Wave form multiplexer design

Table: Comparison Table between exiting and proposed mux

DESIGN	AREA (nm)	CELL COUNT	Cell area (sq. nm)	EXTERNAL FIXED INPUT	NO OF CLOCK USED
Existing MUX 1	18144	23	7452	4	4
Existing MUX 2	20000	23	7452	3	2
Existing MUX 3	13924	17	5508	3	3
Proposed MUX	9604	12	3888	2	1



Graph between area, cell area of existing and proposed de

As shown in Comparison table and graph shows the our proposed multiplexer design improved to exiting multiplexer designs in terms of area, cell count and the clock used in the design that calculate the delay of the design how much clock used in the design than delay are increased in the design circuit and latency are poor in that case.

CONCLUSION

This paper presents novel approach to implement 2:1 MUX circuit using 2 electrons 4 Dot QCA. The proposed 2:1 MUX has been used to implement basic digital logic elementary for QCA. Any higher order MUX can be implemented using the proposed 2:1 MUX respectively. Therefore, using the proposed 2:1 MUX, an efficient 4:1MUX has been proposed.. The proposed design has shown

significant improvements in comparison to previously designed multiplexers in terms of area and complexity. In addition, to demonstrate the utility of the proposed 2:1 MUX a novel multiplexing concept has been proposed.

FUTURE WORK

Even though we have taken a big step forward in the design of area efficient circuits there are still many open ended questions which needs to be answered. One interesting future work will be to design the underlying clocking network. Some of the other areas where one can focus their research include the 4, 8 and 16 bit adder and compare it with both the existing designs and the designs proposed as part of this thesis. Research is also needed for using the proposed custom wire crossing techniques in more complex circuits and the principal of using the dead computation time in clocking scheme should be exploited. Circuits that make use of clocking scheme can be designed and tested for efficiency in terms of power and performance.

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