# IMPLEMENTATION OF A LOW AREA AND FAST SPEED MULTIPLIER FOR ALU USING VEDIC MATHEMATICS

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## Abstract :-

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. The ever increasing demand in enhancing the ability of processors to handle the complex and challenging processes has resulted in the integration of a number of processor cores into one chip. Still the load on the processor is not less in generic system. This load is reduced by supplementing the main processor with Co- Processors, which are designed to work upon specific type of functions like numeric computation, Signal Processing, Graphics etc. The speed of ALU depends greatly on the multiplier.Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. Employing these techniques in the computation algorithms of the coprocessor will reduce the complexity, execution time, area, power etc. This work presents different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier.

**Keywords** — Vedic mathematics ,Urdhva Tiryakbhyam Sutra ,Vedic multiplier.

## I. INTRODUCTION

The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. It deals with various branches of mathematics like arithmetic, algebra, geometry etc. Vedic mathematics is the name given to the ancient system of mathematics. It is a technique of calculations based on simple rules and

principles with which many mathematical problems can be solved, be it arithmetic, algebra, geometry or trigonometry. It is mainly based on sixteen principles which are termed as Sutras.

The system is based on 16 Vedic sutras which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The beauty of Vedic mathematics lies in the fact that it reduces the calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works.

***These Sutras along with their brief meanings are enlisted below alphabetically*.**

1) (Anurupye) Shunyamanyat -If one is in ratio, the other is zero.
2) ChalanaKalanabyham -Differences and similarities.
3) Ekadhikina Purvena- By one more than the previous One.
4) Ekanyunena Purvena -By one less than the previous one.
5) Gunakasamuchyah-Factors of the sum is equal to the sum of factors.
6) Gunitasamuchyah-The product of sum is equal to sum of the product.
7) Nikhilam Navatashcaramam Dashatah -All from 9 and last from 10.
8) Paraavartya Yojayet-Transpose and adjust.
9) Puranapuranabyham -By the completion or noncompletion.
10) Sankalana- vyavakalanabhyam -By addition and by subtraction.
11) Shesanyankena Charamena- The remainders by the last digit.
12) Shunyam Saamyasamuccaye -When the sum is same then sum is zero.
13) Sopaantyadvayamantyam -The ultimate and twice the penultimate.
14) Urdhva-tiryakbhyam -Vertically and crosswise.
15) Vyashtisamanstih -Part and Whole.
16) Yaavadunam- Whatever the extent of its deficiency

A simple multiplier (referred as Vedic multiplier) architecture based on the Urdhva Triyakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. In this paper, after a gentle introduction of this Sutra, it is applied to the binary number system to make it useful in the hardware. The hardware architecture of the Vedic multiplier is presented.[10]

## II. METHODOLOGY

The multiplier is based on an algorithm Urdhva Tiryakbhyam of Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”.

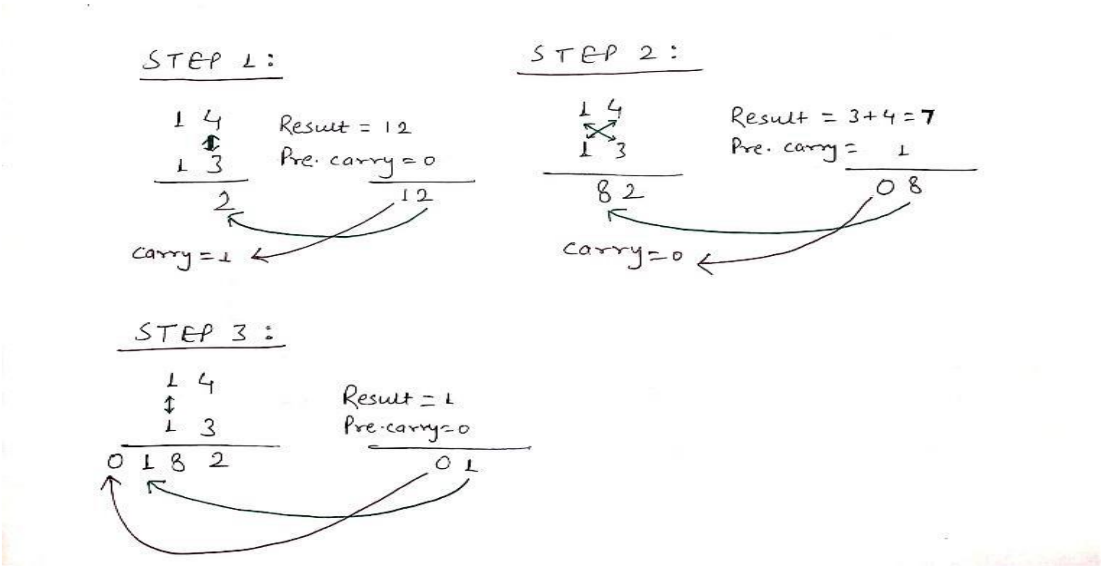


Figure 1: Example of multiplication using URDHVA TRIYAKBHYAM

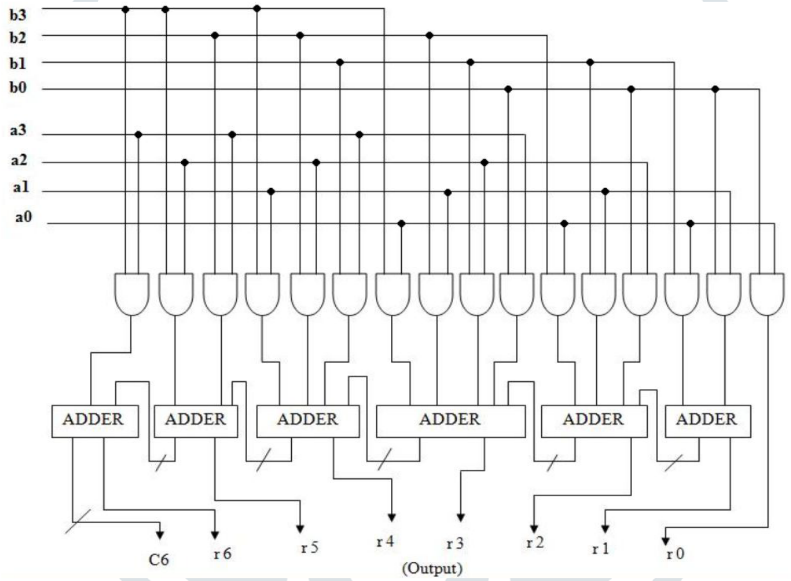


Figure 2: Architecture of Urdhva Trikyakbhyam

Based on the above architecture and the logic, the schematic is drawn in Xilinx ISE 9.2i Tool for design and testing various multiplier implementations. Design entered in the form of schematic .Various simulations are done for early testing. Input has been given through a test bench waveform. Synthesis reports and simulations (Post-route simulation) have been done for device Virtex XCV 300 - 6PQ240.

# III. RESULT

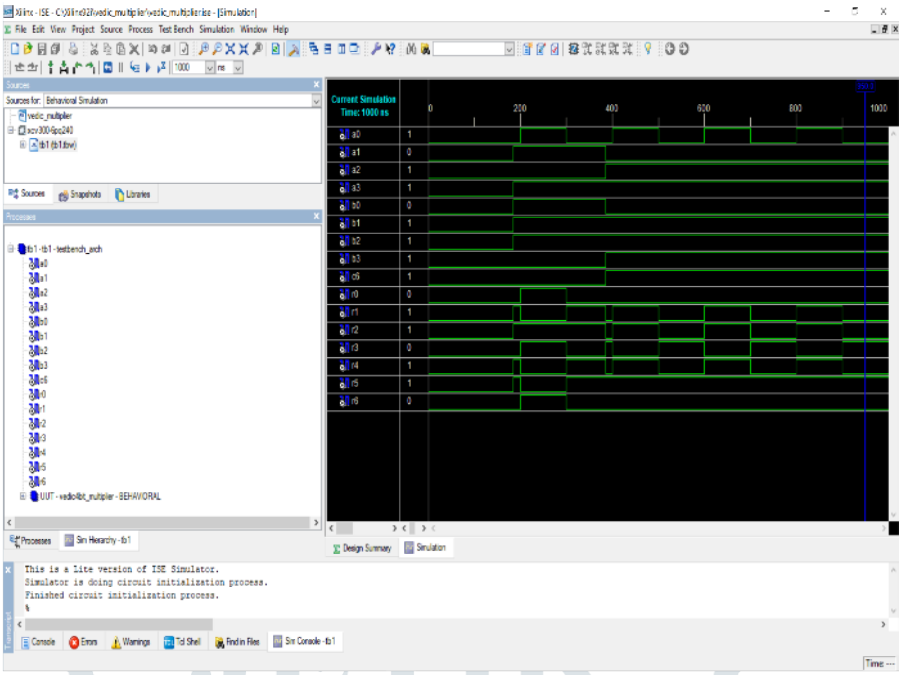

Figure 3: Input- Output Waveform

**Description:**

a : Input data 4 – bit

b : Input data 4 – bit

r0- c6 : Output data 8 – bit

a3- a0 = 1110

b3- b0 = 1101

c6- r0 = 10110110

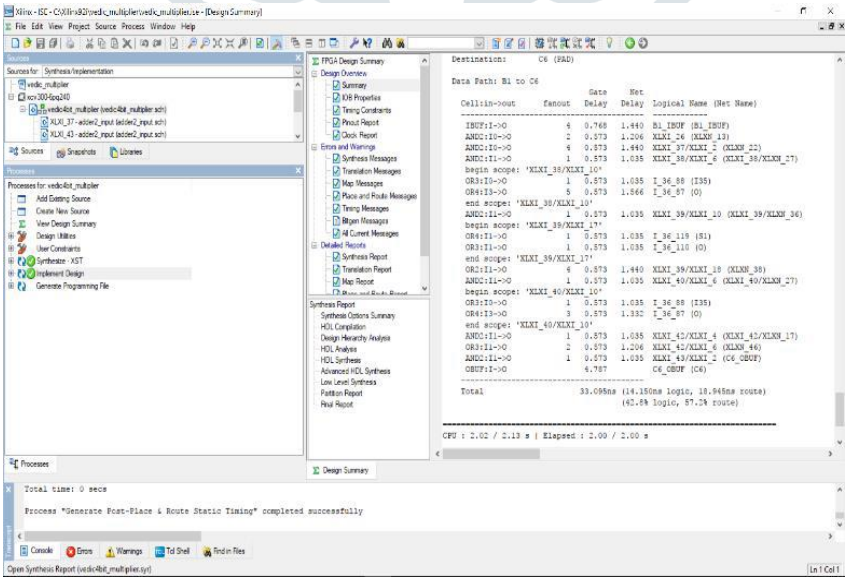

Figure 4:Time Delay Report

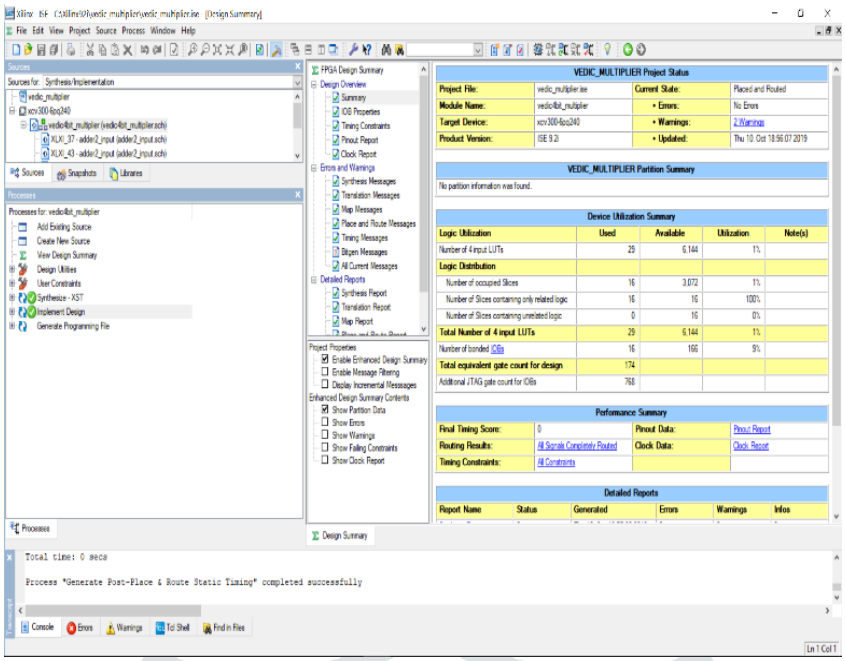


Figure 5:Design Summary

## IV. SYNTHESIS RESULT

| Method | No. of slices out of 3072 | No. of LUTs out of 6144 | Path Delay |
|---|---|---|---|
| Vedic Multiplier | 16 | 29 | 33.095 ns |
| Array Multiplier | 293 | 509 | 88.718 ns |

## V. ADVANTAGES

- Increase the Speed of the system
- To acquire good efficiency of the system
- Reduce the path delay in the multiplier
- Decrease the no. of slices out of 3072
- Decrease the no. of LUT's out of 6144

## VI. CONCLUSION

The number of LUT's for the design of array multiplier is more than that of the vedic multiplier. As number of LUT's is less in the vedic multiplier, so there will be less switching time and thus the power consumption will be less. Also the required area for the implementation is less, since the total equivalent gate count for the design of vedic multiplier is lesser than that of array multiplier as shown above in the design summary. Thus it can be concluded that Vedic Multiplier is superior in all respect like speed, delay, complexity, power.

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