Physical Design Implementation of Volcano SoC with timing closure using 28nm Technology

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ABSTACT

The design-cycle of VLSI-chips consists of different consecutive steps from high-level synthesis (functional design) to production (packaging).This project aims to implement a physical design flow from netlist to gdsii that starts from floorplan, placement, CTS, routing and ends with physical verification. The main objective of this project is to fix the violations those results in the implementation of Volcano SoC such as crosstalk, slew violations, congestion and other signal integrity issues. Results show that the proposed steps eliminate these issues and clear the physical verification checks such as DRC, LVS static and IR and antenna design rule. Further the resultant optimized design meets the timing constraints and minimizes area to obtain a design suitable for manufacture. Here in this design we have used the inputs given by the synthesis team and further physical design flow has been carried out in a proper physical design flow i.e. from import design, floor plan further placement till signoff using the Physical design tools. At each stage checks are done such as timing , quality of report, congestion, routing etc.

Key words- Creating Bounds, Magnet Placement Timing Driven Placement, Congestion Driven Placement , CTS, Congestion, Path grouping.

1. INTRODUCTION

The design-cycle of VLSI-chips consists of different consecutive steps from high-level synthesis (functional design) to production (packaging). The physical design is the process of transforming a circuit description into the physical layout, which describes the position of cells and routes for the interconnections between them. The input of a physical design process is the netlist. The main concern in the physical design of VLSI-chips is to find a layout with minimal area, further the total wire length has to be minimized.

Static timing analysis is a method of validating the timing performance of a design by checking all possible paths for timing violations under worst-case conditions. To check a design for violations, Prime Time breaks the design down into a set of timing paths, calculates the signal propagation delay along each path, and checks for violations of timing constraints. It considers the worst possible delay through each logic element, but not the logical operation of the circuit under test. Static timing analysis checks the design only for proper timing, not for correct logical functionality. In static timing analysis, the word static alludes to the fact that this timing analysis is carried out in an input-independent manner. It locates the worst-case delay of the circuit over all possible input combinations. There are huge numbers of logic paths inside a chip of complex design. It is difficult for EDA tools to complete floorplanning and P&R quickly and accurately, so EDA tools need several constraints for floorplanning. Through multiple iterations and repeated adjustment of floorplaning according to the results of P&R, to finally finish physical design and meet design requirements. Besides, many new algorithms and techniques are applied to VLSI floorplanning, Placement , clock tree synthesis and Routing.

1.1 Design Specifications

Name :Volcano SoC
Technology Node : 28nm
Tools : IC Compiler, Star RC, Prime Time
Instance Count : 50000
Block Dimension : 800x800
Frequency : 450MHz
Clocks : 6 clocks and 2 v_ Clocks
Metal Layer : 9
Hard Macros : 40

1.2 Design Targets

Clock Frequency: 450Mhz. (2.22ns)
Target Skew: 50ps
Max Transition: 100ps
Max Capacitance:50 ff
Max Fan-out:32
Max Insertion Delay: 200ps

2. RELATED WORKS

Buffered clock trees are often desirable, but added at the expense of complicating the clock design. From [1], skew due to buffer mismatch is minimized by first clustering the clock nodes so that identical buffers can be used at a level, and balancing the higher-order loads of the clusters so that load dependent buffer delays are matched. Interconnect delays within clusters are concurrently balanced too, thereby generating a low-skew buffered clock tree design. While the two techniques we have presented are most effective when used concurrently, they are completely independent of each other. The clustering technique can be used to generate clusters of equal capacitive loading for any clock tree synthesis methodology. Similarly, the delay- and admittance-matching wire sizing technique can be used for constructing any buffered clock tree that uses equally-sized buffers at the same level.

Crosstalk is a well–known phenomenon at all levels of electronic packaging from system level cables through wires on printed circuit boards and multi–chip–modules to chip level routing. It is an effect due to coupling capacitances and inductances between currents in electrical conductors. Crosstalk causes undesired signal noise to be coupled from an active line (aggressor) into a quiet line (victim). Depending on its magnitude, the induced noise onto the victim may influence the timing behaviour of the victim signal by increasing its setup time by

[2]. It may even cause failure by inducing false pulses or causing false signal levels which may be propagated through the circuit. With increasing integration density and reduced cycle times, these effects become more visible and more destructive, so they need to be handled more carefully. Crosstalk needs to be considered in particular on VLSI chips with sub–micron structures and today's large die sizes.

[3]. As crosstalk is strictly a local phenomenon it is handled within detailed routing (local routing) rather than in global routing. The final arrangement of all wire segments is determined within detailed routing, where the crosstalk relevant parameters can be extracted. Moreover, the detailed router usually has sufficient freedom for the assignment of wire segments to channels to avoid the most critical coupling configurations.

However, detailed routing is typically one of the most CPU time and memory intensive tasks in physical chip design. Therefore, the detailed router is guided by simple geometrical restrictions for crosstalk avoidance rather than by a complete complex electrical wire model.

3. PROPOSED SYSTEM

This project aims to implement a physical design flow from netlist to gdsii that starts from floorplan, placement, CTS, routing and ends with physical verification. The main objective of this project is to fix the violations those results in the implementation of Volcano SoC such as timing, crosstalk, slew violations, congestion and other signal integrity issues using various techniques such as Creating Bounds, Magnet Placement Applying Blockages Timing Driven Placement Congestion Driven Placement . Path Grouping, Upsizing and Downsizing, Inserting Buffers
Assigning Cock Tress Exceptions Controlling spread of logic

Results show that the proposed steps eliminate these issues and clear the physical verification checks such as DRC, LVC and antenna design rule to obtain a design that is suitable for manufacture. The main focus of this work is to achieve a good floorplan, to get timing clean, congestion free placement, maximum skew and insertion delay targets during CTS, timing fixes and to get a DRC clean, LVS clean design, fixing antenna violations, dynamic and static IR violations.

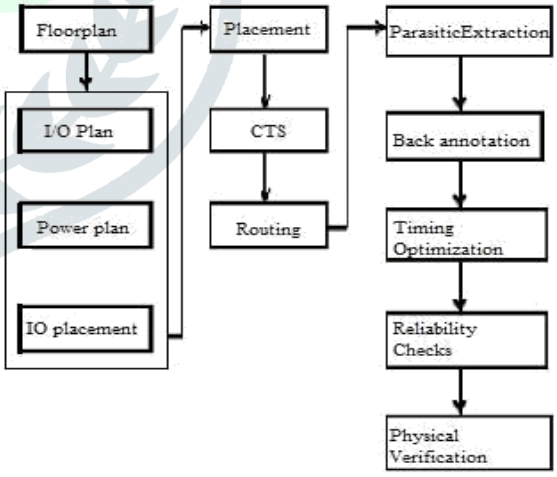

Fig.1 Physical design flow of Volcano SoC

3.1 Inputs Required for Volcano Design

Inputs Required Are Gate level netlist, Logical (Timing) & Physical views of standard cells & all other IPs used in the design, Timing constraints (SDC), Power Intent (UPF / CPF), FP DEF & Scan DEF, Technology file & RC Co-efficient files.

3.2 Key checks to Qualify Import Design

Here Checks of errors and warning have been done while reading netlist, timing constraints, UPF/CPF, black boxes, MV design (equivalent to LP checks) and assign & tri statements (Usually its checked & fixed after Synthesis)

3.3 Sanity Checks

Sanity checks essentially check the condition of netlist in terminology of timing , it also consists of read-through the issues allied to library files, timing constraints, IOs and optimization directives. Sanity checks which have been performed are as

[1]

library checks: to check the missing cell information, missing pin information & if any Duplicate cells present or not.

[2]

design checks: to check the Inputs with floating pins, nets with tristate drivers, nets with multiple drivers, Combinational loops, Empty modules, Assign statements

[3]

constraint checks: to check all flops are clocked or not, unconstraint paths should not be present & Input and output delays.

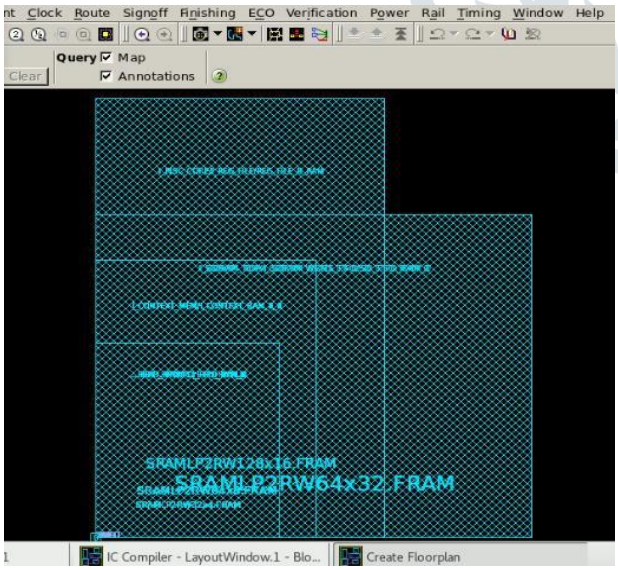

Fig -2: Imported Design

4. FLOORPLAN

This is the first major step in getting the layout done. Here floor plan determines your chip quality. At this step, we define the size of your chip/block, allocates power routing resources, place the hard macros, and reserve space for standard cells. A Satisfactory floorplan can make implementation method (place, CTS, route & timing closure) cake walk. On similar lines a bad floorplan can create all kind issues in the design (congestion, timing, noise, IR, routing issues). A bad floorplan will propel up the area, power & affects reliability, life of the IC and also it can increase overall IC cost (more effort to closure, more LVTs/ULVTs)

4.1 Deciding the Utilization factor & Aspect ratio

a. Utilization factor decides the size of the block meaning suppose out of 100 percent we give utilization factor of 70 percent it means 70 percent will be used for placing macros and instances in the design and remaining 30 percent will be used for routing purpose to connect all the macros and instances in the design

b. Aspect ratio gives shape of the block i.e. width/height example: say height of 1.4 and width of 1.0 is given henceit will form a rectangle shape design

c. After utilization and aspect ratio we go for pin placement. In pin placement we have to place pins legally

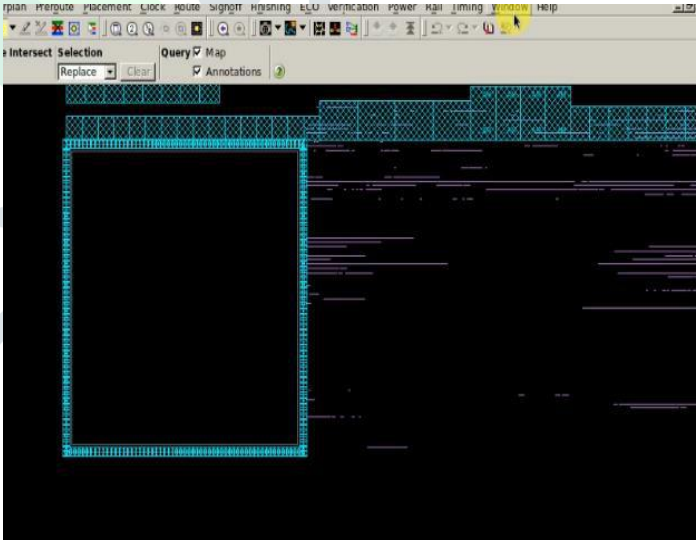

Fig -3 Created floorplan with aspect ratio and utilization factor

4.2 Macros Placement

Method to place macros which have been followed in this design as follows**.**

4.2.1 place macros around chip periphery. If you don't have reasonable rationale to place the macro inside the core area, then place macros around the chip periphery. Placing a macro inside the core can invite serious consequence during routing due to a lot of detour routing, because macros are equal to a large obstacle for routing. Another advantage to placing the hard macros around the core periphery is it's easier to supply power to them, and reduces the change of IR drop problems to macros consuming high amounts of power.

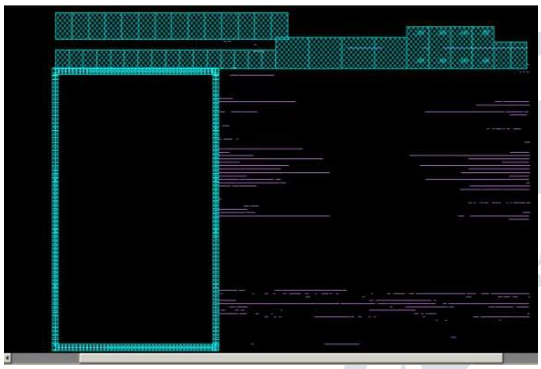

Fig -4: Before macro placement

4.2.2 Consider connections to fixed cells when placing macros. When you decide macro position, you have to pay attention to connections to fixed elements such as I/O and preplaced macros. Place macros near their associate fixed element. Check connections by displaying flight lines in the GUI.

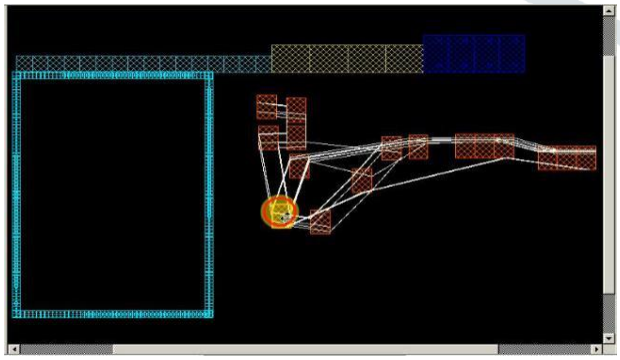

Fig -5: Fly line analysis

4.2.3 Orient macros to minimize distance between pins. When you decide the orientation of macros, you also have to take account of pins positions and their connections.

4.2.4 Reserve enough room around macros. For regular net routing and power grid, you have to reserve enough routing space around macros. In this case estimating routing resources with precision is very important. Use the congestion map from trial Route to identify hot spots between macros and adjust their placement as needed. The space between macros is given by equation

4.2.5 Reduce open fields as much as possible. Except for reserved routing resources, remove dead space to increase the area for random logic. Choosing different aspect ratio (if that option is available) can eliminate open fields.

4.2.6 Reserve space for power grid. The number of power routes required can change based on power consumption. You have to estimate the power consumption and reserve enough room for the power grid. If you underestimate the space required for power routing, you can encounter routing problems 5. After macro placement we will place physical cells like endcap and well tap cells

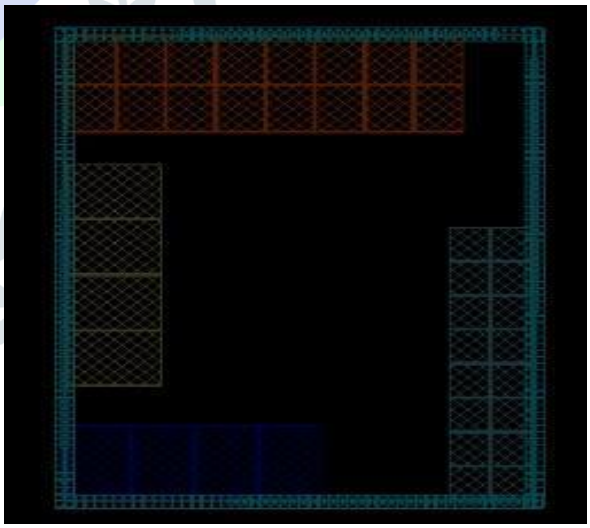

Fig -6: Macros Placed

Further after placing the macro we have added keep out margin to macros, physical cells and cut rows in the design.

PLACEMENT

Before the start of placement optimization all WLM are removed. Placement uses RC values from VR to calculate timing. VR is the shortest Manhattan distance between two pins. Pre-placement Optimization optimizes the netlist before placement, HFNs are collapsed. It can also downsize the cells. In-placement optimization re-optimizes the logic based on VR. This can perform cell sizing, cell moving, cell bypassing, net splitting, gate duplication, buffer insertion, area recovery. Optimization performs iteration of setup fixing, incremental timing and congestion driven placement. Post placement optimization before CTS performs netlist optimization with ideal clocks. It can fix setup, max trans/cap violations. It can do placement optimization based on global routing. It re does HFN synthesis. Post placement optimization after CTS optimizes timing with propagated clock. It tries to preserve clock skew. Objectives of placement includes minimize the all critical net delay, minimize the total estimated interconnect length and minimize the interconnect congestion. Placement is the process of placing standard cells in the rows created at Floorplanning stage. The goal is to decrease the total area and interconnects cost. The trait of routing is highly determined by the placement.

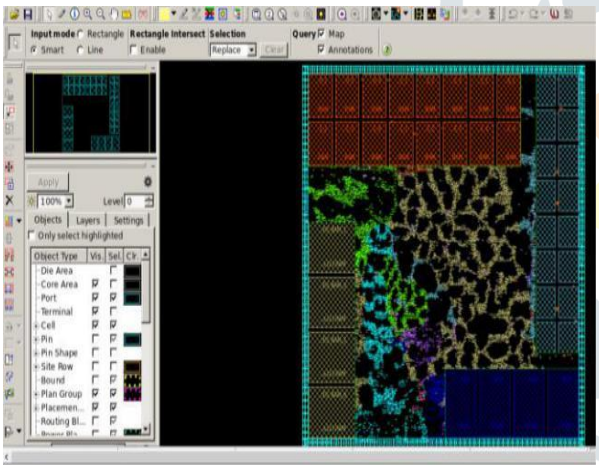

Fig -7: Standard cells placed in the core area

One way to overcome the complication concern is to perform placement in several controllable steps as discussed below.

Global Placement: Global placement aims at generating a coarse placement solution that may violate some placement constrains (e.g., there may be overlaps among modules) while maintaining a global view of whole netlist. here the Objective is to lessen the interconnect wire lengths.

Legalization: Legalization makes the rough solution from global placement legal

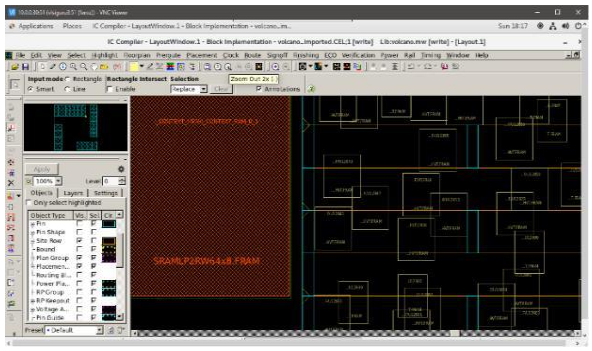

Fig -8: coarse placement of standard cell in the design

Detailed Placement: Detailed placement further improves the legalized placement solution in an iterative method by rearranging a small group of modules in a local region while keeping all other modules fixed. Here the Objective is to meet design constraints such as Timing/Congestion and to conclude standard cell placement

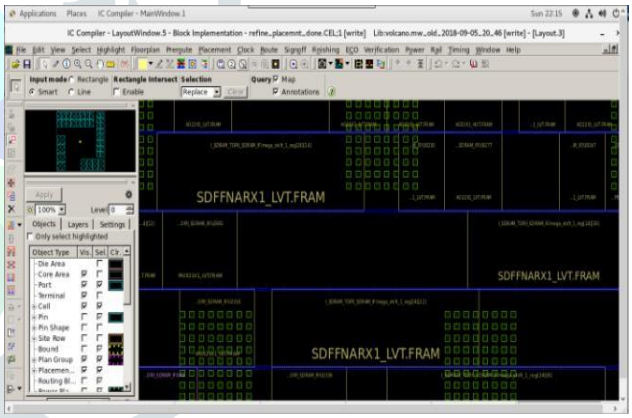

Fig -9: Detailed and legalized placement of standard ell

6. CLOCK TREE SYNTHESIS

The goal of CTS is to minimize skew and insertion delay. Clock is not propagated before CTS .After CTS hold slack should improve. Clock tree begins at .sdc defined clock source and ends at stop pins of flop. There are two types of stop pins known as ignore pins and sync pins. Don't touch" circuits and pins in front end (logic synthesis) are treated as „ignore" circuits or pins at back end (physical synthesis). „Ignore" pins are ignored for timing analysis. If clock is divided then separate skew analysis is necessary. First is global skew achieves zero skew between two synchronous pins without considering logic relationship. Second one is local skew achieves zero skew between two synchronous pins while considering logic relationship. If clock is skewed intentionally to improve setup slack then it is known as useful skew.

In CTO clock can be shielded so that noise is not coupled to other signals. But shielding increases area by 12 to 15%. Since the clock signal is global in nature the same metal layer used for power routing is used for clock also. CTO is achieved by buffer sizing, gate sizing, buffer relocation, level adjustment and HFN synthesis. We try to improve setup slack in pre-placement, in placement and post placement optimization before CTS stages while neglecting hold slack. In post placement optimization after CTS hold slack is improved. As a result of CTS lot of buffers are added. Generally for 100k gates around 650 buffers are added

7. ROUTING

After placement, the routing process determines the precise paths for nets on the chip layout to interconnect the pins on the circuit blocks or pads at the chip boundary. These precise paths of nets must satisfy the design rules provided by chip foundries to ensure that the designs can be correctly manufactured. The most important objective of routing is to complete all the required connections. The routing step adds wires needed to properly connect the placed components while obeying all design rules for the IC.This stage involves routing of nets connecting different standard cells through different metal layers. There are two types of routing in the physical design process namely global and detailed routing. Global routing -is used to provide instructions to the detailed router about where to route every net. It provides channels for interconnect to be routed. Global routing allocates routing resources that are used for connections. Global routing first partitions the routing region into tiles and decides tile-to-tile paths for all nets while attempting to optimize some given objective function. Detailed routing -is where we specify exact location of the wires/interconnects in the channels specified by the global routing. Metal layer information of the interconnect are also specified here. Detailed routing assigns routes to specific metal layers and routing tracks within the global routing resources. The primary goal of detailed routing is to complete all of the required interconnect without leaving shorts or spacing violations.

Objectives of routing are, reducing the routing wire length and ensuring each net to satisfy its required timing budget, have become essential for modern chip design. In detail routing router runs search and repair routing here it locates shorts and opens and spacing violations so, it reroutes the affected area to eliminate violations. As the fixes are done and timings are met this procedure nothing but called as engineering change order(ECO) hence we conclude the physical design flow by handing the GDS II file to the further ASIC flow stage.

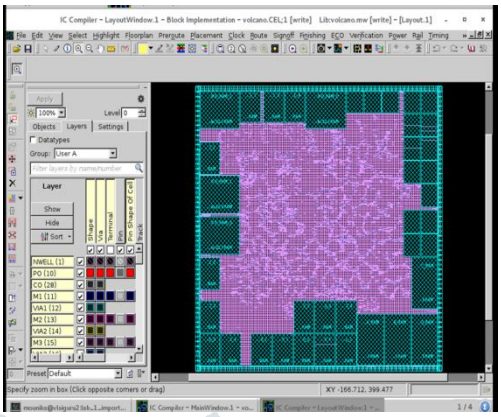

Fig -10: Routed Design

7.1 Physical verification

Physical verification checks the correctness of the generated layout design. The major checks performed here are DRC,LVS ,antenna rule checking,EM and IR analysis.

DRC- checks determine if the layout satisfies a set of rules required for manufacturing. The most common of these are spacing rules between metals, minimum width rules, via rules etc. There will also be specific rules pertaining to the technology. An input to the design rule tool is a „design rule file". LVS- is another major check in the physical verification stage. Here the layout created is verified such that it is functionally the same as the schematic/netlist of the design- that have correctly transferred into geometries your intent while creating the
design.

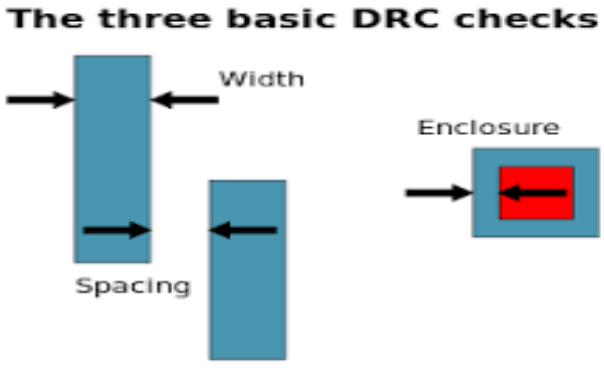

Fig.11 Basic Design Rule Check like spacing width.

8.RESULTS

Placement Congestion Map Results

```
Average horizontal track utilization = 25.80 %
Peak    horizontal track utilization = 233.33 %

Current Stage stats:
[GR: Done] Elapsed real time: 0:00:00
[GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[GR: Done] Stage (MB): Used  -17  Allоctr  -17  Proc    0
[GR: Done] Total (MB): Used  169  Allоctr  179  Proc 2560
GR Total stats:
[GR: Done] Elapsed real time: 0:01:11
[GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:01:11 total=0:01:11
[GR: Done] Stage (MB): Used  159  Allоctr  169  Proc    0
[GR: Done] Total (MB): Used  169  Allоctr  179  Proc 2560
Writing out congestion map...
Updating congestion ...
[DBOUT] Elapsed real time: 0:00:01
[DBOUT] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:01
[DBOUT] Stage (MB): Used -137  Allоctr -147  Proc    0
[DBOUT] Total (MB): Used   11  Allоctr   13  Proc 2560
Final total stats:
[End of Global Routing] Elapsed real time: 0:01:12
[End of Global Routing] Elapsed cpu  time: sys=0:00:00 usr=0:01:11 total=0:01:12
[End of Global Routing] Stage (MB): Used    2  Allоctr    2  Proc    0
[End of Global Routing] Total (MB): Used   11  Allоctr   13  Proc 2560

Information: Reporting global route congestion data from Milkyway...

Both Dirs: Overflow = 3267 Max = 26 (1 GRCs) GRCs = 1140 (0.25%)
H routing: Overflow = 1723 Max = 12 (1 GRCs) GRCs = 668  (0.15%)
V routing: Overflow = 1544 Max = 26 (1 GRCs) GRCs = 472  (0.10%)

1
icc_shell>
```

Fig.12 Congestion Report 1

```
verage horizontal track utilization = 25.73 %
eak    horizontal track utilization = 216.67 %

urrent Stage stats:
GR: Done] Elapsed real time: 0:00:00
GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
GR: Done] Stage (MB): Used  -17  Allоctr  -17  Proc    0
GR: Done] Total (MB): Used  171  Allоctr  182  Proc 2565
R Total stats:
GR: Done] Elapsed real time: 0:01:14
GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:01:14 total=0:01:14
GR: Done] Stage (MB): Used  159  Allоctr  168  Proc    5
GR: Done] Total (MB): Used  171  Allоctr  182  Proc 2565
riting out congestion map...
pdating congestion ...
DBOUT] Elapsed real time: 0:00:01
DBOUT] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:01
DBOUT] Stage (MB): Used -137  Allоctr -147  Proc    0
DBOUT] Total (MB): Used   14  Allоctr   15  Proc 2565
inal total stats:
End of Global Routing] Elapsed real time: 0:01:15
End of Global Routing] Elapsed cpu  time: sys=0:00:00 usr=0:01:15 total=0:01:15
End of Global Routing] Stage (MB): Used    2  Allоctr    2  Proc    5
End of Global Routing] Total (MB): Used   14  Allоctr   15  Proc 2565

nformation: Reporting global route congestion data from Milkyway...

oth Dirs: Overflow = 3343 Max = 26 (1 GRCs) GRCs = 1117 (0.24%)
 routing: Overflow = 1640 Max = 13 (7 GRCs) GRCs = 636  (0.14%)
routing: Overflow = 1703 Max = 26 (1 GRCs) GRCs = 481  (0.11%)
```

Fig.13 Congestion Report 2

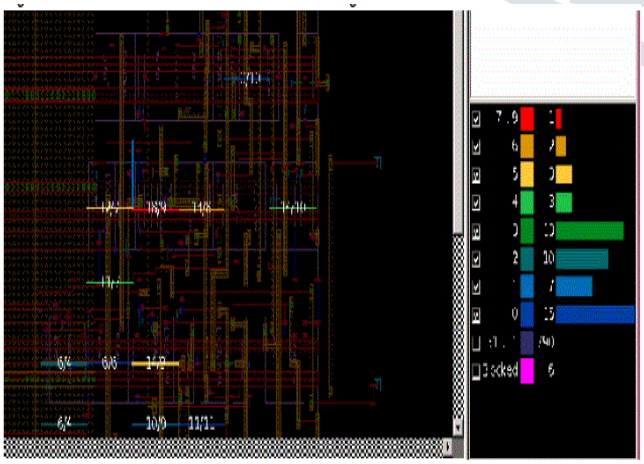

Fig.14 Congestion Report 3 in GUI

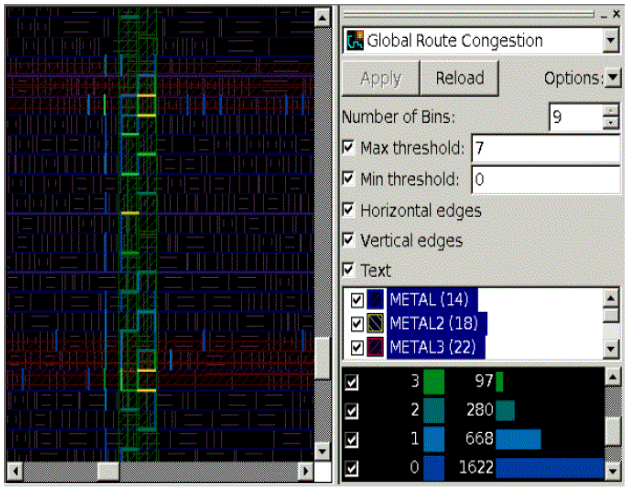

Fig.15 Congestion Report 4 in GUI after fixing the Congestion

Timing Results

```
Startpoint: I_PCI_TOP/R_687
            (rising edge-triggered flip-flop clocked by PCI_CLK)
Endpoint: pack_n (output port clocked by v_PCI_CLK)
Path Group: v_PCI_CLK
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock PCI_CLK (rise edge)                0.00       0.00
clock network delay (ideal)              0.00       0.00
I_PCI_TOP/R_687/CLK (SDFFASX1_LVT)       0.00       0.00 r
I_PCI_TOP/R_687/Q (SDFFASX1_LVT)         0.17       0.17 r
I_PCI_TOP/U1032/Y (NAND3X0_HVT)          0.29 *     0.46 f
I_PCI_TOP/U98/Y (DELLN3X2_HVT)           0.93 *     1.39 f
I_PCI_TOP/U645/Y (AND2X2_HVT)            0.15 *     1.54 f
I_PCI_TOP/pack_n (PCI_TOP)               0.00       1.54 f
io_buff_161_0/Y (NBUFFX4_RVT)            0.08 *     1.62 f
U780/Y (INVX0_HVT)                       0.10 *     1.71 r
U781/Y (IBUFFX2_HVT)                     0.12 *     1.84 f
U782/Y (DELLN3X2_HVT)                    0.76 *     2.60 f
U17/Y (NBUFFX32_HVT)                     0.10 *     2.71 f
pack_n (out)                             0.03 *     2.74 f
data arrival time                                   2.74

clock v_PCI_CLK (rise edge)              7.50       7.50
clock network delay (ideal)              0.50       8.00
output external delay                   -3.00       5.00
data required time                                  5.00
-----------------------------------------------------------
data required time                                  5.00
data arrival time                                  -2.74
-----------------------------------------------------------
slack (MET)                                         2.26
```

Fig.16 Timing Report of Clock 1

```
Startpoint: I_PCI_TOP/R_3
            (rising edge-triggered flip-flop clocked by PCI_CLK)
Endpoint: ppar_en (output port clocked by v_PCI_CLK)
Path Group: v_PCI_CLK
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock PCI_CLK (rise edge)                0.00       0.00
clock network delay (ideal)              0.00       0.00
I_PCI_TOP/R_3/CLK (SDFFASX1_LVT)         0.00       0.00 r
I_PCI_TOP/R_3/Q (SDFFASX1_LVT)           0.17       0.17 f
I_PCI_TOP/U694/Y (NAND2X0_HVT)           0.08 *     0.25 r
I_PCI_TOP/ppar_en (PCI_TOP)              0.00       0.25 r
U631/Y (NBUFFX4_HVT)                     0.14 *     0.39 r
U404/Y (NBUFFX32_HVT)                    0.13 *     0.51 r
U747/Y (DELLN3X2_HVT)                    0.69 *     1.20 r
io_buff_176_0/Y (NBUFFX4_RVT)            0.08 *     1.28 r
U746/Y (NBUFFX2_HVT)                     0.08 *     1.36 r
U16/Y (NBUFFX32_HVT)                     0.10 *     1.46 r
ppar_en (out)                            0.04 *     1.50 r
data arrival time                                   1.50

clock v_PCI_CLK (rise edge)              0.00       0.00
clock network delay (ideal)              0.50       0.50
output external delay                    1.00       1.50
data required time                                  1.50
-----------------------------------------------------------
data required time                                  1.50
data arrival time                                  -1.50
-----------------------------------------------------------
slack (MET)                                         0.00
```

Fig.16 Timing Report of Clock 2

QoR:Quality of Results

```
Timing Path Group 'PCI_CLK'
-----------------------------------
Levels of Logic:                11.00
Critical Path Length:            1.31
Critical Path Slack:             1.47
Critical Path Clk Period:        7.50
Total Negative Slack:            0.00
No. of Violating Paths:          0.00
Worst Hold Violation:            0.00
Total Hold Violation:            0.00
No. of Hold Violations:          0.00
-----------------------------------

Timing Path Group 'SDRAM_CLK'
-----------------------------------
Levels of Logic:                 2.00
Critical Path Length:            0.39
Critical Path Slack:             0.70
Critical Path Clk Period:        4.10
Total Negative Slack:            0.00
No. of Violating Paths:          0.00
Worst Hold Violation:            0.00
Total Hold Violation:            0.00
No. of Hold Violations:          0.00
```

Fig.17 QoR of Generated Clock 3&4

```
-----------------------------------

Timing Path Group 'SDRAM_CLK'
-----------------------------------
Levels of Logic:                 2.00
Critical Path Length:            0.39
Critical Path Slack:             0.70
Critical Path Clk Period:        4.10
Total Negative Slack:            0.00
No. of Violating Paths:          0.00
Worst Hold Violation:            0.00
Total Hold Violation:            0.00
No. of Hold Violations:          0.00
-----------------------------------

Timing Path Group 'SD_DDR_CLK'
-----------------------------------
Levels of Logic:                 7.00
Critical Path Length:            0.95
Critical Path Slack:             0.25
Critical Path Clk Period:        4.10
Total Negative Slack:            0.00
No. of Violating Paths:          0.00
Worst Hold Violation:            0.00
Total Hold Violation:            0.00
No. of Hold Violations:          0.00
-----------------------------------
```

Fig.18 QoR of Generated Clock 4&5

```
Timing Path Group 'SYS_2x_CLK'
-----------------------------------
Levels of Logic:                21.00
Critical Path Length:            2.09
Critical Path Slack:             0.00
Critical Path Clk Period:        2.40
Total Negative Slack:            0.00
No. of Violating Paths:          0.00
Worst Hold Violation:            0.00
Total Hold Violation:            0.00
No. of Hold Violations:          0.00
-----------------------------------

Timing Path Group 'SYS_CLK'
-----------------------------------
Levels of Logic:                33.00
Critical Path Length:            3.96
Critical Path Slack:             0.55
Critical Path Clk Period:        4.80
Total Negative Slack:            0.00
No. of Violating Paths:          0.00
Worst Hold Violation:            0.00
Total Hold Violation:            0.00
No. of Hold Violations:          0.00
-----------------------------------
```

Fig.19 QoR of Generated Clock 6& Clock 7

```
Timing Path Group 'v_PCI_CLK'
-----------------------------------
Levels of Logic:                 7.00
Critical Path Length:            2.97
Critical Path Slack:             2.03
Critical Path Clk Period:        7.50
Total Negative Slack:            0.00
No. of Violating Paths:          0.00
Worst Hold Violation:            0.00
Total Hold Violation:            0.00
No. of Hold Violations:          0.00
-----------------------------------


Cell Count
-----------------------------------
Hierarchical Cell Count:            54
Hierarchical Port Count:          2166
Leaf Cell Count:                 51117
Buf/Inv Cell Count:               5524
Buf Cell Count:                   2989
Inv Cell Count:                   2535
CT Buf/Inv Cell Count:              18
Combinational Cell Count:        45690
Sequential Cell Count:            5427
Macro Count:                        40
-----------------------------------


Area
-----------------------------------
```

Fig.20 QoR of Clock 8 and Design Cell Count

```
-----------------------------------


Area
-----------------------------------
Combinational Area:   125454.120318
Noncombinational Area: 49330.876110
Buf/Inv Area:          14847.092638
Total Buffer Area:         10987.41
Total Inverter Area:        3859.68
Macro/Black Box Area: 264884.269531
Net Area:             147026.850730
Net XLength        :      700782.44
Net YLength        :      746797.44
-----------------------------------
Cell Area:            439669.265958
Design Area:          586696.116688
Net Length         :     1447579.88
```

Fig.21 Design Area Report

```
Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = -20.6607 mW  (114%)
  Net Switching Power  =   2.4946 mW  (-13%)
                         ---------
Total Dynamic Power    = -18.1662 mW  (100%)

Cell Leakage Power     =  22.8741 mW


                 Internal         Switching          Leakage            Total
Power Group      Power            Power              Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000             0.0000             0.0000  (   0.00%)
memory         -2.3438e+04           93.2679             0.0000         -2.3345e+04
                                                                                 ( -495.87%)
black_box          0.0000           0.0000             0.0000             0.0000  (   0.00%)
clock_network     80.2587          880.5476         7.9146e+07         1.0400e+03  (  22.09%)
register       1.7155e+03           97.1046         6.8944e+09         8.7071e+03  ( 184.94%)
sequential         0.3920         7.4480e-04         5.5586e+05             0.9486  (   0.02%)
combinational    981.4607         1.4236e+03         1.5900e+10         1.8305e+04  ( 388.81%)
--------------------------------------------------------------------------------------------------
Total          -2.0661e+04 uW     2.4946e+03 uW      2.2874e+10 pW      4.7080e+03 uW
1
icc_shell>
```

Fig.21 Design Power Report

9. CONCLUSION

The physical design flow of a Volcano SoC from netlist to gdsii that starts from floorplan, placement, CTS, routing and ends with physical verification was implemented. The violations those resulted in the implementation of Volcano SoC such as crosstalk, slew violations, congestion and other signal integrity issues are fixed by inserting additional buffers as well as using double width double spacing rule. For this implementation Synopsys IC Compiler tool is used. Results show that the implemented design clears thephysical verification checks such as DRC, LVS and antenna design rule to obtain a design that is suitable for manufacturing.

REFERENCES

1. R. Chaturvedi and J. Hu, "Buffered clock tree for high quality IC design," in Proc. Int. Symp. Qual. Electron. Des., 2004, pp. 381–386.

2. Tilmann stohr, Markus Alt, Asmus Hetzel, Jergen Koehl. „Avoidance, reduction and analysis of crosstalk on VLSI chips", IBM Entwicklung GmbH, Sch¨onaicher Straße 220, 71032 B¨oblingen, Germany.

3. Youngsoo shin and Jun seomunkaistkyu-myung choi Samsung Electronics and takayasu sakurai, „Power Gating: Circuits, Design Methodologies, and Best Practice for Standard-Cell VLSI Designs" University of Tokyo.

4. "Signal electro-migration analysis and fixing research in IC Compiler." http://www.synopsys.com.cn/information/snug/2011/signal-electro-migration-analysis-and-fixing-research-in-ic-compiler-2

5."Understand and avoid electromigration (EM) & IR-drop in custom IP blocks." http://www.synopsys.com/Tools/Verification/Cap