Comparative Study of Different Types of Shift Register Based on Reversible Logic Gate

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Abstract-
This paper review of Bit Linear Feedback Shift Register which generates pseudo-random test patterns as the input bit is a linear function of its previous state. The total number of random state generated on LFSR depends on the feedback polynomial. As it is simple counter so it can count maximum of 2n -1 by using maximum feedback polynomial. Here in this paper we study of 16-bit different types of shift register on FPGA by using VHDL and analysis the behaviour of randomness. The analysis is conceded out to find number of gates, memory and speed requirement in FPGA as the number of bits is increased. Also, the simulation problem for long bit LFSR on FPGA is presented. The design is simulated and synthesized in Xilinx software.

Keywords—Serial in Serial Output (SISO), Serial in Parallel out, Parallel in Serial out, Parallel in Parallel Out

I. INTRODUCTION

A linear feedback shift register is a combination of series of flip flop and XOR or XNOR logic gates. Its output is pseudo randomly cycle through a sequence of binary values after certain number of clock cycle [1]. The repetition of random output depends on the number of stages in the LFSR. Therefore, it is an important component in communication system where, it play important role in various application such as cryptography application, CRC generator and checker circuit, gold code generator, for generation of pseudorandom sequence, for designing encoder and decoder in different communication channels to ensure network security, Design for Test (DFT) and Built in Self-Test design (BIST).
A linear feedback shift register is linear in the sense that its input bit is a linear function (XORing or XNORing) of LFSR previous state [2].
The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation for VLSI circuits. The power dissipation during the test mode is 200% more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges. Linear feedback shift registers have multiple uses in digital systems design. Here we have implemented a 32 bit length sequence on FPGA using VHDL with maximum length feedback polynomial to understand the memory utilization and speed requirement. Also, we have presented the comparison of performance analysis based on synthesis and simulation result as well identify the simulation problem for long bit LFSR. The target device we have used Xilinx Spartan 3A and performed simulation and synthesis using Xilinx ISE. The HDLs are VHDL and Verilog. We prefer VHDL for programming because it is widely used.

II. REVERSIBLE GATE

Reversible justification is getting hugeness in zones of CMOS setup by virtue of its low control spread. The standard gateways like AND, OR, XOR are for the most part irreversible entryways. Think about the occurrence of regular AND passage. It includes two sources of info and one yield. Along these lines, one piece is lost each time a computation is finished Hence it is unfeasible to choose a momentous data that achieved the yield zero. With a particular ultimate objective to make a gateway reversible additional data and yield lines are included so an organized mapping exists between the information and yield. This keeps the loss of information that is major driver of power dispersal in irreversible circuits. The data that is added to a m x n ability to make it reversible is known as relentless data (CI). All of the yields of a reversible circuit need not be used as a piece of the circuit. Those yields that are not used as a piece of the circuit is called as garbage yield (GO). The amount of waste yield for a particular reversible entryway isn't adjusted. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

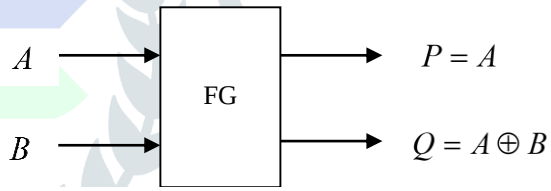

Figure 1: Feynman gate

In figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

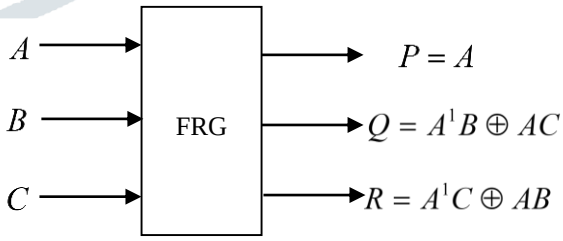

Figure 2: Fredkin gate

Figure 3 demonstrates the Peres door. A segment of the 4x4 entryways are proposed for executing some basic combinational limits not with standing the major limits. Most by far of the previously mentioned doors can be used as a piece of the layout of reversible adders.

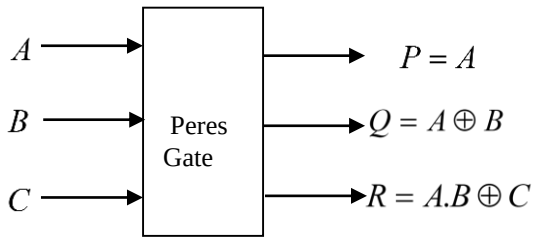

Figure 3: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \tag{1}$$

$$Q = B \tag{2}$$

$$R = A \oplus B \oplus C \tag{3}$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \tag{4}$$

The quantum cost and postponement of the HNG is 6. Right when D = 0, the predictable estimations made on the R and S yields are the required aggregate and complete activities for a full snake. The quantum portrayal of the HNG is shown in Fig. 4.

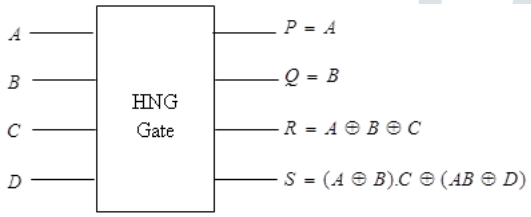

Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PAOG) gate – is presented which produces outputs

$$P = A \tag{5}$$

$$Q = A \oplus B \tag{6}$$

$$R = AB \oplus C \tag{7}$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \tag{8}$$

Fig. 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

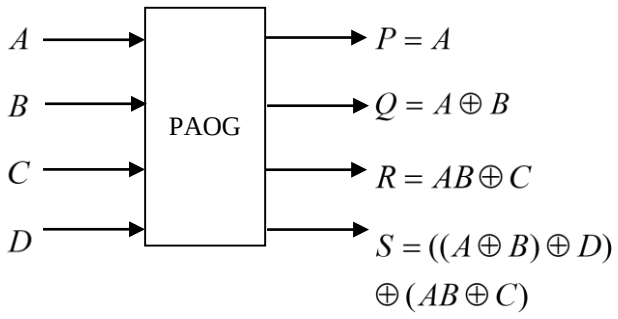

Figure 5: Block Diagram of the PAOG

A few 4x4 doors have been depicted in the writing focusing on minimal effort and postpone which might be executed in a programmable way to create a high number of sensible computations. The DKG door creates the accompanying coherent yield computations:

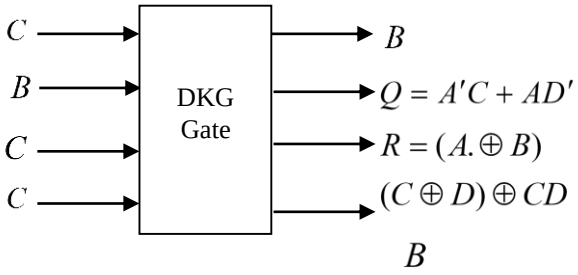

Figure 6: DKG Gate

$$P = B \tag{9}$$

$$Q = A'C + AD' \tag{10}$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \tag{11}$$

$$S = B \oplus C \oplus D \tag{12}$$

III. LITRATURE REVIEW

Partho Ghose [1], reversible logic is an emerging technology that plays an important role in the fields of low power computation and can be applied in cryptography, communications, quantum computing etc. Reversible shift registers are one of the most important elements in fabricating reversible memory circuits. In this paper, we present efficient design of different reversible shift registers such as Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out and Parallel In Parallel Out registers. We have also outlined appropriate lemmas to illustrate different properties of the proposed designs. Suitable algorithms for designing the reversible shift registers are also mentioned. Comparative analysis reveals that our proposed design requires minimal number of reversible gates and constant inputs, and also produces less number of garbage outputs than the state-of-theart design. Furthermore, to clarify the validity of our design, all the proposed circuits have been simulated using DSCH3.

Rajeshwari et al. [2], One of the most potential technologies for low-power VLSI is reversible computing and it has enormous applications has found in low-power CMOS, Quantum computing, Nanotechnology, QCA. The main condition of reversibility is every individual input and outputs are connected internally. In this paper, we proposed optimized reversible design of linear feedback shift registers (LFSR) while designing the LFSR, we have designed optimized Serial input serial output (SISO), Serial input parallel output(SIPO) up to N-bit with reversible gates and it has explored in terms of delay, quantum cost, garbage outputs. Complete simulation and the synthesis process are carried out with the Xilinx ISE 14.7 and are dumped on FPGA Spartan-6E.

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Mishra Shivshankar et al. [4], this paper focus on the implementation of configurable linear feedback shift register (CLFSR) in VHDL and evaluate its performance with respect to logic, speed and memory requirement in FPGA. Behavioral implementation of CLFSR in VHDL is configurable in terms of number of bits in the LFSR, the number of taps; positions of each tap in the shift register stage and seed value of LFSR. The target device used for implementation of CLFSR is Xilinx Virtex-4 FPGA. For simulation and synthesis of CLFSR Xilinx ISE 9.2i tool is used. The output waveforms and timing report are also discussed.

Sharma Radhika et al. [5], in chip manufacturing technology, reduction in chip size possess great concern for power dissipation. Low power testing has become an important issue as power dissipation during testing mode is very high as compare to normal mode. LFSR is used in testing of ASIC chips by generating pseudo random patterns. This paper deals with design of low power LFSR by using GDI technique. GDI technique is one of the low power technique used for implementing various digital circuits.
This technique uses only two transistors to design fast and low power circuits with improvement in power characteristics. LFSR has been implemented by conventional and GDI technique in Cadence Virtuoso at 90nm technology. Comparative analysis is carried out between the two methods showing up to 45.4 % and 20 % reduction in power and area respectively in GDI technique. Simulation and variation of power with frequency and voltage is also discussed.
Hathwalia Shruti et al. [6], this paper proposes a 32 Bit Linear Feedback Shift Register which generates pseudo-random test patterns as the input bit is a linear function of its previous state. The total number of random state generated on LFSR depends on the feedback polynomial. As it is simple counter so it can count maximum of 2n -1 by using maximum feedback polynomial. Here in this paper we implemented 32-bit LFSR on FPGA by using VHDL to study the performance and analysis the behaviour of randomness. The analysis is conceded out to find number of gates, memory and speed requirement in FPGA as the number of bits is increased. Also, the simulation problem for long bit LFSR on FPGA is presented. The design is simulated and synthesized in Xilinx 14.5 ISE and Model Sim 10.1b.

Table 1: Summary of Literature Review

Ref. No.	Title, year of publication	Author Name	Methodology Used	Software	Result
1.	Design of Reversible Shift Registers Minimizing Number of Gates, Constant Inputs and Garbage Outputs, IEEE 2018	Partho Ghose and Md Naimur Rahman	Design 8-bit and 16-bit SISO, SIPO, PISO and PIPO shift register	Xilinx 14.1i	Slice flip flop= 13 IOBs = 10, LUTs = 3, MCPD = 2.363 ns
2.	Design and Implementation of 8 Bit Shift Register using Reversible Logic, IEEE 2018	Rajeshwari. M, Rohini. S. Hongal and Rajashekar B. Shettar	Design 8-bit right and left shift register using reversible logic gate	Xilinx 14.1i	QC = 96, Delay = 6.76 ns, Logic gate
3.	FPGA Implementation of optimized Reversible Linear Feedback Shift Registers, IEEE 2018	K. Rajesh and G. Umamaheswara Reddy	Design linear feedback SISO and SIPO shift register using reversible gate	Xilinx 14.1	QC = 38, Delay = 38 ns, GO = 7
4.	Implementation of Configurable Linear Feedback Shift Register in VHDL, IEEE 2017	Shivshankar Mishra, Ram Racksha Tripathi and Devendra Kr. Tripathi	Design 8-bit and 16-bit linear feedback shift register	Xilinx 14.1i	Slice flip flop= 18 IOBs = 14, LUTs = 7, MCPD = 2.881 ns
5.	Design and Analysis of Linear Feedback Shift Register (LFSR) using Gate Diffusion Input(GDI) Technique, IEEE 2016	Radhika Sharma and Balwinder Singh	Linear Feedback Shift Register(LFSR) Using Gate Diffusion Input	Xilinx 13.2i	Slice = 104, Power = 34.72 uW
6.	Design and Analysis of a 32 Bit Linear Feedback Shift Register Using VHDL, IEEE 2014	Shruti Hathwalia, Meenakshi Yadav	Linear Feedback Shift Register which generates pseudo-random test patterns as the input bit is a linear function	Xilinx 12.1i	Slice = 18, Slice flip flop = 32, IOBs = 34

IV. LINEAR FEEDBACK SHIFT REGISTER

Linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. An LFSR is a class of devices known as state machine. It is a shift register whose input bit is a linear function of its previous state. The only linear functions of single bits are XOR and XNOR. Thus it is a shift register whose input bit is driven by XOR or XNOR of some bits of overall shift register value.

Theory of Operation: - Feedback around an LFSR's shift register comes from a selection of points (taps) in the register chain and constitutes XORing these taps to provide tap(s) back into the register. Register bits that do not need an input tap, operate as a standard shift register. It is this feedback that causes the register to loop through repetitive sequences of pseudo-random value. The choice of taps determines how many values there are in a given sequence before the sequence repeats. The implemented LFSR uses a one-to-many structure, rather than a many-to-one structure, since this structure always has the shortest clock-to-clock delay path.

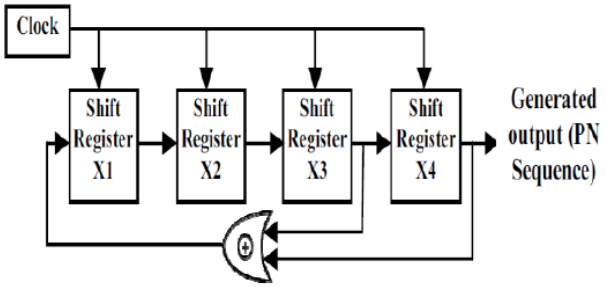

Figure 7: Basic block diagram of LFSR

Pseudo random number sequence generator is generated in VHDL according to the following circuit in Figure 1 based on the concept of shift register. The bits in the LFSR state which influence the input are called taps. A maximum-length LFSR produces an m- sequence (i.e. it cycles through all possible 2n - 1 state within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change. The sequence of numbers generated by this method is random. The period of the sequence is (2n - 1), where n is the number of shift registers used in the design.

V. PROPOSED METHODOLOGY

This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name Shift Register.

A shift register basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.

Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.

The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches.

Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

Shift register IC's are generally provided with a *clear* or *reset* connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

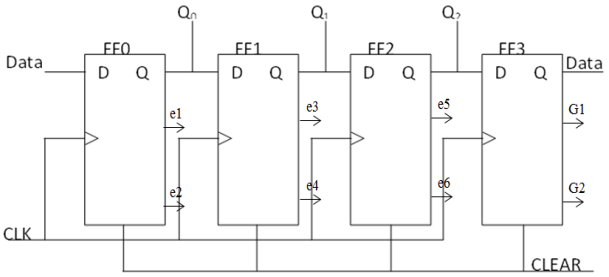

Figure 8: Flow Diagram of Serial in Parallel Output Shift Register

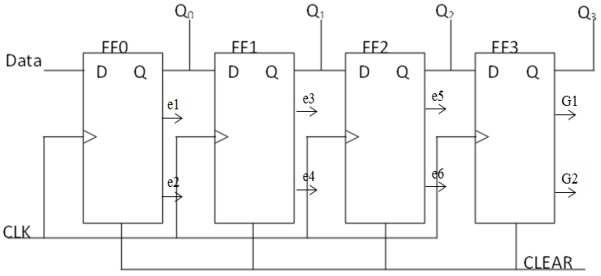

Figure 9: Flow Diagram of Parallel in Serial Output Shift Register

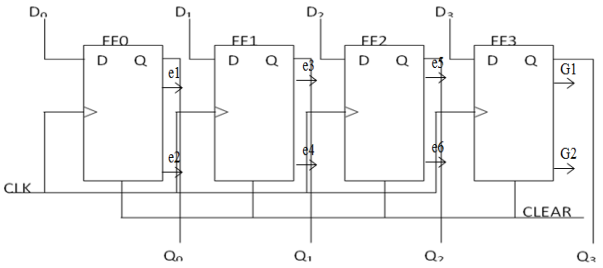

Figure 10: Flow Diagram of Parallel in Parallel Output Shift Register

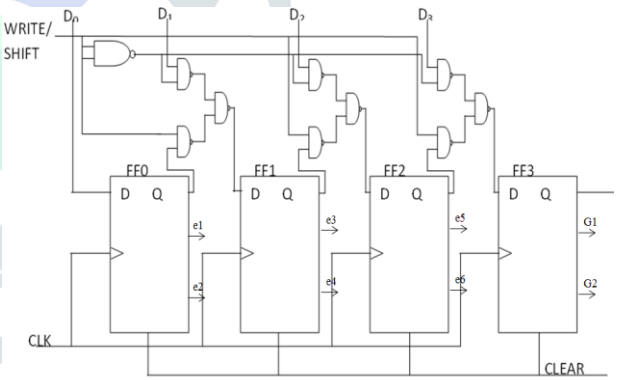

Figure 11: Block Diagram of Reversible Parallel in Serial out Shift Register

VI. EXPECTED RESULT

The proposed implementation is programmed (Described) and implemented using VHDL language which is a Hardware Description Language that was developed by the Institute of Electrical and Electronic Engineers (IEEE) as a standard language for describing the structure and behavior of digital electronic systems. It has many features appropriate for describing the behavior of electronic components ranging from simple logic gates to complete microprocessors and custom chips. The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams, or system-level VHDL descriptions) for the purpose of simulation.

- Design 4-bit, 8-bit and 16-bit register with the help of logic gate and flip flop.

- All design are implemented using Xilinx Software for different device family and calculate various parameter i.e.
- Number of Slice
- Number of LUTs
- Number of Flip Flop Pair
- Number of Input Output
- Delay

All design will be compared with the previous base paper (2018) in different device family and achieved good result.

Table II: Comparison Result for 8-bit Shift Register

Register	Design	Bit	Minimum Period	Arrival time before max input clock	Number of Slice	Slice Flip Flop
SISO	Previous Design	8-bit	2.432 ns	2.993 ns	6	10
	Proposed Design		1.343 ns	2.474 ns	6	10
SIPO	Previous Design	8-bit	2.521 ns	2.892 ns	7	10
	Proposed Design		1.343 ns	2.474 ns	6	10
PISO	Previous Design	8-bit	3.053 ns	3.461ns	7	10
	Proposed Design		1.333 ns	2.474 ns	5	10
PIPO	Previous Design	8-bit	-	2.867 ns	7	10
	Proposed Design		-	2.454 ns	5	9

VII. CONCLUSION

Design of a random testing circuit based on LFSR for the external memory interface is discussed in this paper. The random test patterns can improve testing efficiency, and reduce the artificial dependence in testing process in any circuit. Definitely 16-bit LFSR with maximum length feedback polynomial will generate large sequence which is more secure than other but because of simulation difficulties modification in long bit LFSR is needed.

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