An Evaluation of 128-bit Addition using Ripple Carry Adder with Layout based on CMOS 28 Transistor and 24 Transistor Full Adder in 90 nm Technology

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Abstract: Adding two 128 bits numbers has been common with microprocessors with over 1 GHz and memory capacity raced over 40 bits or Tera bits in PC or Smart Phones. Ripple Carry Adder (RCA) is the simplest technique with almost lowest area and a comparative power factor when compared to other adder techniques. This paper will present simulation and layout of 128 addition from a 64 bits, 4 bits, full adder, and half adder with Mentor and Microwind tools at 90 nm technology based on CMOS 28 or 24 transistor full adder layouts.

IndexTerms **- Ripple Carry Adder, Addition, CMOS, Layout, 90 nm Technology.**

I. INTRODUCTION

A Giga Hertz (GHz) Microprocessor processes information at a "Nano second" (ns) cycle time as billion of mobiles and millions of laptops or tablets or personal computers have been sold in 2017 to 2019. 10 GHz microprocessors have been pushing technology with addition done by Arithmetic Logic Unit (ALU) especially in Digital Signal Processing (DSP) or Internet of Things (IOT) or Artificial Intelligence (AI) with facial or voice recognition. Video processing will dominate in next ten years where adder plays a significant role. A "Full Adder" has to be designed with Verilog and verified, with simulated at logic and circuit level. Finally it has to be drawn in so called "Layout" in CMOS. The layout of 128 bit adder with Ripple Carry" techniques used in data processing will be shown based on 28 or 24 transistor 90 nm CMOS technology.

II. ADDER DESIGN

Addition of four bits will be done from Least Significant Bit (LSB) of two inputs. But at LSB there are only two bits, but from addition of next bit there are three inputs because a carry is generated at LSB level based on the logic as shown in table 1. A "Half Adder" (HA) performs addition of LSB bits of each input A and B. It also will generate two 3outputs called "Sum" and "Carry out" as shown in table 1. A basic logic design begins with a truth table and converts into a Kernaugh Map or K-Map to optimized the logic design with equation.

Table 1: Truth table & K-Map for Half-Adder

A	B	Sum	Co
0	0	0	0
0	0	1	0
0	1	1	0
0	1	0	1

For Sum

A \ B	0	1
0	0	1
1	1	0

For Carry Out

A \ B	0	1
0	0	0
1	0	1

The equation for Sum for HA from K-Map

S = AB' + A'B or A ⊕ B ----- eq 1.1

the symbol ⊕ stands for Exclusive OR (ExOR). A' is the complement of A.

The equation for Carry Out of a HA from K-Map

Carry Out = AB ----- eq 1.2

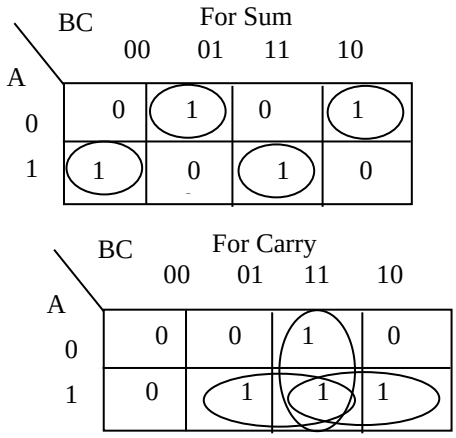
From 2nd bit onwards, the addition has to take place from three bits which are two inputs A and B with Carry out generated at LSB which has been defined as "Full Adder" (FA) and truth table has been shown in table 2 (Mano, 2002). So a FA has three inputs: A, B, Carry in (Cin) and two outputs: Sum, Carry out. The logic evolves from 3 inputs with 8 combinations as shown in table 2. A simple addition of binary mathematics for three bit has been shown as truth table in table 2. The equation for Sum for a Full Adder from K-Map is not simple, so take individual terms from K-Map for a value of "1"

S = AB'Cin' + A'B'Cin + A'BCin' + ABCin (take Cin' in 1st and 3rd term, 2nd and 4th terms)
= (AB' + AB')Cin' + (A'B' + AB)Cin
= (A ⊕ B)Cin' + (A ⊕ B)Cin
= (A ⊕ B)Cin' + ((A ⊕ B)')Cin
= A ⊕ B ⊕ Cin ----- eq 1.3

S = A ⊕ B ⊕ Cin, the symbol ⊕ stands for Exclusive OR, logically when inputs are not equal output will be ONE else output will Zero.

Table 2: Truth table & K-Map for Full Adder

A	B	Cin	Sum	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

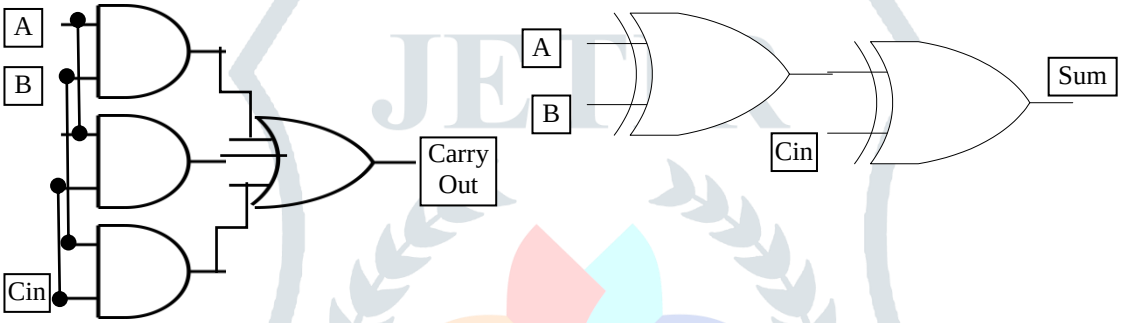


Equation for Carry out is

Co = AB + ACin + BCin or AB + (A⊕B)Cin ----- eq 1.4

The logic from equations 1.3 and 1.4 will translated in logic as symbols fundamental for design of Integrated Circuits for CMOS or any other technology. Sum has two ExOr and Carry Out has two logic levels. First is AND gates and 2nd stage is OR as shown in figure 1. This can be done with a NAND and NAND implement in CMOS easily.

Figure 1: Logic Diagram for Carry out and Sum, Full Adder

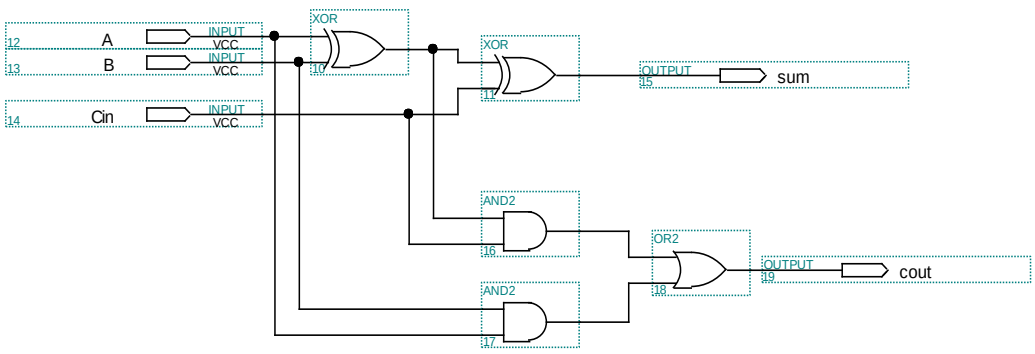


A Very Large Scale Integrate (VLSI) design over thousands of Integrated Circuits in Metal Oxide Semiconductor (MOS) requires automation of logic with Electronic Design Automation (EDA) tools with Mentor or Cadence or Synopsys or Microwind. Generally, logic is defined as a behavioural model with respect to truth table as defined in table 2 for this case "Full Adder". Verilog is a open source logic accepted by any EDA tool vendor and after RTL, a logic diagram will be developed (Weste, 1993). A Verilog code for a Full adder is

```
module fulladder(a,b,c,sum,carry);
  input a,b,c;
  output sum,carry;
assign sum = a ^ b ^ c;
assign carry = (a & b) | (b & c) | (c & a);
endmodule
```

A full adders with two exclusive OR gates is shown for the output Sum and two AND and a OR shown for Carry out in the figure 2 after the logic synthesis from Mentor Tools. ExOR from A and B can replace an AND gate.

Figure 2: Logic Diagram generated for a Full Adder in Mentor tools

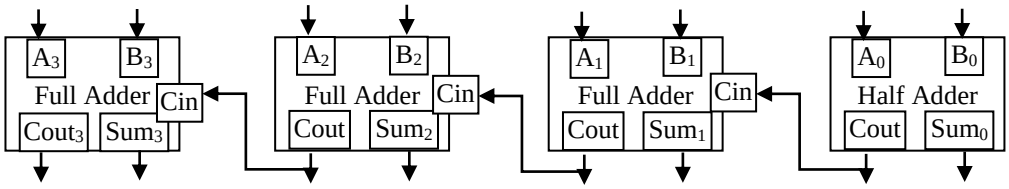


III. 4 BIT RIPPLE CARRY ADDER

A simple design of addition has been based on propagating carry from right to left as done in physical addition process of decimal system or binary system one learns in high school. So, the "Carry out" becomes "Cin" at next stage where a full adder is used because there are three inputs. So a half adder and three full adders are used to design a 4 bit Ripple Carry Adder. The delay for the Carry Out would be based on the "Carry out = AB + (A+B)Cin" implemented with two AND gates in first stage and a OR

gate in second stage so the total delay will be 2 gates. Four "Full Adders" are connected in series so the carry ripple through each adder stage as shown in figure 3. So the gate delay for 4 bit RCA is 8 gates. A gate delay is primarily defined by gate length L.

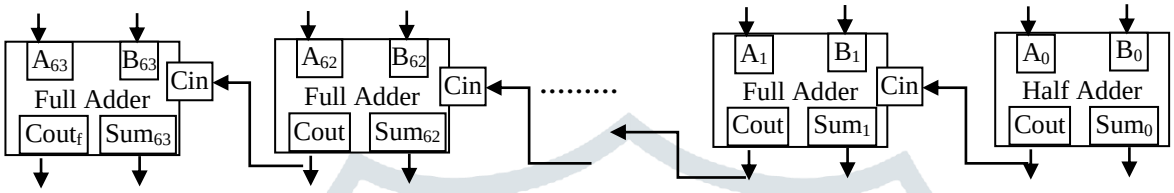
Figure 3: Logic Diagram for a 4 bit RCA



IV. 64 BIT AND 128 BIT RIPPLE CARRY ADDER DESIGN

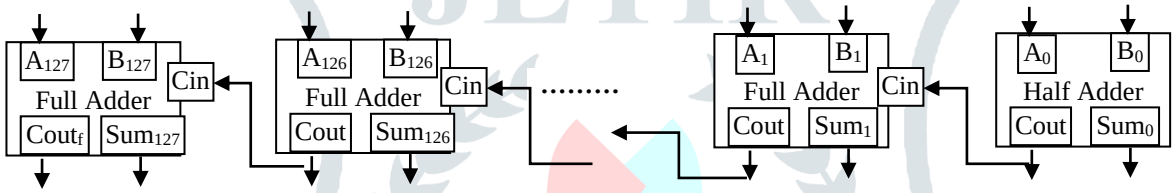
64 bit RCA has sixteen 4-bit Ripple Carry Adders but only the first 4-bit RCA has a half adder. 16 gate delays for 8 bit RCA, 32 gate delays for 16 bit RCA, and 64 gate delays for 32 bit RCA is the critical path. So the gate delay for 64 bit RCA is128 gates.

Figure 4: Logic Diagram for a 64 bit RCA



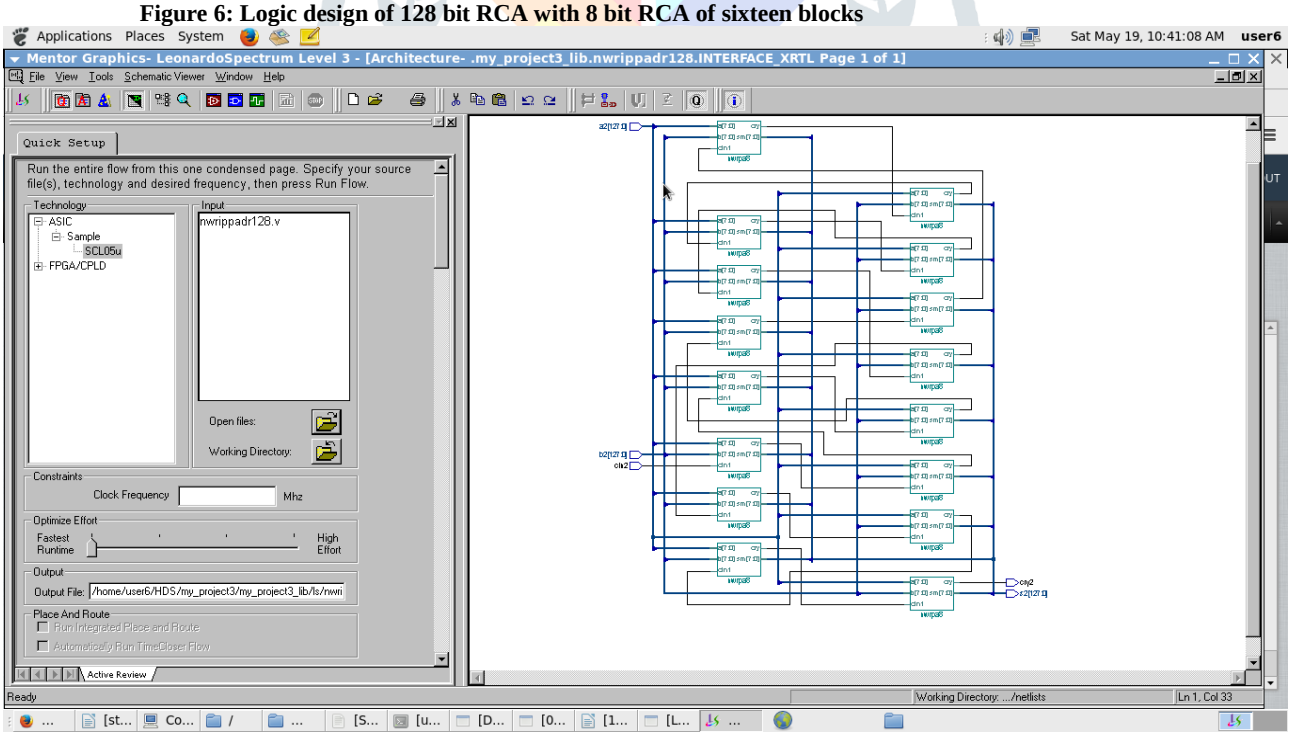
A 128 bit RCA there will be 256 gate delays and design has been shown in figure 5. There are no papers in open access have simulated for 128 bits. Also, the EDA tools are complicated and costly.

Figure 5: Logic Diagram for a 128 bit RCA



The total logic gate count for 128 bit RCA is 11,274 in this design using Mentor tools as shown in figure 6.

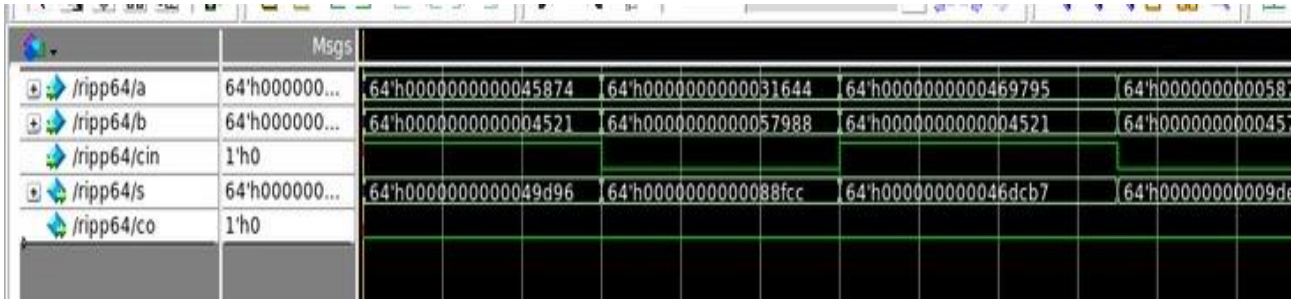
Figure 6: Logic design of 128 bit RCA with 8 bit RCA of sixteen blocks



V. Simulation and Layout of 128 bit RCA

64 bit RCA has been simulated in Mentor tool called Questa_sim and Leonardo spectrum as shown in figure 7 with A=45986, B=4521, Sum will be 49d96 as first case. In 2nd case, A=31644, B=57988 and Sum = 88FCC and in last case, A=469795, B=4521 and Sum = 46DCB7.

Figure 7. Simulation of 64 bit RCA in Mentor Tools

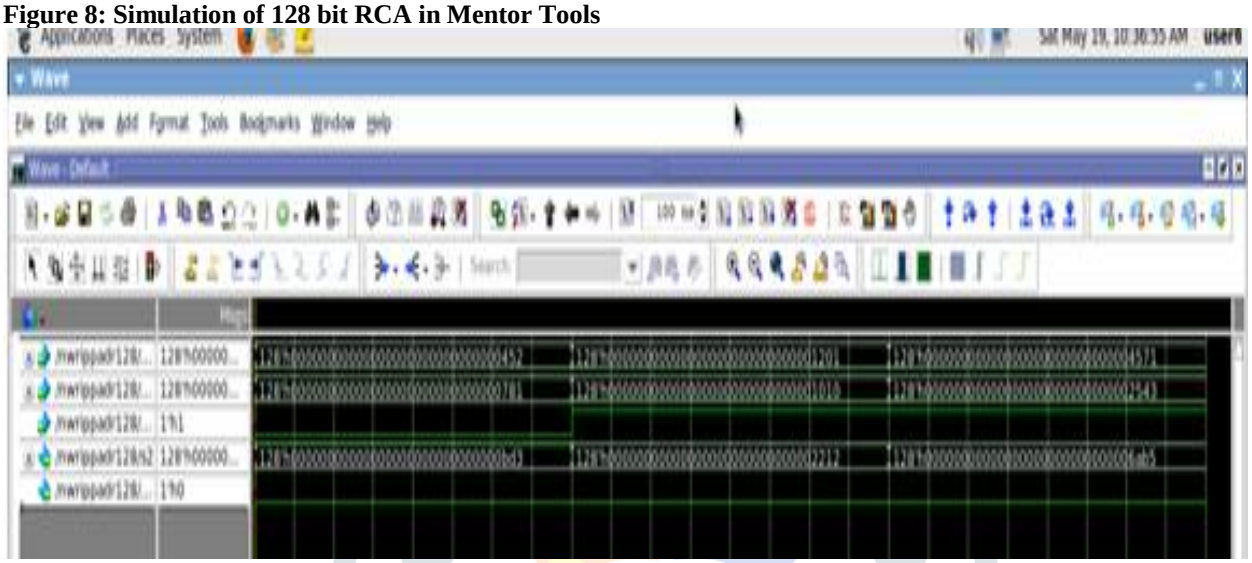


Mentor Logical Simulation begins with a set of inputs to the 128 bit RCA and verifies the outputs of 128 bit of Sum and a Carryout have to be checked and make sure they are correct as shown in figure 8.

A = 452, B = 781 and Cin= 0, Output is BD3, Carry out = 0,

A = 1201, B = 1010 and Cin= 1, Output is 2212, Carry out = 0, A = 4571, B= 2543 and Cin= 1, Output is 6AB5, Carry out = 0

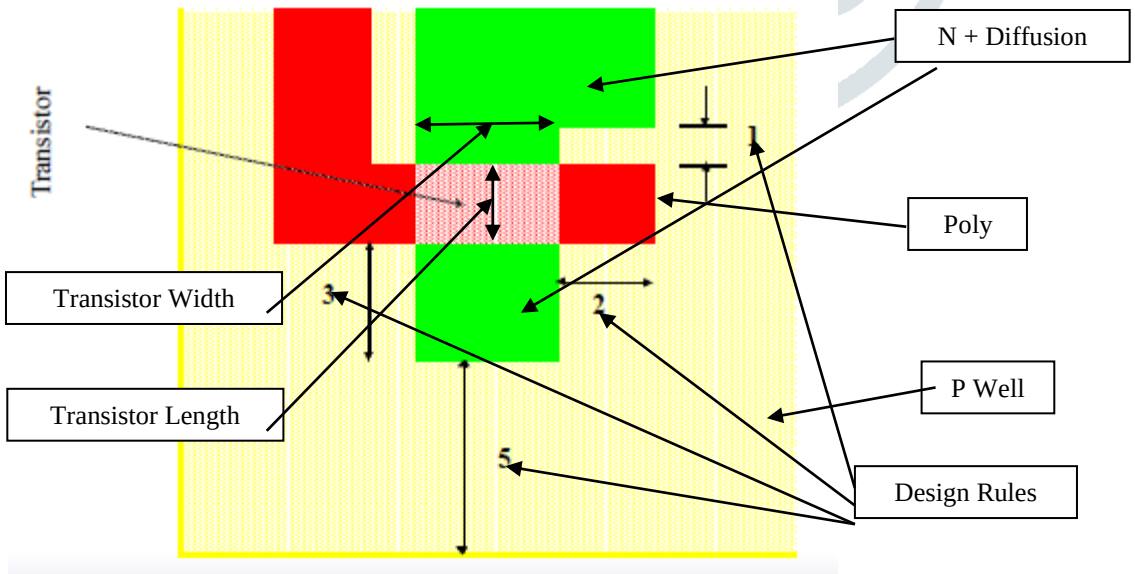
Figure 8: Simulation of 128 bit RCA in Mentor Tools



VI. Layout of 64 bit and 128 bit RCA in CMOS

A transistor is the basic component of layout with layers used to build the process of electrical terms defined for CMOS transistor as shown in figure 9, George P. Patsis (2018) and Microwind User manual.

Figure 9: Basic nMOS transistor, Red is Poly, Green is N+ Diffusion with layout rules



These layers are N-Well where P Transistors will be fabricated which is the first “Mask”. Next step is active transistor area with Poly, generally colour Red has been used, 2nd “Mask”. Then N+ Diffusion for source and drain of N transistor has been defined with Green Colour. 3rd “Mask”.

Next, P+ Diffusion for source and drain of P transistor has been defined with Purple or Yellow Colour, 4th “Mask”. To make Vdd connect to P Transistor or Vss / Ground to the source of N Transistor a “Contact” in black colour has been defined, 4th “Mask”. A Field Oxide “Mask” will be defined to isolate each transistor of P or N next the Vdd or Vss diffusion of source, called “Bulk” Contact, 5th “Mask”.

Using Microwind tools, a layout for this 28 transistor has been shown in figure 10 by N. Zhuang and H. Wu (1992) and layout in figure 11 with red colour representing "Poly", top with Purple colour is "P Diffusion", bottom in Green is "N Diffusion", with Contacts White Colour, and Metal 1 in Blue. Vdd is in top and Vss in the bottom.

Figure 10.: A Standard 28 transistor Full Adder by N. Zhuang and H. Wu (1992)

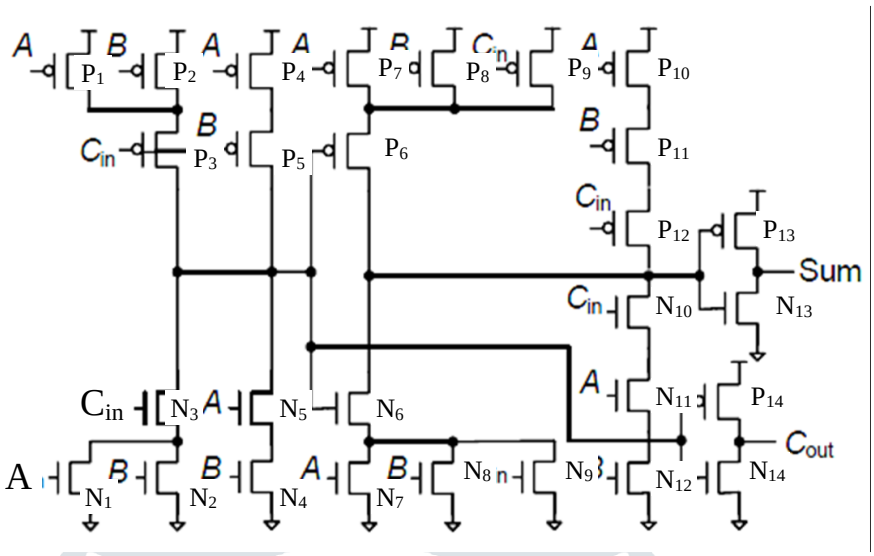
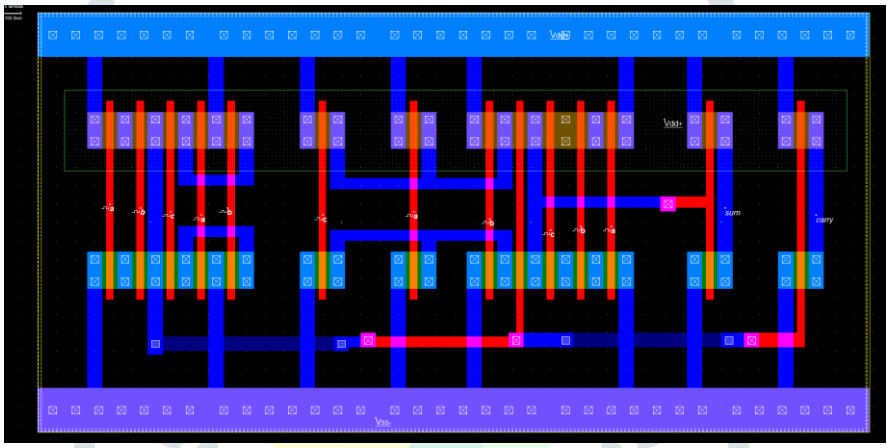
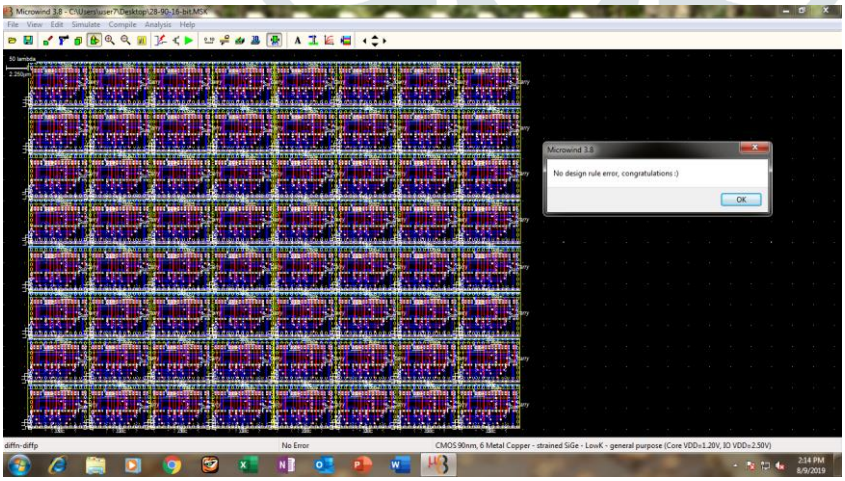


Figure 11: A Layout for standard 28 transistor Full Adder



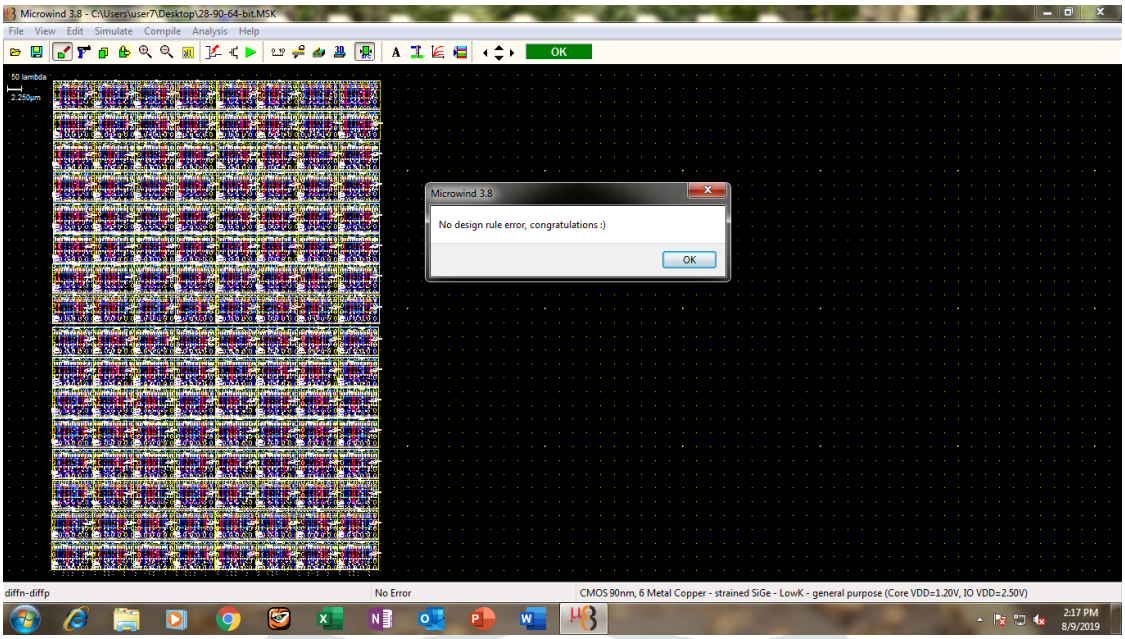
8 slices vertically and 8 slices horizontally used for the layout of a 64 bit RCA with a 28 transistor full adder, as shown in figure 12 using Microwind tools. A 64 bit RCA has an area of 39.7 um by 53.4 um with a total area of 2.487.2 square um.

Figure 12: A Layout for 64 bit Ripple Carry Adder with a standard 28 transistor FA



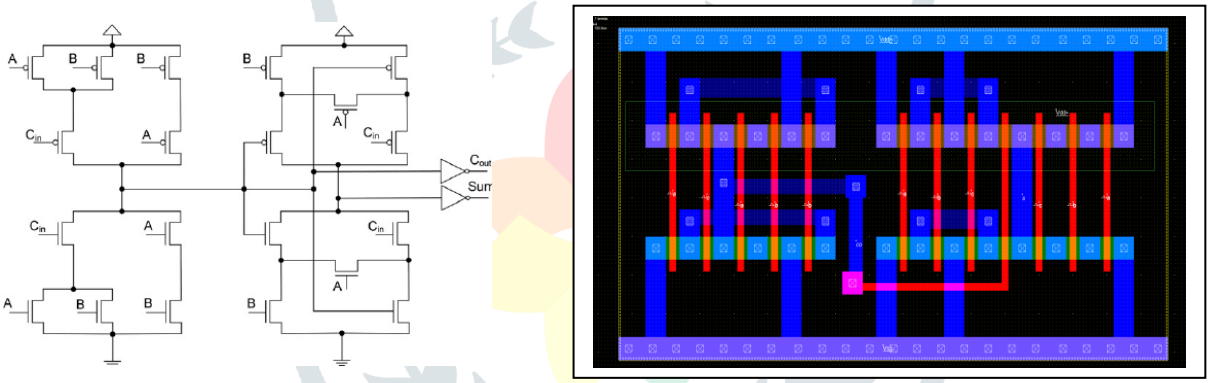
The layout of a 128 bit Ripple Carry Adder with a standard 28 transistor full adder, as shown in figure 13 using Microwind tools with an area of 80 um by 53.4 um with a total area of 4285.7square um with 1,792 nMOS transistor and 1,792 pMOS transistors.

Figure 13: A Layout for 128 bit Ripple Carry Adder with a standard 28 transistor FA



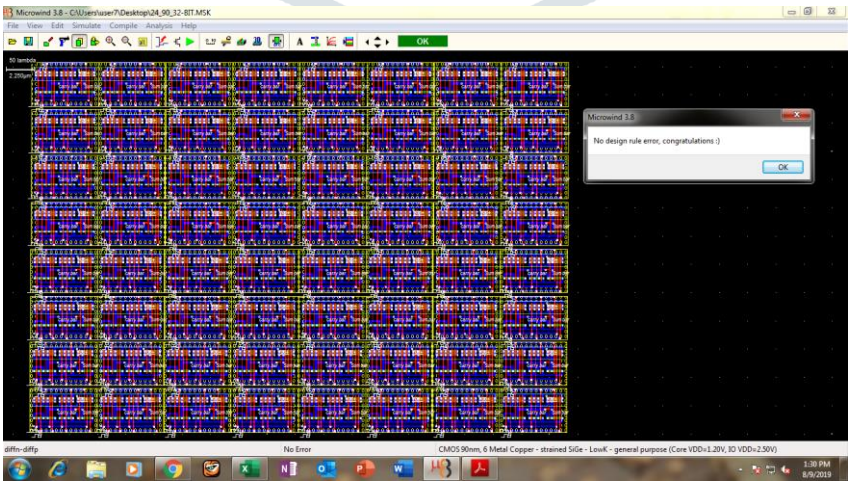
This design is a modified version of a 28 transistor design for a full adder shown in previous section. Both Sum and Carryout has inverters too. In the second section, the design has used only four pMOS transistors to connect P6 and another four nMOS transistors to connect N6. If anyone input is high a low passed throught nMOS, similarly if anyone input is low a high is passed through pMOS. So the transistor size has been lowered to 24. The design is shown in figure 14.

Figure 14: A Standard 24 transistor Full Adder with Layout in Microwind



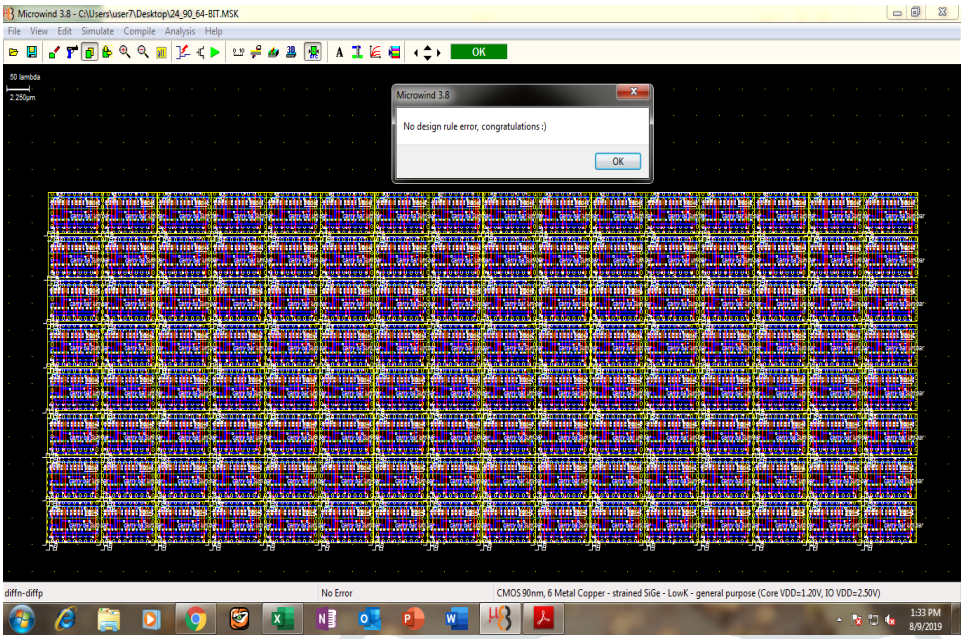
The layout for a 24 transistor based full adder has been done in Microwind tool and shown in figure 14 with Poly for in Red Colour, N Diffusion in the bottom, P Diffusion on top with metal in Blue Colour. The layout of a 64 bit Ripple Carry Adder has been shown figure 15 with 24 transistor full adder, has an area is 29.4 um by 42.9 um.

Figure 15: A Layout for 64 bit Ripple Carry Adder with standard 24 transistor FA



The layout of a 128 bit Ripple Carry Adder has been shown figure 16 with 24 transistor full adder, has an area is 84.5 um by 29.4 um with total area of 2,516.3 square um. It has 1536 nMOS and pMOS transistors.

Figure 16: A Layout for 128 bit Ripple Carry Adder with standard 24 transistor FA



VII. Results and Discussion

The Ripple Carry Adder has been simulated for 64 and 128 bits using Mentor graphics with 90 nm CMOS technology. The simulation results of these two designs for RCA in terms of delay and gate count as shown in table 3. Gate count has been doubled from 64 bits to 128 bits but the delay increased by not even 50 percent 64 bit design.

Table 3: Area and Delay comparison of 64 and 128 bit RCA

NAME	GATE COUNT	DELAY
64 bits	5461	22.0 ns
128 bit	11,274	32.5 ns

Balasubramanian P and S. Yamashit, (2016) did a simulation of various adders at 32 bits and found a 32 bit RCA had a delay of 3.29 ns, simulated with a 32/28 nm CMOS process of Synopsys. This is a better process than what has been used in this result which is at 90 nm. According to A Maheswara Reddy and G V Vijayalakshmi (2016), the delay of RCA at 64 bits is 4.87 ns and at 128 bits it is 8.4 ns. For Kogge-Stone adder, the delay is 8.69 ns for 64 bits and 10.06 ns for 128 bits but they not mentioned what technology they were using only said delays obtained from the Xilinx ISE synthesis. P. Manga Rao and K. Ashok Kumar (2014) have used 0.18-m CMOS technology for CSLA structure of 32 bit with a delay of 15.63 ns, at 64 bits the delay was 29.75 ns and at 128 bits the delay was 36.52 ns. The implemented was done with Verilog-HDL in Modelsim and sunthesized using Xilinx ISE 10.1. Shoba Mohan and Nakkeeran Rangaswamy (2016) did a 8 bit RCA with GDI technology and got a delay of 31 ns at 250nm technology

Table 4: Layout comparison of RCA with three full adder circuits

Type of Ful Adder used in the Design	Bits of the Adder	Size in um	Total Area in square um
28 Transistors	64 bit	53.4 x 39.7	2,487
	128 bit	53.4 x 80	4,285
24 Transistors	64 bit	42.9 x 29.4	1,262
	128 bit	85.5 x 29.4	2,516

24 transistor based full adder has half the area of at 64 bit RCA when compared with the area with 28 transistor based full adder but at 128 bits area with 24 transistor base full adder is about 40 percent that of 28 transistor full adder. 24 transistor based full adder is preferred and none has done even 64 bit layout yet.

P. Manga Rao and K. Ashok Kumar (2014) have used 0.18-m CMOS technology for CSLA structure of 32 bit had area 87 sq um, at 64 bits area was 186 um^2 and at 128 bits area was 431um^2., but this desing was CSLA. According to Balasubramanian P and S. Yamashit, (2016), a 32 bit RCA had an area of 2,049 square um which is 40 percent more than the 64 bit RCA with 24 transistors, even with 28 transistors at 64 bits the area is just 20 percent more.

Conclusions

Complexity increased at 128 bit designed of RCA but it will boast the performance of any microprocessor. It has less gate count than most adder architectures. This has been done with 90 nm technology in Mentor tool. At 19 ns, the One GHz microprocessor has to wait for 20 cycles to finish a 128 bit addition. One can do the design in 65 nm to reduced the delay as

microprocessors are going over 10 GHz speed. The area is the best with 24 transistors and one can do the layout at 65 or 45 nm as they are available through TSMC or Global foundaries academically.

REFERENCES

[1]. A Maheswara Reddy and G V Vijayalakshmi (2016), "Speed Comparison Parallel Prefix Adders with RCA and CSA in FPGA", IJIREC, Volume 2, Issue 5, July 2015, PP 8-16, ISSN 2349-4050 (Online)

[2]. Balasubramanian P and S. Yamashit, 2016, "Area/latency optimized early output asynchronous full adders and relative-timed ripple carry adders", SpringerPlus, 5:440, Pages 1-26.

[3]. Bharathi A, K. Manikandan, K. Rajasri, and Santhini, (2014), "High Speed Multioutput 128bit Carry Lookahead Adders Using Domino Logic", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 3 / 10

[4]. Bui, H.T., Y.Wang, and Y.Jiang (2002), "Design and Analysis of Low-Power 10-transistor Full Adders using Novel XOR-XNOR gates", IEEE Transactions on Circuits and Systems – II, Analaog and Digital Signal Processing, Vol. 49, No.1.

[5]. George P. Patsis (2018), "Educational Introduction to VLSI Layout Design with Microwind", IOSR Journal of VLSI and Signal Processing, (IOSR-JVSP), Volume 8, Issue 5, Ver. I (Sep. - Oct. 2018), PP 18-29, e-ISSN: 2319 – 4200

[6]. P. Manga Rao and K. Ashok Kumar (2014), "An optimized implementation of 128 bit Carry Select Adder using binary to excess-one converter for delay reduction and area efficiency", International Journal of Professional Engineering Studies, Vol. IV, Issue 4, December.

[7]. Kishore Prabhala, Haritha Dasari, and Thrinadh Komatipalli (2018), "Performance Comparison of 64-Bit Adders", IJEDR, Volume 6, Issue 2, June 2018, ISSN: 2321 9939

[8]. Kishore Prabhala (2016), A Study of CMOS VLSI Technology Landscape Challenges towards 7 nm, International Conference in Electronic and Electrical Engineering, ICAECS 2016. 10th Dec., 2016, Vadlamudi, Guntur Dist., AP.

[9]. Morris Mano "Digital Design". Pearson Education Asia. 3rd Ed, 2002.

[10] Shoba Mohan and Nakkeeran Rangaswamy (2016), "Design of Ripple Carry Adder using GDI logic", Pondicherry University, https://www.researchgate.net/publication/300113051

[12]. Weste, N. and K. Eshranghian, "Principles of CMOS VLSI Design: A System Perspective," Reading MA:Wesley, 1993.

[13]. Zhuang N. and H. Wu (1992), "A new design of the CMOS full adder," IEEE J. Solid State Circuits, vol. 27 / 5, pp. 840–844.

[14]. Zimmermann R. and W. Fichtner (1997), "Low-Power Logic Styles: CMOS Vs Pass- Transistor Logic" IEEE Journal of Solid-State Circuits, vol. 32 / 7, pp. 1079–1090.