Performance Analysis of Thermal Aware Floor Planning Techniques

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***Abstract*— Floor planning is a prominent area in the (VLSI) circuit design automation, because it affects the performance, size, yield and reliability of the VLSI chips. Shrinking of manufacturing process, the power density of chips has increased under such a large power density the temperature problem will be highlighted. As technology progresses and the number of IP core in chips increases, power density in SoCs caused local temperature rose rapidly, which affects the stability of chips? Especially, how to avoid the local hotspots problem has become a major challenge in the design stage. Due to this problem thermal-aware floor planning attracts the researchers' attention. PSO based approach for VLSI floor planning exhibits rapid convergence, leads to more optimal solutions and gives reasonable solutions only on the hard IP modules placement problem. Modeling wire delay without considering temperature variations(gradient) in different areas of the die crossed by global wires can lead to too pessimistic, or in general in accurate, estimates. A PSO-GA based hybrid algorithm is used to reduce the area, wire length, and hotspot by distributing the temperature evenly across the chip. Using geometric programming (GP) method it is possible to find a floor plan that can reduce the maximum temperature of the chip and lower the chip area while maintaining comparable performance.**

***Keywords*— Very Large-Scale Integrated, Thermal Aware Floor Planning, Genetic Algorithm, Particle Swarm Optimization, Harmony Search Algorithm.**

1. INTRODUCTION

VLSI physical design automation process plays an essential role in fabrication of ICs. In the physical design cycle, floor planning is a important step because it affects the successive process such as placement and routing [1]. The primary objective for floor planning is to minimize the total area required to accommodate all of the functional blocks on a chip. To handle the design complication, Intellectual Property (IP) modules are widely used. This makes the floor planning problem as Non-Deterministic Polynomial time (NP) hard problem [1]. Floor plan is of two forms: 1) slicing floor plan, 2) non-slicing floor plan. In non-slicing floor plan, modules in the layout cannot be obtained by either horizontal or vertical bisection. Area occupied by slicing floor plan representation is large compared to non-slicing representation. Also, modules in the floor plan can be either hard modules or soft modules. Hard modules have fixed width (W) and height (H) whereas soft modules have varied aspect ratio [3].

1.1 Thermal aware floor planning

In recent years, as thermal issues become crucial, the maximum temperature is also added to the cost functions [3].The hotspot in a modern chip might have a temperature of greater than 100oC, where the intra chip temperature differentials can be larger than 10~20o C. Temperature can have a dramatic impact on circuit performance . Power-aware design alone is not able to address the temperature challenge, because the thermal distribution profile based on not only the power density but also the physical size and location of each functional block [2]. High temperature will affect the chips in several ways. First, the carrier mobility is degraded at higher temperature, and slows down the device. Secondly, the leakage power maximizes due to the exponential maximize of sub-threshold current with temperature. Lastly, the interconnect resistivity increases with temperature, leading to worse IR drops and interconnect RC delays, hence causing performance loss and complicating timing and noise analysis[4].

1.2 Thermal aware optimization Techniques

1.2.1 Genetic algorithm based thermal aware floorplanning methods:

Genetic algorithms (GA) are a class of search and optimization methods that mimic the evolutionary principles in natural selection.
In general, a genetic algorithm has the following steps:
1. Generation of initial population.
2. Fitness function evaluation.
3. Choice of chromosome.
4. Reproduction, Crossover, Mutation operations.

1.2.1.1 Thermal-aware floorplanning framework

This thermal-aware floor plan optimization flow is based on the genetic algorithm and is shown in Figure 2 below. The representation of a floor plan design is encoded into integer and bit mixed strings called chromosome. The optimization flow begins with a randomly produced initial population, which consists of many randomly generated (floorplan).chromosomes The placement of each block and the polish expression of slicing tree are obtained from individual rotate and slicing strings. The area evaluation function and Hot Spot are invoked to calculate dead space and temperature. The fitness is assigned to every population based on the evaluation of these two variables. The optimization flow is an iterative procedure. The chromosomes with more fitness will survive at each generation and the three different operations (reproduction, crossover and mutation) are evoked to derive a new group of chromosomes – or new floorplans. The iteration continues until the termination basis is met [2].

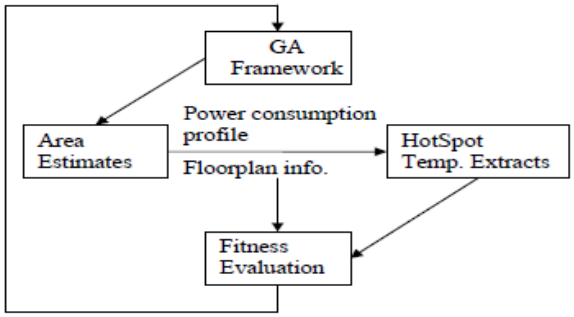

Figure 1.1: Thermal-aware floor planning flow

1.2.1.2 Hybrid Particle Swarm Optimization: Genetic Algorithm

1.2.1.2.1 Standard PSO Algorithm

Particle swarm optimization (PSO) is a viable method that optimizes the problem by iteratively refining a candidate's solution with regard to a given measure of quality. PSO optimizes a problem by forming a population of candidate solutions (from the B*-tree). The individuals in the population are named particles. By plying the PSO algorithm, the particles are rendered around in the search scope according to simple mathematical formulae upon the particle's position and velocity. Each particle's movement is effected by its local best-known position and is also leaded toward the best-known position in the search space. The particles which are updated as better locations are found by other particles. This is expected to move the swarm toward the best solutions [5].PSO is a bio-inspired algorithm based on population. The individual elements of the population are called as particles. For individual particles the fitness value is computed [1].

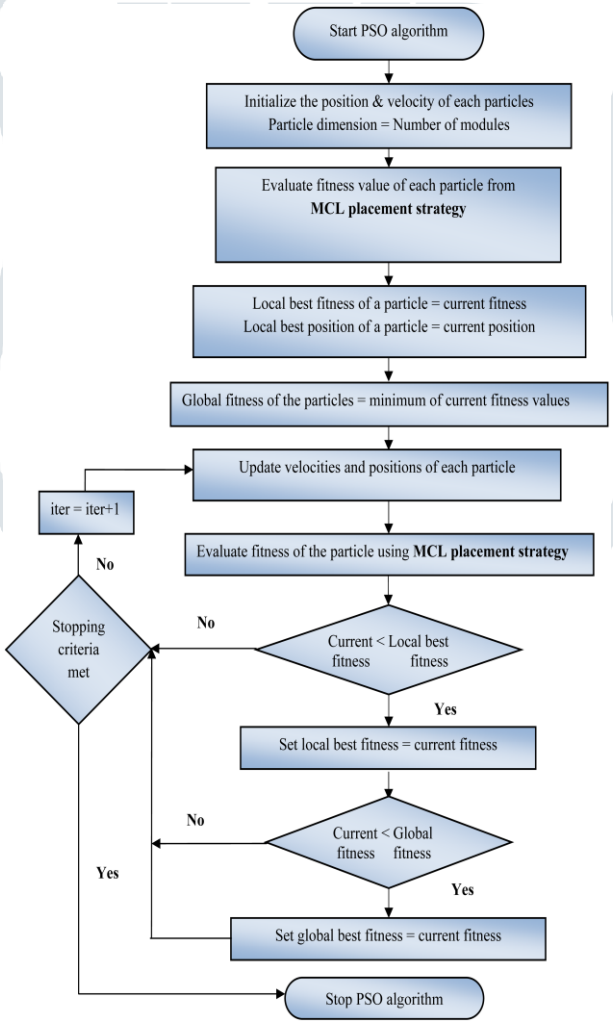

Figure 1.2: Flowchart of PSO algorithms [1]

1.2.2 Temperature Aware Floorplanning via Geometry Programming

Incremental floor planning problems get more and more attention with the rapid advancement of technology. It is very hard for designer to meet all the geometry constraints or performance acquirements. Therefore, it is essential to execute the incremental modifications. The incremental area of a chip also significant affects the temperature of module. In order to keep the chip temperature below a specific limit, the increasing chip area can be a cost function. Since the cost of maximizing the chip area is about the inverse rate as power density, reducing the maximum temperature in the chip can minimize the cost of the cooling system, which constitutes a major component of the overall cost. With increases in power density of digital circuits is fast becoming a significant process in microprocessor design. Recently temperature aware designs have been used. Temperature aware design issues for simultaneous Multithreading and Chip Multiprocessing architectures have been studied. The thermal efficiency of SMT and CMP architectures have been take into account by and temperature

aware micro architectures have been proposed. However, it will benefit the design if a cost function that can co-optimize temperature reduction and chip region minimization in the optimization problem. A geometric programming (GP) is a type of mathematical optimization approach characterized by objective and constraint functions with special form [6].

1.2.3 Simulated Annealing Based Thermal-aware Floorplanning

A simulated annealing based thermal-aware floor planning framework considers the area and wire length. A module temperature model is established. Temperature matrix is constructed based on giving power and module information. The effective integration of floor planning process is implemented by combining both regulating area of some modules and adjusting module locations to effectively reduce chip temperature [4].

1.2.4 Harmony Search Algorithm

HS (Harmony Search algorithm) is a meta-heuristic and derivative-free algorithm based on music improvisation which is influenced by harmony present in the music. Harmony Memory Size (HMS), HMCR (Harmony Memory Consideration Rate) and PAR (Pitch Adjustment Rate) are the control variables of HS algorithm. The HMCR value deviates between 0 and 1; it is rate of selecting a particular value from the already stored values in HM, whereas (1-HMCR) is the rate of choosing a (random value) fresh value within the accessible possible limit (i X). Detailed flowchart of the proposed HS algorithm is shown in Figure 3 [1].

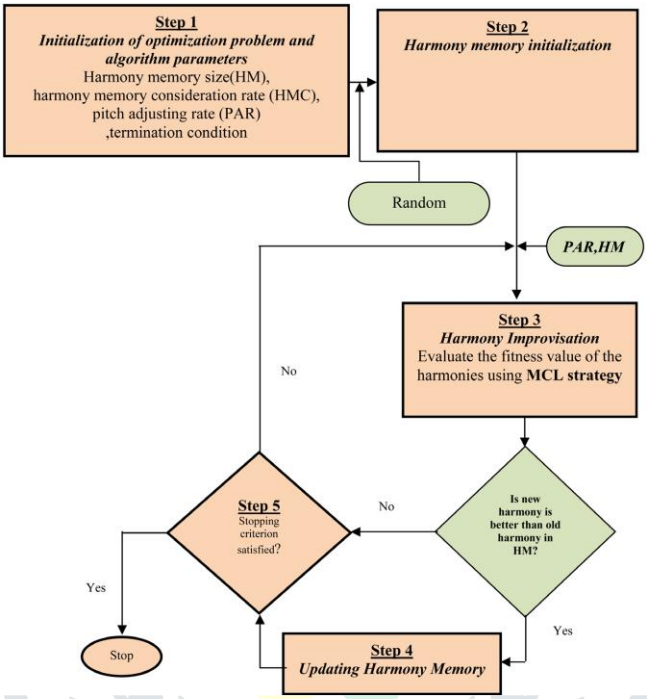

Figure 1.3: Flowchart of Harmony Search Algorithm

2. RELATED WORK

Sivaranjani Paramasivam et al. (2016) in this a methodology is given to distribute the temperature of the module on the layout while simultaneously optimizing the total area and wire length by applying a hybrid Particle Swarm Optimization-Harmony Search (HPSOHS) algorithm. This hybrid algorithm employs diversification method (PSO) to find global optima and intensification strategy (HS) to achieve the best solution at the local position and Modified Corner List algorithm (MCL) for floorplan representation. A thermal modeling tool called hotspot tool is combined with the proposed algorithm to obtain the temperature at the block level. The proposed algorithm is explained using Microelectronics Centre of North Carolina (MCNC) benchmark circuits. The results generated are relate with the solutions derived from other stochastic algorithms and the proposed algorithm provides better solution.

W-L. Hung et al. (2005) a genetic algorithm based thermal-aware floorplanning framework that aims at minimizing hot spots and distributing temperature evenly across a chip while optimizing the traditional structure metric, chip area. The floorplanning problem is developed as a genetic algorithm problem, and a tool called HotSpot is used to compute floorplanning temperature based on the power dissipation, the physical dimension, and the position of modules. Area and/or temperature optimizations lead the genetic algorithm to produce the final fittest solution. The experimental results plying MCNC benchmarks and a face recognition chip show that our integrated area and thermal optimization technique decreases the peak temperature adequately while providing floorplans that are as concise as the traditional area-oriented techniques.

Andreas Thor Winther et al. (2015) Traditional floor planning algorithms use wire length to evaluate wire performance. In this work, we show that this does not always generate a design with the shortest delay and author propose a floor planning algorithm taking into account temperature dependent wire delays one metric in the evaluation of a floor plan. In addition, we consider other temperature dependent factors such as congestion and interconnect reliability. The experiment results show theta shorter delay can be achieved using the proposed method

Lixia Qi et al. (2011) As technology advances, and the number of IP core in chips increases, power density in SoCs caused local temperature rose speedly, which affects the stability of chips. Aiming at SoC thermal problem, combining to lessen temperature structure and application of efficient cooling approches, Author suggests a simulated annealing depended thermal-aware floor planning for SoC design. The suggested method is applied to MCNC benchmark circuits, the results show that the temperature for MCNC hp can be minimized up to 23.

P. Sivaranjani et al. (2015) In this a smart decision-taking hybrid particle swarm optimization-genetic algorithm that stress at reducing the area, wire length, and hotspot by dividing the temperature smoothly across the chip is presented. B*-tree is used to generate the initial floorplan and next a PSO-GA based hybrid algorithm is used to produce an optimal placement solution. Temperature-driven floor planning is considered at the perturbation phase to separate the hotspots, thereby reducing the average and maximum temperature. The experimental results of the suggested algorithm are compared with other stochastic algorithms using MCNC and Alpha processor floorplan benchmark devices. The result shows that the proposed algorithm performs efficient floorplanning, with minimized average and peak temperature.

Yiming Li et al. (2008) In this author employ geometric programming (GP) technique for the minimum temperature and area floor planning problem. Noticed that it is a nonlinear convex problem and its optimal solution can be produced by GP method. The numerical result gives that the difference between the original temperatures and temperatures for MCNC ami33 after expansion can be as high as 80oC. Author has modified a floor planning tool to involve temperature as an objective for block area to reduce the hot spot temperature. Author gives that it is possible to find a floor plan that can minimize the maximum temperature of the chip and minimize the chip space while maintaining comparable performance.

3. PROPOSED WORK

In this work hybrid HPSO-ACO and HPSO-GA are implemented in C compiler using Oracle VM VirtualBox. The simulation is performed on ubuntu 10.04. Floorplanning problem of Apte, Xerox, Hp, Ami33 and Ami49 modules are considered. Their simulation results using simple GA, SA and hybrid HPSO-ACO and HPSO-GA will be compared thereafter.

4. RESULTS

Table 4.1: Comparison of thermal aware floorplan for different algorithms

Algorithm	Performance Parameter	Benchmark Circuits				
		Apte	Xerox	Hp	Ami33	Ami49
GA	Area	47.52	20.26	9.44	1.27	39.16
	Peak Temp.	118.10	88.2	120.5	103.5	121.2
HPSO-ACO	Area	48.1	20.2	9.99	1.22	39.8
	Peak Temp	77.8	79.3	81	121	89.6
SA	Area	48.66	-	9.78	1.27	38.86
	Peak Temp	78	-	89	87	95
HPSO-GA	Area	47.44	20.2	9.50	1.24	41.01
	Peak Temp	73.61	84.38	114.8	101.14	96.26

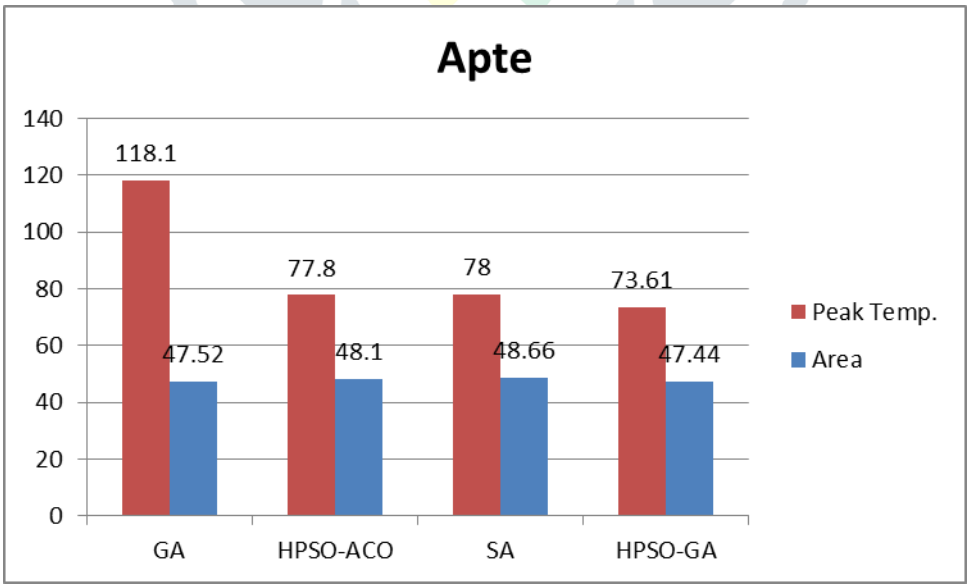

Figure 4.1: Peak Temp and Area Analysis of Various Optimization Methods for Apte Benchmark Circuit

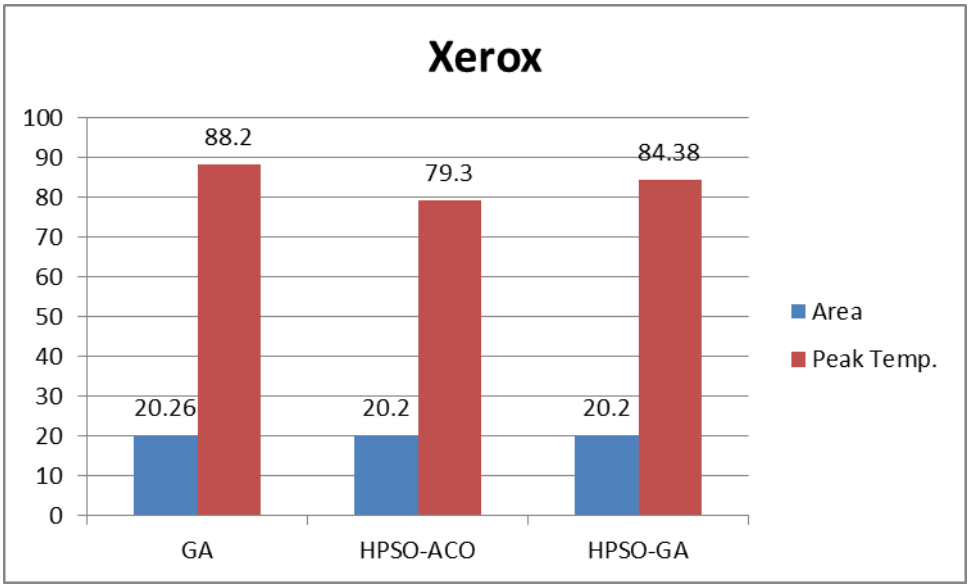

Figure 4.2: Peak Temp and Area Analysis of Various Optimization Methods for Xerox Benchmark Circuit

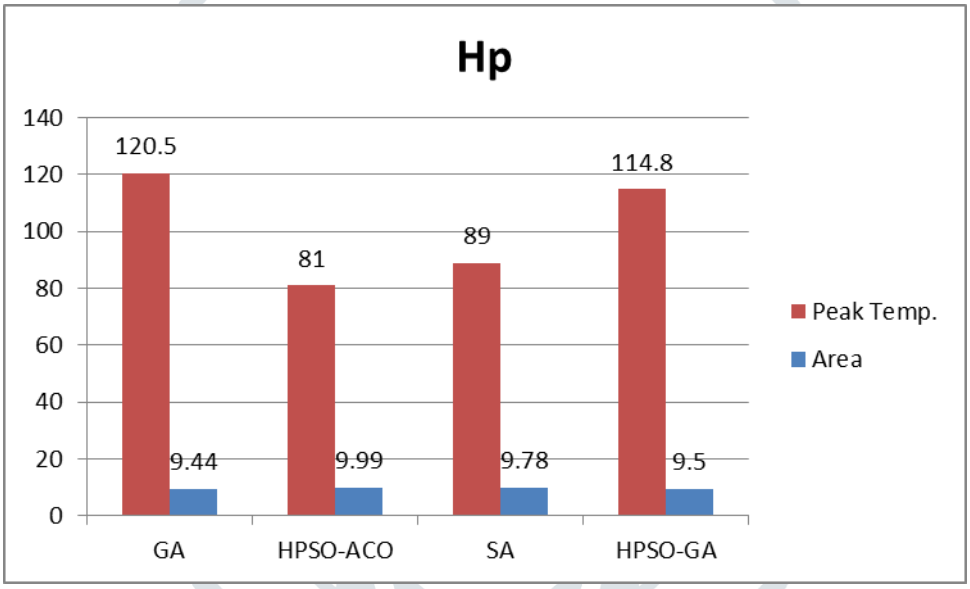

Figure 4.3: Peak Temp and Area Analysis of Various Optimization Methods for Hp Benchmark Circuit

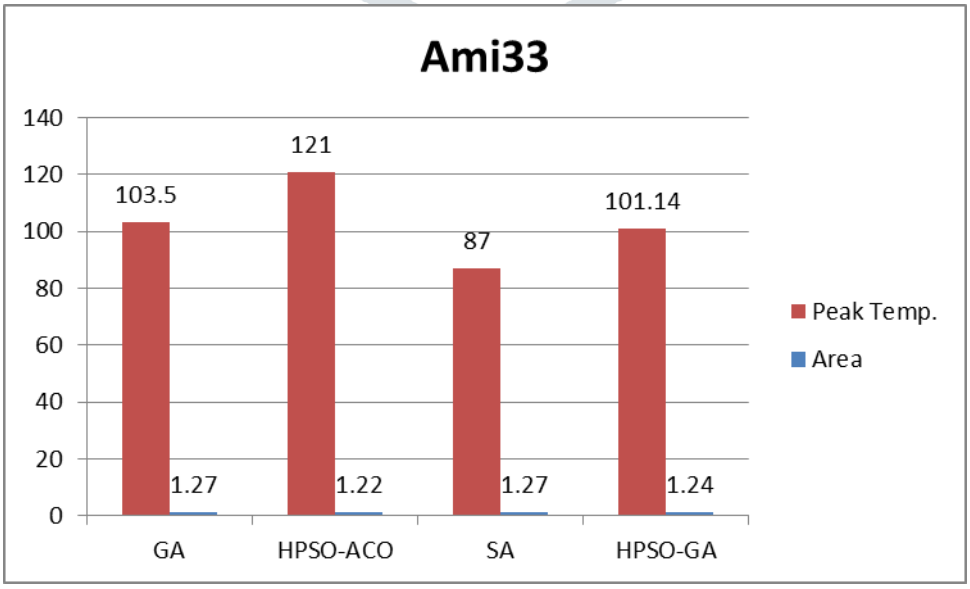

Figure 4.4: Peak Temp and Area Analysis of Various Optimization Methods for Ami33 Benchmark Circuit

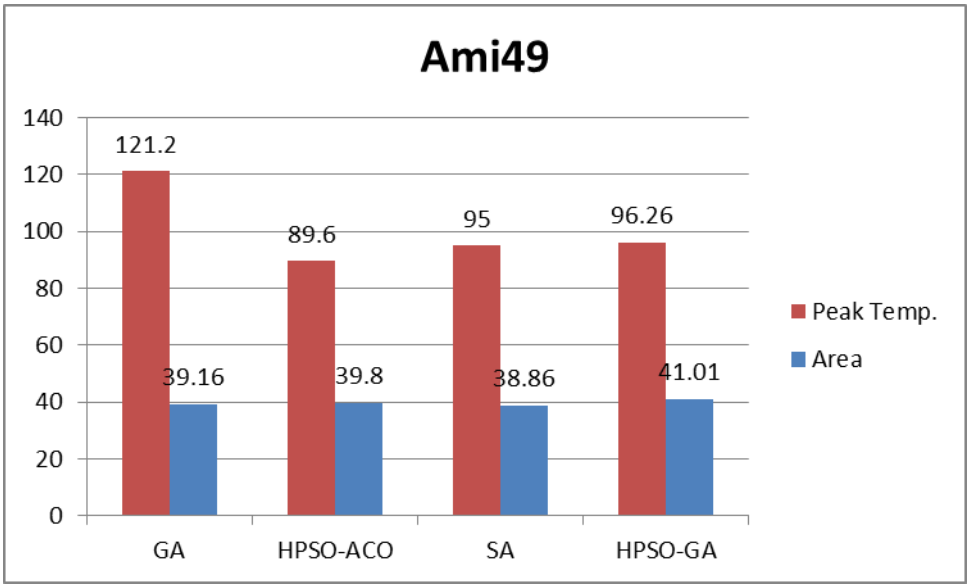

Figure 4.5: Peak Temp and Area Analysis of Various Optimization Methods for Ami49 Benchmark Circuit

5. CONCLUSION

Along with growing number of transistors, the chip area has been minimizing at the equal rate. Even though the current in every element of a modern microprocessor is very small, owed to very high element density, a lot of heat needs to be dissipated from a small surface area so that, modern microprocessors have very high power densities. Power density of the microprocessors is also growing with every new process generation since feature size and frequency are scaling speedily than the operating voltage. As a result, there has been an increase in maximum chip temperatures because power density directly converts into heat. Thermal aware floor planning can be used as one of the strategy for decreasing the maximum temperature of the chip. Several techniques show various results as hybridization of HS with PSO manages the problem of balancing global exploration and local misuse. The simulation results for MCNC benchmark circuit demonstrate that the proposed algorithm accomplish the optimal solution specifically for massive number of modules. Thermal aware floor planning algorithm based on Genetic Algorithms and combined area decreases the chip temperatures sufficiently while providing floor plans that are as compact as the conventional area-oriented techniques. Simulated Annealing Based Thermal-aware Floor planning can be used to solve the problem of thermal-aware floor planning, and can effectively reduce the chip's maximum temperature. PSO-GA algorithm for MCNC benchmark circuits demonstrated best and reasonable solution for the non-slicing placement of IP modules. GP (geometric programming) method is a cost-effective way.

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