Review of Low Power Transistor Single Phase Clocked Flip-Flop

[1]Kanchan Kumar, [2]Dr. Bharti Chourasia
[1]M.Tech Scholar, [2]Professor & HOD
[1]Department of Electronics & Communication,
[1]RKDF Institute of Science & Technology Bhopal, India.

Abstract : Flip-Flops (FFs) are basic storage elements used extensively in digital system designs. In the existing flip flop design 19 and more transistors were used to design. It increases the power consumption delay and time performance. So its need to reduce the above mentioned problems. This paper review of ultralow power true single phase clocking flip flop designs achieved using fewer transistors. The transistor count is reduced by using logic structure reduction scheme.

IndexTerms **–** FF, True single phase clock, Low Power, Transistor.

I. INTRODUCTION

A transmission-gate-based FF (TGFF) is arguably the most widely used FF currently. One possible drawback of this design is the excessive work load on the clock signal where complementary signals are required. The consequence is the presence of a considerable dynamic power even when the data switching activity is low. Recently, true single-phase clocking (TSPC) FF designs have been developed with the objective of lowering the clock signal loading. This is usually achieved through circuit simplification. Cross-coupled set– reset (SR) latches are used in lieu of the TG-based latch to support single-clock-phase operations.

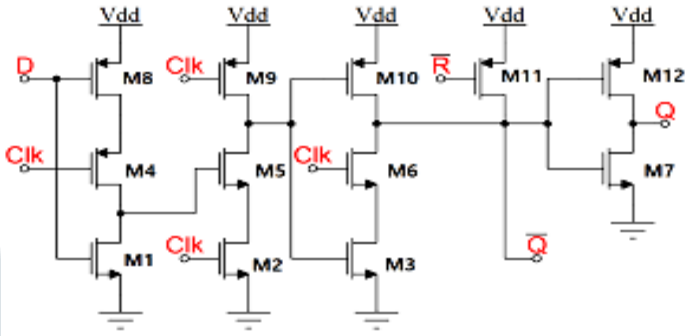

Figure 1: Basic TSPC based FF

The basic circuit element in dynamic logic is a dynamic (inverting) D-flip-flop. Normally such an element is designed as two tristate inverters following each other, where either the first or the second inverter is active. The flip-flop must never be transparent for data from input to output. The clock conveyance system (or clock tree, when this system shapes a tree) appropriates the clock signal(s) from a typical point to every one of the components that need it. Since this capacity is crucial to the task of a synchronous framework, much consideration has been given to the qualities of these clock signals and the electrical systems utilized in their conveyance. Clock sign are regularly viewed as basic control signals; be that as it may, these sign have some extremely unique qualities and traits.

Clock sign are normally stacked with the best fanout and work at the most elevated paces of any sign inside the synchronous framework. Since the information sign are given a fleeting reference by the clock flag, the clock waveforms must be especially perfect and sharp. Besides, these clock sign are especially affected by innovation scaling (see Moore's law), in that long worldwide interconnect lines become fundamentally progressively resistive as line measurements are diminished. This expanded line opposition is one of the essential purposes behind the expanding importance of clock conveyance on synchronous execution. At long last, the control of any differences and vulnerability in the landing times of the clock sign can seriously restrict the most extreme exhibition of the whole framework and make cataclysmic race conditions in which an off base information sign may lock inside a register.

Most synchronous digital frameworks comprise of fell banks of successive registers with combinational rationale between each arrangement of registers. The utilitarian necessities of the digital framework are fulfilled by the rationale stages. Every rationale stage presents postpone that affects timing execution, and the planning execution of the digital structure can be assessed with respect to the planning necessities by a planning examination. Regularly uncommon thought must be made to meet the planning prerequisites. For instance, the worldwide exhibition and nearby planning prerequisites might be fulfilled by the cautious inclusion of pipeline registers into similarly dispersed time windows to fulfill basic most pessimistic scenario timing limitations.

II. LITERATURE REVIEW

J. Lin, et al., [1] an ultralow-power true single-phase clocking flip-flop (FF) design achieved using only 19 transistors is proposed. The design follows a master-slave-type logic structure and features a hybrid logic design comprising both static-CMOS logic and complementary pass-transistor logic. In the design, a logic structure reduction scheme is employed to reduce the number of transistors for achieving high power and delay performance. Despite its circuit simplicity, no internal nodes are left floating during the operation to avoid leakage power consumption. In this design, a virtual VDD design technique, which facilitates a faster state transition in the slave latch, is devised to enhance time performance. In circuit implementation, transistor sizes are optimized with respect to the powerdelay product (PDP). A TSMC 90-nm CMOS process was selected as the implementation technology.

V. L. Le et al., [2] This work presents an extremely low-voltage and low-power single-phase-clocking redundant-transition-free flip-flop (FF), named change-sensing FF (CSFF). By utilizing a local change-sensing scheme for eliminating redundant transitions of internal clocked nodes, CSFF does not consume any dynamic power when there is no data activity. Measurement results from a test chip fabricated in 40-nm CMOS technology show that CSFF saves up to 90% power dissipation at 5% data activity without additional transistors compared to the conventional transmission-gate FF (TGFF). CSFF consumes only 0.138 fJ/cycle, which is 84% lower than that of TGFF, at 0.4 V and 10% activity. In addition to the significant improvement in power and energy efficiencies, CSFF also enhances performance and minimum operating voltage. The test chip measurement demonstrates successful operations of CSFF down to 0.19 V and the delay improvement of 37% compared to TGFF in the supply voltage range of 0.4-1 V.

M. Tsai et al., [3] In this work, an ultra-low-power true single-phase clocking flip-flop (FF) design is proposed. The design follows a master-slave-type logic structure and features a hybrid logic design comprising both static-CMOS logic and pass-transistor logic (PTL). In the design, a logic structure reduction scheme is employed to reduce the number of transistors for achieving low power and short delay performance. Comparing with the conventional transmission gate flip-flop (TGFF), the proposed flip-flop reduced power-delay product (PDP) by 62.3% under 12.5% data switching activity. Moreover, the circuit also achieves better hold time variation and is implemented with TSMC 90-nm CMOS technology.

X. Ji, et al., [4] A new true-single-phase-clock (TSPC) divide-by-2/3 prescaler is presented in this work. By merging one of the branches of the TSPC D flip-flops (DFF) and the modified dual-modulus control circuit, it is can realize a divide-by-2/3 prescaler with only 5-stage TSPC logic gates and fewer transistors compared with the conventional designs. Analysis shows that the load capacitance at output of the proposed prescaler can be much reduced, and the prescaler can operate as fast as a single TSPC flip-flop when working in the divide-by-3 mode. The proposed prescaler and the recently published works are both simulated in a low power 65nm CMOS process. From the simulation results, it is shown that the proposed divide-by-2/3 prescaler demonstrates the highest power efficiency among the referenced designs.

H. Ashwini et al., [5] True Single Phase Clock (TSPC) is a general dynamic flip-flop that operates at high speed and consumes low power. This work describes the design and performance analysis of 5 transistor (5T) TSPC D Flip-flop in comparision with different TSPC D Flip-flops such as; (i) MS-Negative-edge triggered TSPC D Flip-flop, (ii) Positive-edge triggered TSPC D Flip-flop with (a) 13 transistors, (b) 11 transistors, (c) 9 transistors, (d) 8 transistors, (e) 6 transistor TSPC D Flip-flops with respect to transistor density, power and delay. Finally Charge Pump with PFD is designed using 5T TSPC D Flip-flop method and functionality of the circuit is verified through simulation. A Layout of 5T TSPC D Flip-flop and Charge Pump with PFD are designed. DRC, ERC, LVS are verified with gpdk 180nm technology. All the circuits used in this work are designed and simulated using Cadence Virtuoso Platform, with gpdk 180nm CMOS process using 1.8V supply voltage.

S. Jia, et al., [6] A novel low-power and high-speed dual-modulus prescaler based on extended true single-phase clock (E-TSPC) scheme is presented. By restricting the short-circuit current in noncritical branchs, the design reduces the major source of power dissipation in E-TSPC scheme. The presented design enhances the maximum working frequency with shorter critical path and lower load capacitances. Simulation results in SMIC 40nm process show that compared with referenced E-TSPC based designs at least 61.2% (divide-by-2) and 41.1% (divide-by-3) reduction in power delay product (PDP) can be achieved by the proposed design.

E. Låte et al., [7] Nine D flip-flop architectures were implemented in 28nm FDSOI at a target, subthreshold, supply voltage of 200mV. The goal was to identify promising D flip-flops for ultra low power applications. The pass gate flip-flop was implemented using 49% of the S2CFF's area and was functional at the lowest operating voltage of 65mV in the typical process corner. At the targeted supply voltage of 200mV the racefree DFF gives the best functional yield of 99.8%. The flip-flops having the shortest D-Q delays were the PowerPC 603 and the transmission gate D flip-flop. These also had the lowest power delay products of 52.08aJ and 61.09aJ respectively.

S. Jia et al., [8] New design improvement aiming to reduce the power consumption of true single-phase clock-based dual-modulus divide-by-2/3 prescalers is presented. The first latch stages of TSPC FFs are merged to reduce power and capacitance. Also, a pass transistor is introduced to cut off short circuit current. Hspice simulation of the proposed scheme in 40nm process

demonstrates best power efficiency and power-delay-product among referenced designs. Besides, it shows comparable speed with extended TSPC prescalers.

Table 1: Summary of literature survey

Sr No	Author Name	Publish Details	Proposed Work	Outcome
1	V. L. Le	IEEE 2018	Presents an extremely low-voltage and low-power single phase clocking.	CSFF down to 0.19 V and the delay improvement of 37%
2	M. Tsai,	IEEE 2018	Design follows a master-slave-type logic structure	The circuit also achieves better hold time variation and implemented with TSMC 90-nm.
3	J. Lin,	IEEE 2017	This work proposes 19-transistor single-phase clocked	PDP improvement in the proposed design was up to 63.5% and the area saving was approximately 10%
4	X. Ji, X	IEEE 2017	A new true-single-phase-clock divide-by-2/3 prescaler is presented.	Highest power efficiency among the referenced designs.
5	H. Ashwini,	IEEE 2016	Design and performance analysis of 5 transistor TSPC D Flip-flop.	GPDK 180nm CMOS process using 1.8V supply voltage.
6	S. Jia	IEEE 2016	Presented design with shorter critical path and lower load capacitances.	TSPC based designs at least 61.2% (divide-by-2) and 41.1% (divide-by-3) reduction design.
7	E. Låte	IEEE 2015	The pass gate flip-flop was implemented using 49% of the S2CFF's area.	Supply voltage of 200mV. FF having the shortest D-Q delays.
8	S. Jia,	IEEE2014	True single-phase clock-based dual-modulus divide-by-2/3 presales is presented.	Best power efficiency and power-delay-product among referenced designs.

III. EXISTING TSPC

A. Latch Based TSPC

It is difficult to determine a Boolean condition speaking to a conduct of the exhibited S-R hook. The following yield Qn+1 is a component of Qn, S and R signals. Later in this book we will misuse those straightforward conditions so as to configuration improved clocked storage components. Displayed S-R hook can change the yield Q anytime.

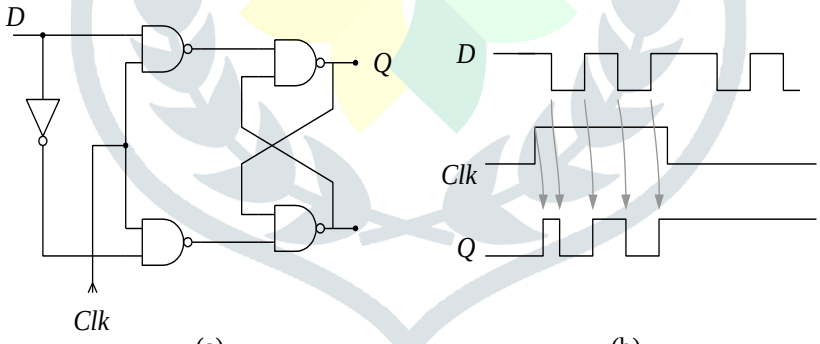

Figure 2: (a) Clocked D-Latch (b) timing diagram of clocked D-Latch

So as to make it perfect with the synchronous structure we will confine when Q can be influenced by presenting the clock signal which entryways S and R inputs. On the off chance that the information input D is associated with S, and the property of S-R lock, which makes S and R totally unrelated, is connected, the subsequent D hook is appeared in Fig.2 (a). The related planning graph of a D-Hook is appeared in Fig. 2 (b). The hook is straightforward amid the timeframe in which clock is dynamic, – for example expecting rationale 1 esteem.

B. True-Single-Phase-Clock (TSPC) latch

This latch was developed by combining two sections comprising of CMOS Domino and CMOS NORA rationale. Amid the dynamic clock (Clk=1), CMOS Domino assesses the contribution to a monotonic style (just a progress from rationale 0 to 1 is conceivable), while NORA rationale is pre-charging. On the other hand, amid dormant clock (Clk=0) Domino is being pre-charged (hence is non-straightforward) while NORA is assessing its information. The mix of NORA and Domino rationale stages results in a non-straightforward Ace Slave latch that requires just a single clock. Thus the name given to it was True-Single Phase Clock hook (TSPC).

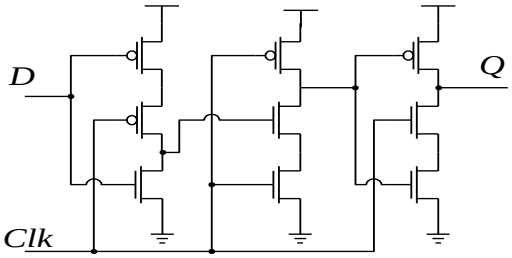

Figure 3: True Single Phase Clock (TSPC)

Latch introduced by Yuan and Svensson The task of TSPC latch is represented in Fig. 3. Whenever Clk=0, the principal reversal organize L1, is straightforward and the second half L2 of TSPC is pre-charged. In this manner, toward the finish of the half-cycle amid which Clk=0, the info D is available at the contribution of the Domino hinder as its supplement . At the point when the clock changes to rationale 1 (Clk=1), Domino rationale assesses and the yield either remains at rationale 0 or makes progress from 0 to 1 contingent upon the tested information esteem . This change can't be turned around until the following clock cycle. In actuality the primary inverter associated with the information goes about as an Ace Hook, while the second (Domino) arrange goes about as a Slave Lock. The exchange from the Ace Hook to the Slave latch happens while the clock changes its incentive from rationale 0 to rationale 1. Along these lines, TSPC carries on as a "main edge" activated Flip-Flop. It is additionally often called a Flip-Flop, however by the idea of TSPC activity this grouping is wrong.

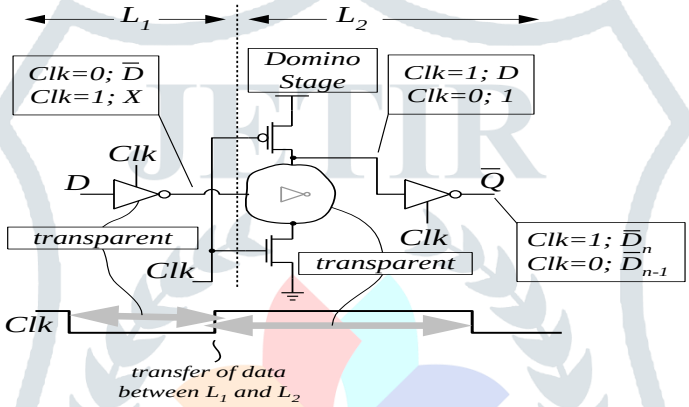

Figure 4: TSPC Latch operation

Because of its effortlessness and speed TSPC was an exceptionally mainstream method for actualizing clocked storage component. Be that as it may, TSPC displayed affectability to glitches made by the clock edges. This glitch is shown on the yield holding a rationale estimation of "1", while the info is accepting D=0.

IV. CONCLUSION

Clocking is one of the most critical parts of each processor, often determining its performance and largely impacting its power consumption. The clocking subsystem and clocked storage elements in particular are responsible for an increasingly substantial portion of the circuit design improvements needed to accommodate the continuing scaling trends with each processor generation. In this paper an overview of clocking and design of clocked storage elements is presented. It shows how different clocked storage elements work against each other. TSPC is one of the storage systems which are using most of digital circuit system.

REFERENCE

1. J. Lin, M. Sheu, Y. Hwang, C. Wong and M. Tsai, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 11, pp. 3033-3044, Nov. 2017.
2. V. L. Le, J. Li, A. Chang and T. T. Kim, "A 0.4-V, 0.138-fJ/Cycle Single-Phase-Clocking Redundant-Transition-Free 24T Flip-Flop With Change-Sensing Scheme in 40-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 10, pp. 2806-2817, Oct. 2018.
3. M. Tsai, P. Kuo, J. Lin and M. Sheu, "An Ultra-low-power True Single-phase Clocking Flip-flop with Improved Hold time Variation using Logic Structure Reduction Scheme," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, 2018, pp. 1-4.
4. X. Ji, X. Yan, G. Fengqi and Y. Guo, "High speed low power true single phase clock CMOS divide by 2/3 prescaler," *2017 International Conference on Circuits, Devices and Systems (ICCDS)*, Chengdu, 2017, pp. 80-83.
5. H. Ashwini, S. Rohith and K. A. Sunitha, "Implementation of high speed and low power 5T-TSPC D flip-flop and its application," *2016 International Conference on Communication and Signal Processing (ICCSP)*, Melmaruvathur, 2016, pp. 0275-0279.
6. S. Jia, Z. Wang, Z. Li and Y. Wang, "A novel low-power and high-speed dual-modulus prescaler based on extended true single-phase clock logic," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, QC, 2016, pp. 2751-2754.
7. E. Late, A. A. Vatanjou, T. Ytterdal and S. Aunet, "Comparative analysis of flip-flop architectures for subthreshold applications in 28nm FDSOI," *2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC)*, Oslo, 2015, pp. 1-4.

8. S. Jia, S. Yan, Y. Wang and G. Zhang, "Design of low-power high-speed divide-by-2/3 prescalers with improved true single-phase clock scheme," *2014 Asia-Pacific Microwave Conference*, Sendai, Japan, 2014, pp. 241-243.
9. A. Saha, D. Pal and M. Chandra, "Low-power 6-GHz wave-pipelined 8b x 8b multiplier," in *IET Circuits, Devices & Systems*, vol. 7, no. 3, pp. 124-140, May 2013.
10. Y. Hwang and J. Lin, "Low Voltage and Low Power Divide-By-2/3 Counter Design Using Pass Transistor Logic Circuit Technique," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 9, pp. 1738-1742, Sept. 2012.