A NOVEL IMPLEMENTATION OF LOW POWER AND FAST FULL ADDER DESIGN USING XOR AND XNOR GATES

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ABSTRACT

In current technology, VLSI design plays an important role in any Electronic industry, so advanced improvement is needed at every Logic design. In this paper XOR, XNOR based Full-adder design is implemented with 9T level, to overcome the limitations such as power consumption, delay and speed of operation for the Full adders designed using Earlier methods. This 9T based full adder design improves the power, delay and performance parameters. This investigation has been implemented using 25nm technology, full adder design with XOR, XNOR gates. This modern computational design for numerical computations is used to reduce the power and increases the speed of operation which has less delay of 1.67 ms at 5V and power consumption of 4.41mW at 1.5v input and power delay product is 16.8 at 1.5v input.

Index terms: Full adder XOR and XNOR, 25nm technology,Logic design,Numerical computations,Parameters,Power delay product.

1. Introduction

In this work, we look at numerous circuits for XOR or XNOR (XOR/XNOR) and simultaneous XOR and XNOR (XOR–XNOR) gates and offer new circuits for every of them. Also, we try to eliminate the problems current in the investigated circuits. “Afterward, with those new XOR/XNOR and XOR–XNOR circuits, we propose 1 bit FA systems. The rest of this paper is ready as follows. The circuits for XOR/XNOR and simultaneous XOR–XNOR are reviewed. The novel XOR/XNOR and XOR–XNOR circuits are proposed and the simulation outcomes of those systems are presented. Furthermore, these designs have more adavantages at serial communication like bit by bit transfer. 1 bit FA circuits are proposed and downsides of them are investigated, the transistor sizing techniques are first investigated, after which by using manner of supplying the right technique for transistor sizing, the circuits are simulated for strength, take away, and PDP parameters. The simulation effects are analyzed and in assessment concludes this work.

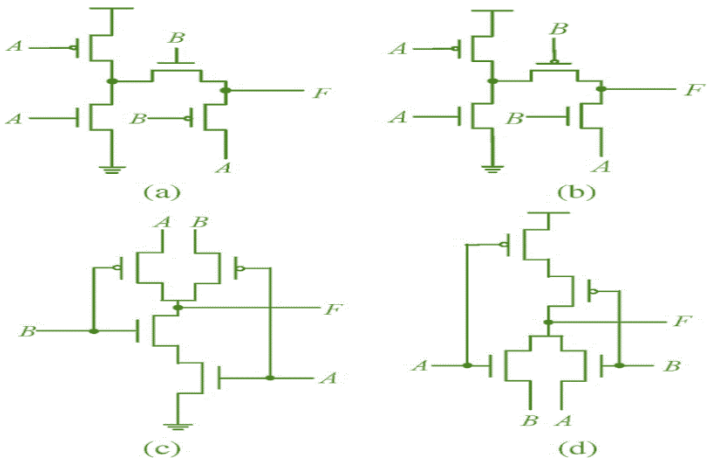

Figure: 1.Full-swing XOR/XNOR

Hybrid FAs are made from two modules, which incorporate 2-input XOR/XNOR (or simultaneous XOR–XNOR) gate and a dual 2X1 multiplexer (2-1-MUX) gate [3]. The XOR/XNOR gate is the fundamental customer of electricity inside the FA cell. Therefore, the electricity intake of the FA cellular may be decreased via the use of the maximum suitable designing of the XOR/XNOR gate. The XOR/XNOR gate has additionally many packages in the digital circuits design. Many circuits have been proposed to implement XOR/XNOR gate, in which a few examples of the maximum green ones are demonstrated in Fig. 1". The suggested general-swing XOR/XNOR gate circuit [16] designed through a double pass-transistor commonplace feel (DPL) style is shown. "This shape has eight transistors. The critical hassle of this circuit is the use of high energy consumption NOT gates on the critical course of the circuit, because of the fact the NOT gates need to force the output capacitance. Therefore, the scale of the transistors in the NOT gates should be extended to attain a lower in crucial route do away with. Furthermore, it motives the introduction of an intermediate node with a large capacitance. Of route, this means that the NOT gates pressure the output of the circuit via, for example, bypass transistor or TG. Therefore, the quick-circuit electricity and, therefore, the whole energy dissipation of this circuit are notably increased. Moreover, within the maximum tremendous PDP state of affairs, the important route put off may also be multiplied slightly. But the important direction of XNOR circuit is produced from a NOT gates and a pMOS transistor (P5) (pMOS transistor is slower than nMOS transistor). Therefore, to enhance the XNOR circuit speed, the dimensions of pMOS transistor (P5) and NOT gates have to be multiplied.

This structure has 9 transistors. The most important hassle of this circuit is using excessive energy consumption NOT gates at the crucial route of the circuit, due to the fact the NOT gates need to stress the output capacitance. Therefore, the size of the transistors within the NOT gates must be improved to achieve a decrease important course postpone. Furthermore, it motives the creation of an intermediate node with a huge capacitance. Of direction, which means the NOT gates pressure the output of the circuit via, for example, pass transistor or TG. Therefore, the quick-circuit electricity and, therefore, the overall power dissipation of this circuit are extensively advanced. Moreover, within the great PDP state of affairs, the crucial course postpones can also be prolonged slightly. This circuit is primarily based on the PTL good judgment style, whose removal and strength intake are higher than the circuit depicted in above figure1. The handiest hassle of this form is the usage of a NOT gates at the critical course of the circuit. But the essential route of XNOR circuit is made out of a NOT gates and a pMOS transistor (P5) (pMOS transistor is slower than nMOS transistor). Therefore, to enhance the XNOR circuit pace, the size of pMOS transistor (P5) and NOT gates need to be extended".

3. Related methods

In the ultra-modern years, the simultaneous XOR–XNOR circuit is drastically applied in hybrid FA structures [3], [9]. Commonly, inside the "hybrid FAs, the XOR–XNOR signals are related to the inputs of two-1-MUX as choose out strains. Therefore, two simultaneous alerts with the same put off are important to keep away from gadget faults inside the output nodes of the FA. This circuit is primarily based at the

CPL common sense style that has been designed by way of the usage of ten transistors. In this shape, the outputs had been driven best via nMOS transistors, and hence, pMOS transistors are linked to outputs (XOR and XNOR) as go-coupled to get better the output-degree voltages.

One hassle of this XOR–XNOR circuit is to have the comments (bypass-coupled shape) on the outputs, which increases the postpone and quick-circuit energy of this form. Therefore, to mitigate the imposed dispose of, the scale of transistors ought to be improved. Another drawback of this form is the existence of two NOT gates in the crucial route. This "zero" on XOR prices the XNOR output to VDD through transistor P3. Therefore, the critical path of this circuit is bigger than that of the circuit. Also, on this shape, the short-circuit modern-day may be passed through the circuit while the input is modified from AB = 01 to AB = 00. When the inputs are in-united states of America AB = 01, good judgment "1" is surpassed via the transistors N2, N3, and P2 to XOR output and accurate judgment "0" is surpassed via the transistor N4 to XNOR output. When the inputs change to AB = 00, all transistors turn into OFF besides transistors N2 (thru the enter A) and P2 (through the XNOR output, which has no longer modified now). Therefore, the fast-circuit contemporary will pass from the transistors P2 and N2. If the quantity of current being sourced from the transistor P2 is bigger than that of present-day being sunk from the transistor N2, the fast-circuit present day will remain drawn from VDD and will by no means switch XOR and XNOR output. This scenario additionally takes location while the entry is changed from AB = eleven to AB = 10 and influences the right functioning of the circuit". To grantee, the right operation of this circuit, the ON-nation resistance of transistors P2 and P3 need to no longer be smaller than that of transistors N2 and N5 (RP2 > RN2, RP3 > RN5), respectively. Furthermore, this form will be very touchy to the method model; if the dimensions of transistors is modified, the circuit might not characteristic well. In [7] and [13], complete-swing XOR–XNOR gate with the nice six transistors is proposed. "The complimentary remarks transistors (N3 and P3) repair the susceptible logic in the output nodes (XOR and XNOR) whilst the inputs same to AB = 00, eleven. However, this circuit suffers from the excessive worst-case delay, because of the truth even as the inputs exchange from AB = 01, 10 to AB = eleven, 00, the outputs attain its final voltage price in two steps. To make clear the hassle, at the same time as the inputs equal to AB = 10, commonplace experience "1" and suitable judgment "zero" are surpassed through the N2 (XOR output) and P2 (XNOR output) transistors, respectively. By changing the input mode to AB = 11, the transistors P1 and P2 are growing to become OFF (XOR node is to start with excessive impedance) and susceptible common feel "1" (VDD−Vthn) is exceeded via the transistors N1 and N2 to the XNOR output. The susceptible, not unusual feel "1" on the XNOR turns ON the remarks N3 so that the XOR output is pulled right down to vulnerable common sense "zero," which this prone common sense "0" turns ON the remarks P3. Eventually, effective remarks is made and the XNOR and XOR outputs could have sturdy commonplace feel "1" and not unusual experience "0," respectively. This slow reaction problem is worse inside the low-voltage operation And moreover will increase the fast-circuit present-day [when one of the outputs (XOR or XNOR) is high impedance and circuit feedback has not yet acted completely, the short-circuit current is passing through the circuit]. Also, if the scale of transistors in this circuit isn't always well decided on, the circuit may not be efficaciously operated. Thus, this form may be very sensitive to technique–voltage–temperature (PVT) versions.

3. Proposed method

The advantages of this structure are nicely the use of capability, following output, and robustness against transistor sizing and deliver voltage scaling. The essential hassle of this circuit is the shape of comments that imposes more parasitic capacitance to the XOR and XNOR output nodes. Thus, postpone and electricity intake extensively will increase.

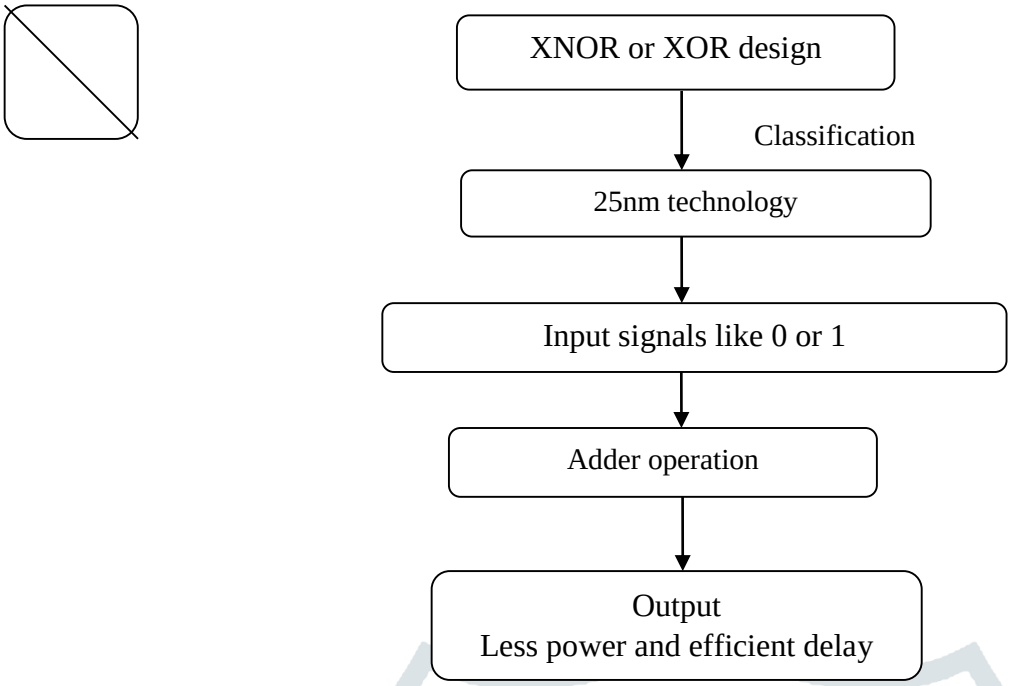

Figure: 2 block diagram of XNOR XOR Adder design

The Combination of XOR and XNOR circuits of figure will bring about simultaneous XOR–XNOR gates. These new systems should have all the advantages and downsides in their XOR/XNOR circuits".

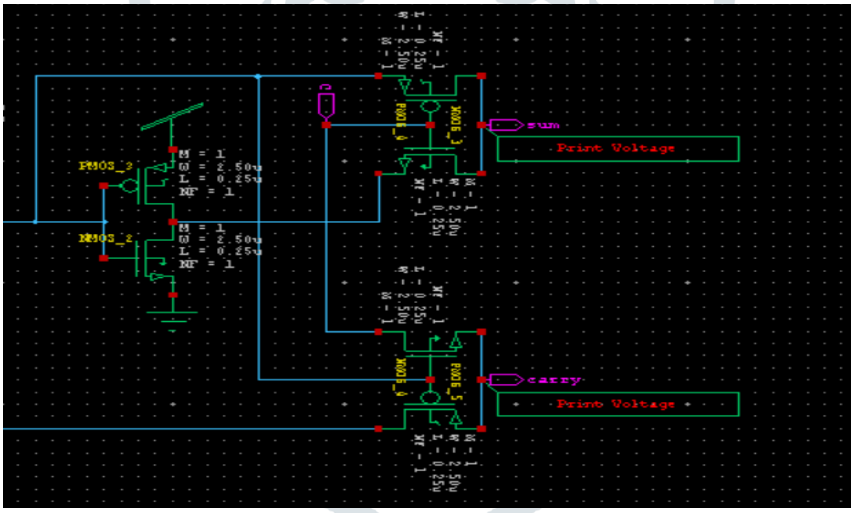

Figure: 3. Proposed full-swing XOR/XNOR gate.

The nonfull-swing XOR/XNOR circuit of Fig. 3 is inexperienced in terms of energy and postponement. "Furthermore, this shape has an output voltage drop problem for the best one to go into a logical charge. To resolve this hassle and offer the greatest structure for the XOR/XNOR gate, we advocate the circuit proven in Fig. 3. For all viable enter combinations, the output of this form is complete swing.

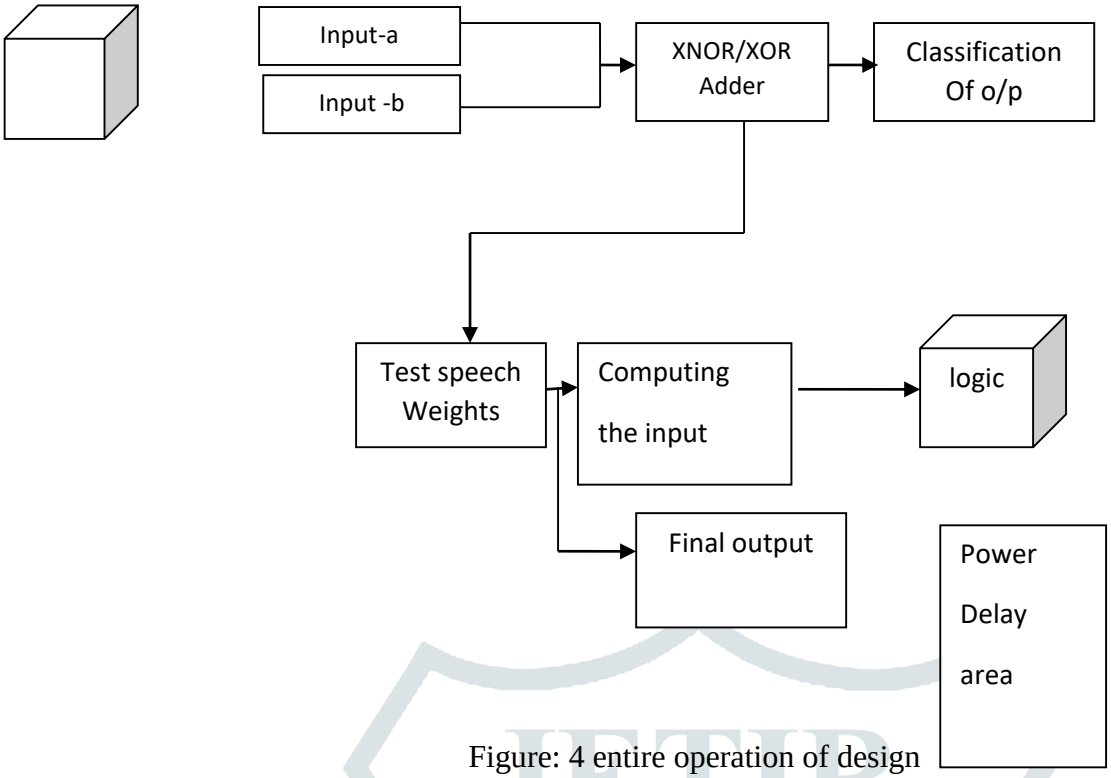

Figure: 4 entire operation of design

The proposed XOR/XNOR gate does not have NOT gates at the essential direction of the circuit. Thus, it's going to have a decrease eliminate and genuine usage of the capability in assessment with the systems of Fig. 4 Although the proposed XOR/XNOR gate has one greater transistor than the form of Fig. 4, it demonstrates decrease power dissipation and higher velocity. The input A and B capacitances of the XOR circuit tested in above picture aren't symmetric, because this kind of must be associated with the entry of NOT gates and some other need to be connected to the diffusion of nMOS transistor. Furthermore, the enter capacitances of transistors N2 and N3 aren't the same in the maximum best situation (minimal PDP). Also, the order of input connections to transistors N2 and N3 will now not have an effect on the man or woman of the circuit. Thus, it's far better to connect the input A, which is likewise connected to the NOT gates, to the transistor with smaller enter capacitance. By doing this, the enter capacitances are greater symmetrical, and as a result, the dispose of and power consumption of the circuit can be reduced.

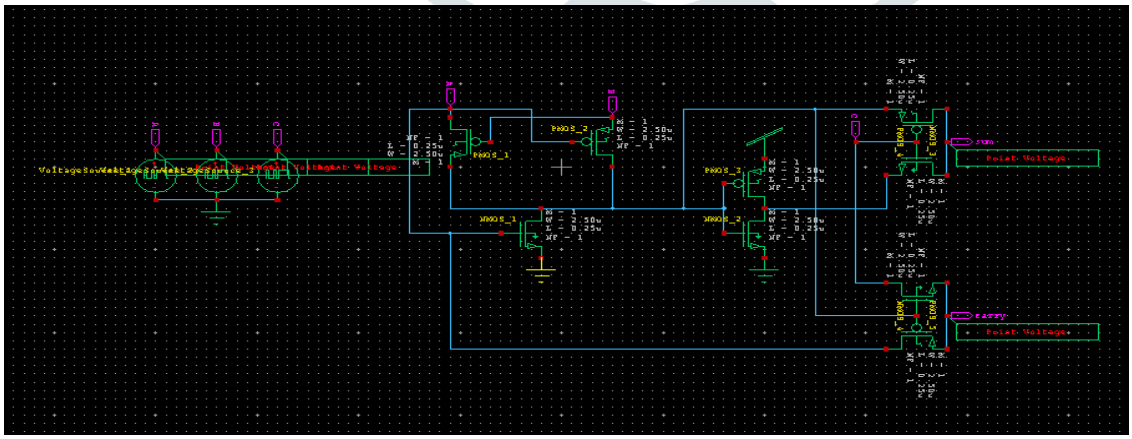

Figure : 5.implemented design 25nm

To make clear which transistor (N2 or N3) has large input capacitance, allow us to consider the condition that the inputs alternate from AB = 00 to AB = 10. In this case, because the RC model of XOR is shown in above the transistor N2 is using simplest the capacitance of node X from GND to VDD − Vthn [Fig. 5], so it'll no longer require a decrease RN2".

"The proposed XOR/XNOR and simultaneous XOR–XNOR systems had been compared with all the above-said systems. The simulation outcomes at TSMC sixty 5-nm generation and 1.2-V electricity deliver voltage (VDD) are tested in below section. The enter sample is used as all feasible enter combos were covered. The most frequency for the inputs turned into 1 GHz and four× unit-length inverter (FO4) grow to be linked to the output (as a load). The length of transistors has been selected for max PDP by means of using the proposed transistor sizing method, wherein the proposed technique is probably described below. The most satisfying length of transistors for each XOR/XNOR and XOR–XNOR circuits are expressed in below explanation. In the output upward thrust and fall transition, the put off is calculated from 50% of the enter voltage level to 50% of the output voltage degree. The PDP may be calculated with the aid of multiplying the worst-case postpone with the resource of the commonplace strength intake of the principle circuit.

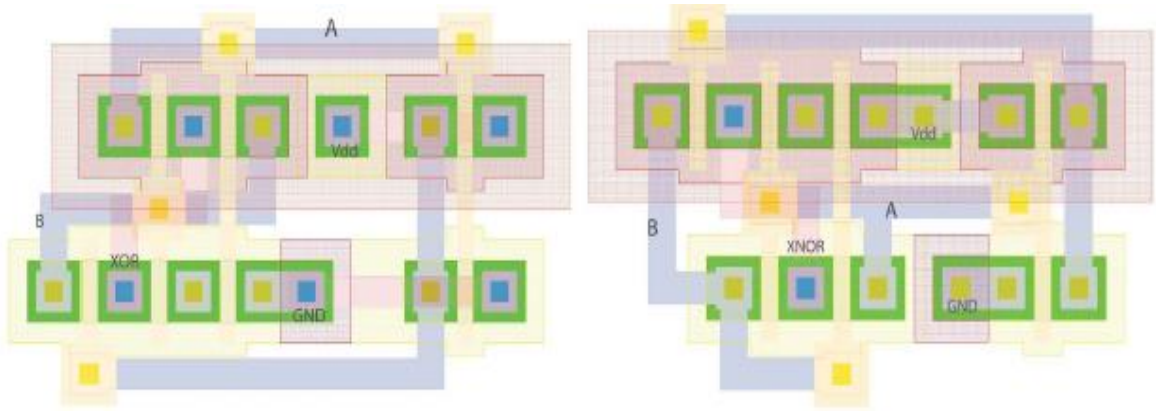

Figure: 6. XOR and XNOR layouts

The consequences indicate that the performance of the proposed XOR/XNOR and simultaneous XOR–XNOR systems is higher than that of the in comparison structures. The proposed XOR and XNOR circuits [Fig. 6] have the bottom PDP and delay, respectively, in comparison with one-of-a-kind XOR/XNOR circuits. Also, the postpone of these proposed circuits will be very near together that prevents the advent of glitch on the following diploma. The removal, energy intake, and PDP of the XOR and XNOR circuits of Fig. 6 are nearly identical, due to having the same structures. As mentioned earlier and consistent with the received outcomes, the XOR schematic has a higher overall performance than its XNOR circuit. The proposed circuit for simultaneous XOR–XNOR has better efficiency in all 3 calculated parameters (delay, electricity dissipation, and PDP) whilst it's miles as compared with different XOR–XNOR gates. The proposed XOR–XNOR circuit is saving nearly sixteen.2%–eighty five.Eight% in PDP and its miles 9%–83.2% faster than the opposite circuits. The circuits of Fig6. above have the very immoderate cast off due to its output comments (which have the gradual response trouble)".

In practice, the riding functionality of VLSI circuits is degraded because of the arrival of the parasitic capacitors and resistors during the fabrication, as well as growing the edge voltage of transistors over time, however, the output buffer improves this case. This offers the 1/3 proposed hybrid FA with buffers at the Sum and Cout outputs and it's far made with 9 transistors. There are XOR–XNOR gate, one 2-1-MUX gate, and NOT gates at the crucial course of HFA-B-11T. The output NOT gates is used to save you the riding output nodes with the useful resource of the inputs of the circuit and also lessen the resistance from the output node of the circuit to the assets (VDD and GND). The electricity consumption and removal of HFA-B-11T are extra than that of HFA-20T and HFA-17T FAs. It indicates any other proposed hybrid FA with new buffers (HFA-NB-26T), wherein they may be located in the information inputs of 2-1-MUX gates in the vicinity of putting the buffers inside the outputs. If the enter indicators of A and C are produced via the buffer, then for all viable input combos, the Sum and Cout outputs aren't driven through the use of the inputs of the circuit. To do that painting, 3 additional NOT gates are sufficient, due to the fact there was already the A signal and maybe made the buffered A signal with an in addition NOT gate." So the HFA-NB-11T FA circuit is made through 26 transistors. The statistics input nodes of two-1-MUXs attain to their final charge (GND or VDD) in advance than the XOR and XNOR alerts are

produced. Thus, the essential direction of HFA-NB-11T includes an XOR–XNOR gate and a 2-1-MUX Gate and its put off is reduced in contrast with the HFA-B-11T.

The use of the functionality of the HFA-NB-11T is barely a terrific deal less than that of HFA-B-11T due to the gift two-1-MUX gate among the buffer and the output node [which increases the resistance from the output node to the sources (VDD and GND)]. "The circuits of HFA-11T and HFA-9T were designed in order that the great deal much less range of transistors has been used. To produce the output Sum signal, the XOR, XNOR, and C signs are tremendous used so no extra NOT gates needs to generate the C sign, even as if the C sign is also used to supply the Sum output, then XOR and XNOR signs will no longer force the Sum output thru the TG multiplexer, however, quality they may be related to the records pick out lines of two-1-MUX. So the capacitance of XOR and XNOR nodes end up smaller, and the elimination of the circuit can be advanced. Another trouble of this approach is that it attempts to lessen the postponement in preference to reducing the PDP of the circuit, whilst our number one goal is to lessen the PDP of the circuit. In [18], each other technique for transistor sizing is proposed, which is nearly the perfect technique, and its basic overall performance is higher than the previous method. In the approach [18], much like the method [9], all transistors of the circuit and dependencies between them have now not been taken into consideration on the equal time. Also, the final cease end result is exceptionally depending on the initial size of the transistors. Of route, those strategies lose their precision in the pick of lowering the simulation time. 2) Proposed Method for Transistor Sizing: Results:"

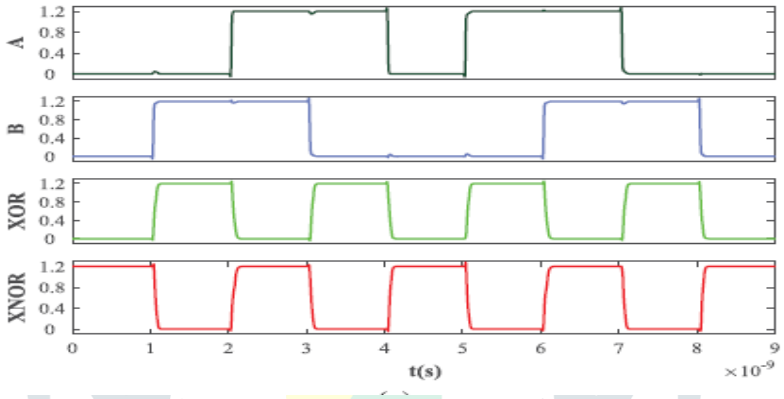

Figure: 7. Time domain simulation

The abovementioned strategies do no longer don't forget the dependence of transistors and, therefore, do no longer have proper accuracy. There are first-rate methods to optimize a feature, wherein this form of technology is particle swarm optimization (PSO). The circuits of Fig. 7 (named HFA-11T and HFA-9T, respectively) had been created by the use of using the above concept to HFA-9T and HFA-11T, respectively. It is expected that the strength intake and dispose of the HFA-11T and HFA-9T FA circuits are a lot a good deal much less than that of HFA-11T and HFA-9T, respectively (in spite of having extra transistors), because of the plenty less capacitance of XOR and XNOR nodes. Also, with the aid of consisting of the C sign, the riding functionality of HFA-11T and HFA-9T may be higher than that of HFA-11T and HFA-9T, respectively.

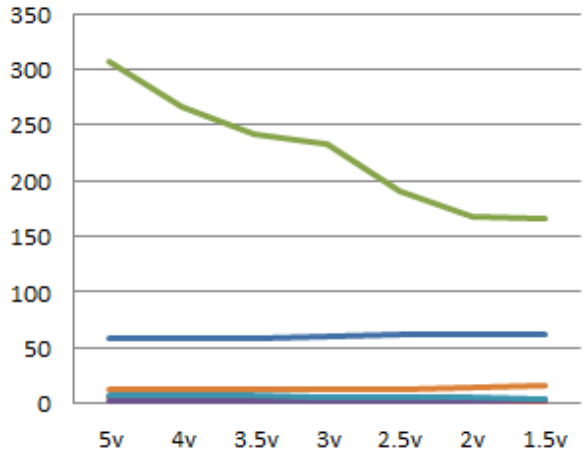

Figure: 8 PDP VS DELAY

Therefore, choosing the perfect method of transistor sizing, before obtaining the important parameters of the circuit, is vital. There are several techniques for transistor sizing [9] . 1) Review on Transistor Sizing Methods: Shams et al. [9] present the method for transistor sizing. Since this approach is quite simple and rapid, the simulation time for optimizing the circuit is lots of decreased shown in Fig. 8.

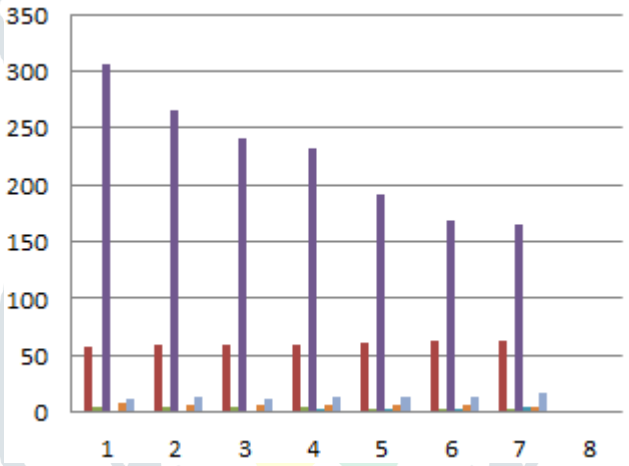

Figure: 9.PDP vs. Designs

The transistor sizing approach, which incorporates reducing or enlarging the width of transistors, is an effective and effective tool for optimizing the VLSI circuits and has for use inside the layout technique of immoderate-performance circuits. 9.

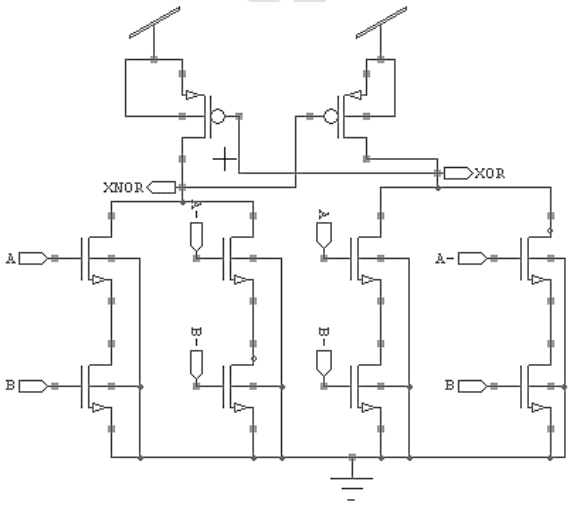

Figure: 10. various transistors design

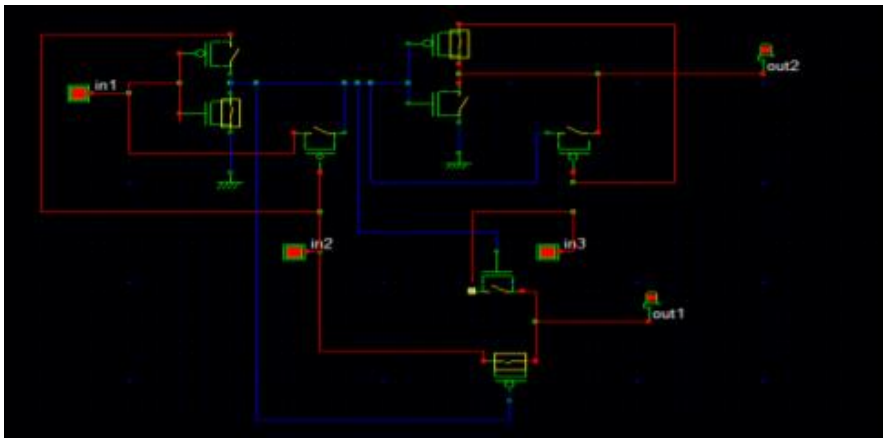

Figure: 11. Layout design of 9T

In pc technological information, the PSO set of rules is a numerical computation method that optimizes a function iteratively. It is attempting to suggest a better answer with the attention of the acquired value of the feature. It solves a problem by means of the usage of giving the candidate answers, which is referred to as the particles, and transferring that debris to the great-appeared function inside the seek-place consistent with smooth mathematical components (7). If a higher position is located in the are looking for a location with the aid of the use of other particles, it is up to date as the superb-regarded function. Eventually, the swarm actions closer to the terrific solution. The PSO set of guidelines is turning into famous because of its simplicity of implementation and capability to unexpectedly converge to an awesome solution shown in Fig. 10 and 11.".

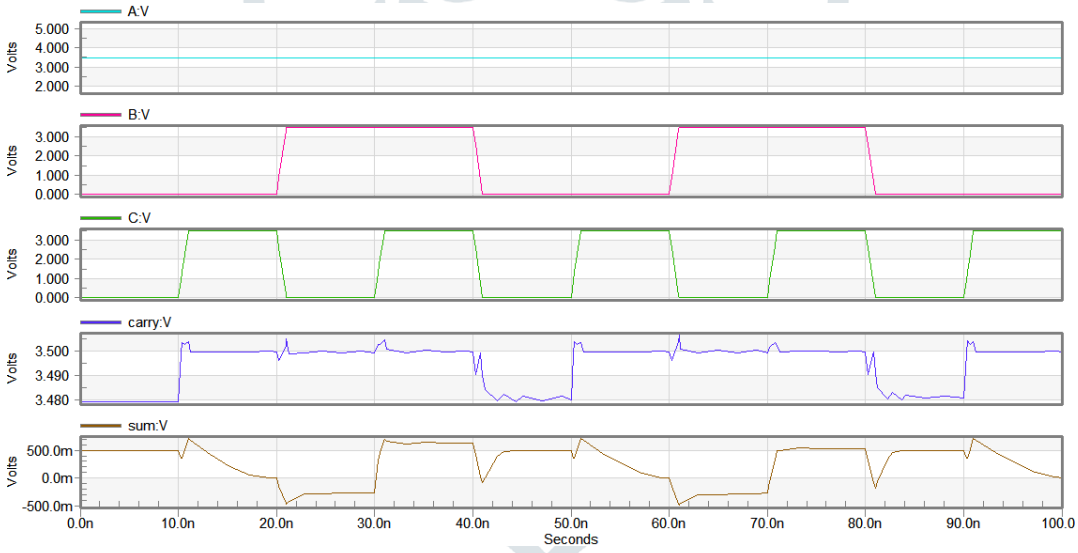

Figure: 12. Time-domain simulation results (waveform) of the proposed FA.

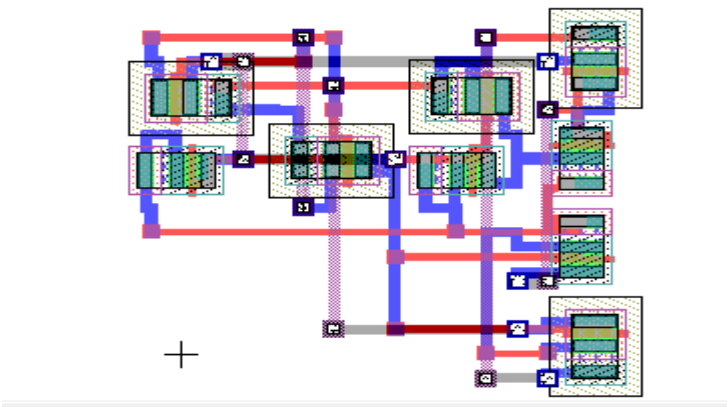

Figure :13 layout for implemented design

Table : 1 Simulation Results(DELAY IN ps),PDP IN aj, FOR FA CIRCUITS IN 25-nm TECHNOLOGY

vdd(V)	HFA 22T DELAY(s)	HFA 22T POWER(mw)	HFA 22T PDP(aj)	HFA 9T DELAY(s)	HFA 9T POWER(mw)	HFA 9T PDP(aj)
5v	57.5	5.32	306.43	1.67	7.432	12.4
4v	58.6	4.53	265.91	1.78	7.211	12.8
3.5v	59.09	4.08	241.12	1.84	6.59	12.12
3v	59.5	3.9	232.05	2.1	6.17	12.95
2.5v	61.29	3.12	191.25	2.23	5.98	13.33
2v	61.89	2.71	167.74	2.49	5.51	13.71
1.5v	62.09	2.66	165.18	3.81	4.41	16.8

The optimization techniques, such as deciding on the most reliable circuit shape for the meant reason, the precise top judgment style, and transistor sizing, were implemented for boosting the performance of circuits. The fundamental trouble of this approach is that the transistors worried within the crucial direction are most effective considered, while in a circuit, all (OFF or ON) transistors are worried inside the critical route put off of the circuit due to the fact all of them affect the power dissipation and nodes capacitance of the circuit (and additionally PDP). Therefore, the more appropriate technique is to do not forget all transistors of the circuit on equal time, although they'll be OFF shown in Fig. 13 and table:1

Conclusion:

In this work 9T based XOR / XNOR full adder design is implemented, which is used at many Low Power Vlsi applications. Existing methods that are designed based on Nand gates, Nor gates etc... have certain drawbacks viz. more power consumption and delay. These limitations can be overcome by using Xor and Xnor 9T level logic gates, Implemeted Full adder which has less delay of 1.67 ms at 5V and power consumption of 4.41mW at 1.5v input and power delay product of 16.8 at 1.5v input.Therefore implemented desing is most useful at every applications in VLSI adder operations.

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