DESIGN AND IMPLEMENTATION OF TESTABLE REVERSIBLE SEQUENTIAL CIRCUITS

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ABSTRACT: The structure of testable consecutive circuits by two vectors utilizing moderate rationale. The proposed consecutive circuits dependent on preservationist rationale outmaneuver the customary circuits constructed utilizing traditional gates as far as testability. Any consecutive circuits dependent on traditionalist rationale can test for stuck at 0 and stuck at 1 issue by utilizing two vectors 0 and 1. The structure of testable master-slave D flip-flop, Double Edge activated flip lemon(DET) flip-flop utilizing two vectors 0and 1 are introduced. The significance of the proposed work is that we are structuring reversible successive circuits appropriate for testing. Consequently both moderate rationale and reversible rationale is utilized. In the proposed work.We structure a reversible successive circuit utilizing Fredkin gate. Fredkin gate is the main reversible gate which bolsters both moderate and reversible rationale and furthermore having less quantum delay.

KEYWORDS: Conservative logic, Reversible logic, Fredkin gate, D Flip Flop.

I.INTRODUCTION:

Conservative logic could be a logic family that displays the property that there area unit equal numbers of 1s within the output as in that the input. Conservative logic it zero internal power dissipation that is an extra advantage to the present projected Technique. Changeability is that the property that shows matched mapping between input and output vector .Therefore the vector of input states. May be continuously reconstructed from the vector of output states. Reversible logic does not permit fan-out to occur .It means that for every input corresponding output is created. Therefore for one input multiple outputs doesn't seem to be possible.

This can be strictly restricted by reversible logic which ends up testing to be simple.Conservative logic is additionally known as reversible conservative logic once there is one to one mapping between input and output vectors along side the property that there area unit equal number of 1 s within the output as within the inputs.If a circuit is intended in associate in nursing irreversible manner then there will be a touch of knowledge lost and which ends up in chilling. The road of aaproach offered by conservative logic avoids variety of dead ends that the area unit found in ancient models and parades contemporary views.

According to landauer principle one little bit of info lost is equal KTln2 joules of energy lost,wherever K is the physical constant and T is the temperature during which operation is performed. Thus to scale back this energy lost fully we have a tendency to use reversible logic and additionally reversible logic fully reduces chilling. Reversible logic has received nice attention within the recent years because of their ability to scale back the heat dissipation that is the main demand in low power VLSI style.

Reversible logic takes care of Fan out draw back. It supports the method of running the system each forward and backward. The projected technique can beware of the fan-out at the output of the reversible latches and additionally disrupt the feedback to form them appropriate for take a look at solely 2 test vectors.all 0s and every one 1s. by this manner we will simply take a look at the circuit with ease in alternative words once circuit is dead in traditional mode. Feedback are going to be gift as a result of to complete the additional inputs. And equally once dead in take a look at mode its feedback is discontinuos and therefore the circuit is tested for stuck at faults. Thus projected technique is split into 2 modes traditional and take a look at mode. The projected technique is extended toward the planning of 2 vectors testable for DET flip-flops.

Reversibility in computing implies that no information regarding the machine states will ever be lost. Thus we will recover any past stage by computing backwards or un-computing the results. This is often termed as logical changeableness. The benefits of logical changeableness will be gained solely once using physical changeableness is much unacceptable. A circuit is claimed t be reversible if the input vector will be unambiguously recovered from the output and output assignments. That is not solely the outputs will be unambiguously determined from the inputs. However additionally the inputs will be regained from the outputs.

II.REVERSIBLE LOGIC GATES

A reversible gate is associate in nursing n –input n-output logic device with matched mapping. This helps to search out the outputs from the inputs and additionally the inputs are unambiguously regained from the output. In reversible circuits direct fan out is not allowed as one to many thought is not reversible. A reversible circuit ought to be designed mistreatment marginal range of reversible logic gates. From the approach of reversible circuit style there are several factors to de ide the quality and performance of circuits.

1.The quantity of reversible gates(N):The number of reversible gates employed in circuit.

2.The range of constant inputs(CI): This refers to amount of inputs that are to be preserved constant at either zero or one so as to provide the given logical operation

3. The range of garbage outputs(GO): This refers to the amount of unused outputs during a reversible logic circuit. Additionally the rubbish outputs as these are terribly essential to realize changeability.

4.Quantum price(QC): this refers to be price of the circuit in terms of the price of a primitive gate.

There are completely different reversible gates and that they are

- NOT Gate
- Feymann gate
- Fredkin gate
- Toffoli gate
- Peres gate
- Sayem gate
- Double feymann gate

In this toffoli gate and fredkin gate are universal gates.universal gates suggests that mistreatment these gates any sort of mathematical expression is obtained (i.e) any sort of circuits are designed. Not gate is the basic reversible gate. Feymann gate may be a 2*2 one through reversible gate. The input vector is I(A,B) and output is O(P,Q). The outputs are outlined by P=A,Q=B, R=AB⊕C. NOT gate is associate in nursing electrical converter that inverts the input. likewise different gates at glorious during this we tend to choose fredkin gate primarly as a result it is compatible with each reversible and conservative logic.

A. FREDKIN GATE:

Fredkin gate is a 3*3 entry way appeared in Fig 1.the information vectors is I(A,B,C) and the yield vector is O(P,Q,R). The yield is characterized by P=A, Q=A′B $\oplus$ AC and R=A′C $\oplus$ AB. Quantum cost of a fredkin gate is 5. It is utilized in preservationist,switch,collaboration and reversible rationale. Because of its properties fredkin gate is utilized for planning consecutive circuit and furthermore it decreases postponement and zone utilized for structuring a circuit. It is reversible and conservative in nature(i.e) it has exceptional information and yield mapping and furthermore has indistinguishable number of 1's in the yields from the source of information ,depends upon the main information which is a control signal yield are delivered. In the event that the main info is 1 methods, at that point the other two information sources are recovered as yields. On the off chance that the info is 0, at that point the other two data sources are swapped and delivered as yields.

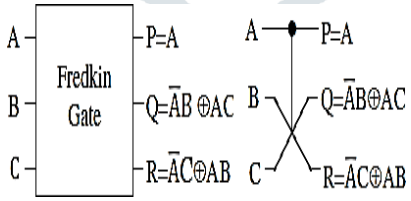

Fig1(a): fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig1(b) : fredkin gate truth table

B.RELATED WORK: Any nanotechnology having utilizations of reversible rationale, for example, in view of nano-CMOS gadgets, low force atomic QCA registering, or NMR-based quantum processing, all are powerless against high blunder rates because of transient shortcomings. As to this paper on reversible successive circuits, the model of reversible consecutive circuits is tended to in the different fascinating commitment with regards to which the structures are improved as far as different capacities, for example, the quantity of reversible entryways, quantum cost, trash yields, delay and so forth. To the best of our comprehension, the disconnected testing of flaws in reversible consecutive circuits isn't tended to in the writing. In this paper, we present the structure of reversible successive circuits that can be tried by just two test vectors, all 0's and all 1's, for any unidirectional stuck-at-flaws. By giving all the contributions as 1 we test for stuck-at-0 shortcoming and comparably on the off chance that we give all the contribution as 0 methods we test for stuck-at-1 deficiency

III.PROPOSED SYSTEM:

A.DESIGN OF TESTABLE REVERSIBLE D LATCH:

The characteristic equation of the D latch can be written as Q+ = D • E + .E • Q. In the proposed work, enable (E) refers to the clock and is used conversely in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is Q+ = D. While, when E = 0 the latch preserves its previous state, that is Q+ = Q. In Fig. 2(a) reversible D latch is shown and its characteristic equation is reverse of D latch characteristic equation but that design cannot be tested only by two vectors because of feedback. Some misinterruptions may occur.So in our proposed work we will cascade two Fredkin gate and Q output of one gate will follow the other. And it has two control signals C1 and C2 by which the design works. In normal mode which is shown in Fig. 2(b) works when C1 and C2 is given as 0 and 1 and the circuit works as a D latch without any fan-out problem. In test mode which is shown in Fig. 2(c) and (d) works when C1 and C2 is given as 1 and 1 or 0 and 0, the circuit disrupts the feedback and checks for stuck-at-0 or stuck-at-1 fault.

B.DESIGN OF TESTABLE NEGATIVE ENABLE D LATCH:

A negative enable reversible D latch will pass the input D to the output Q when E = 0; otherwise preserves the previous state. The characteristic equation of the negative enable D latch is Q+ = D•E +E•Q. This characteristic equation of the negative enable reversible D latch can be mapped on the second output of the Fredkin gate. The next Fredkin gate in the design take cares of the FO. This Fredkin gate in the design also helps in making the design testable by two test vectors, all 0's and all 1's, by breaking the feedback based on control signals C1 and C2 as illustrated above for positive enable D latch. The negative enable D latch is helpful in the design of testable reversible master-slave flip flops. This is because as it can work as a slave latch in the testable reversible master-slave flip-flops in which no clock inversion is required.

C.DESIGN OF TESTABLE MASTER-SLAVE FLIP-FLOPS:

We have proposed the design of testable flip-flops using the master slave strategy that can be tested for any stuck-at faults using only two test vectors, all 0s and all 1s. Master latch will be positive enabled Fredkin gate based D latch and slave latch will be negative enabled Fredkin gate based D latch. Fig 4 shows the master-slave D flip flop. There are 4 control signals

sC1, sc2, mC1 and mc2. mC1 and mC2 control the master latch and similarly sC1 and sC2 control the slave latch. When signals are given as 0 and 1 it will work in normal mode and avoid fan out problem. If the signals are given 0 and 0 it will disrupt the feedback and test the circuit for stuck-at-1 fault. Suppose if the signals are given as 1 and 1 then it will test the circuit for stuck-at-0 fault. Here Master controls the slave latch. If signal is given as 1 master latch works and vice-versa slave latch will work.

D.DESIGN OF TESTABLE REVERSIBLE DET FLIP-FLOPS:

In the master-slave flip-flop, it does not sample the data at both clock edges; instead it waits for the next rising edge of the clock to work as a master or slave latch. In order to overcome the abovementioned problem, researchers have introduced the concept of DET flip-flops which sample the data at both the edges. Thus, DET flip-flops can sample and receive two data values in a clock period thus frequency of the clock can be reduced to half of the master- slave flip-flop while maintaining the same data rate. The half frequency operations make the DET flip flops very much useful for low power computing as frequency is equal to power consumption in a circuit. It is designed by connecting the two latches, via, the positive enable and the negative enable in parallel rather than in series. The 2:1 Multiplexer at the output transfer the output from one of these latches which is in the storage state (is holding its previous state).

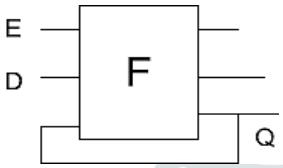

Fig2(a). reversible D latch

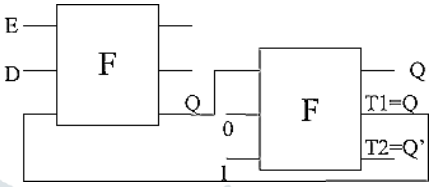

FIG 2(b): normal mode

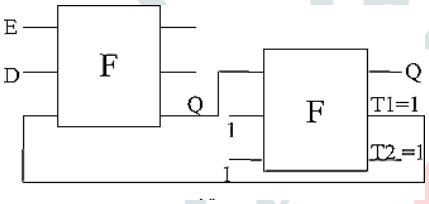

Fig2(c.) test mode for stuck-at-0 fault

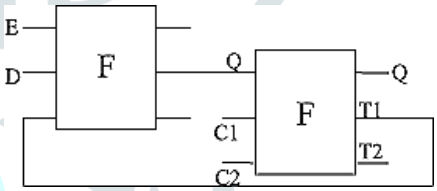

Fig2(d). test mode for stuck-at-1 fault

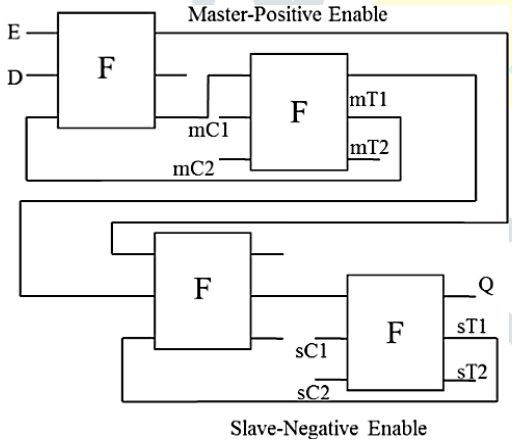

Fig3. Master-slave D flip-flop

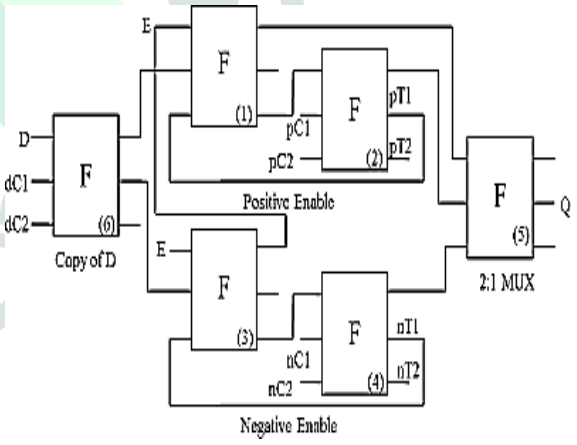

Fig4(a). DET flip-flop

In the proposed design of testable reversible DET flip- flop, the positive enable testable reversible D latch and the negative enable testable reversible D latch are set up in parallel. The Fredkin gates labelled as 1 and 2 forms the positive enable, while the Fredkin gates labelled as 3 and 4 forms the negative enable testable D latch. In reversible logic Fan-out is not allowed so the Fredkin gate labelled as 6 is used to copy the input signal D.

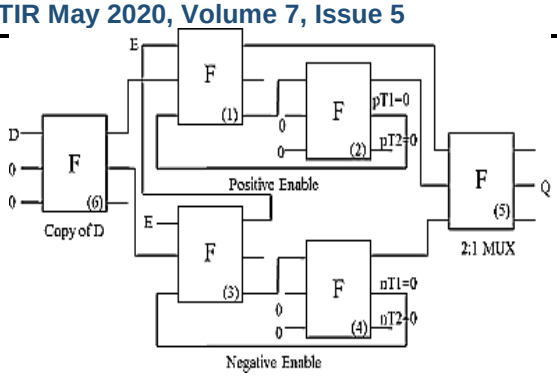

Fig 4(b): Test mode for stuck at 1 fault

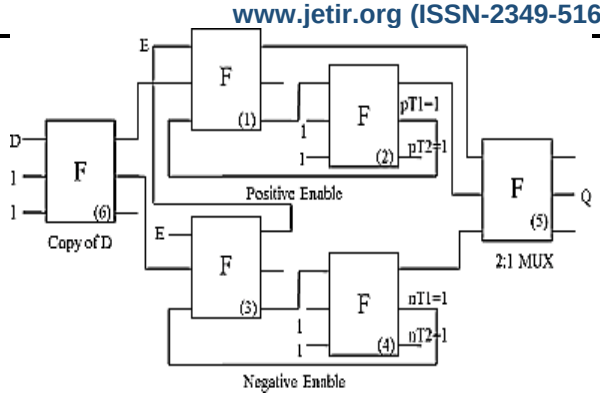

fig 4(c) : Test mode for stuck at 0 fault

2:1 MUX and transfer the output from one of these testable latches (negative enable D latch or the positive enable D latch) that is in the storage state (is holding its previous state) to the output Q. In the proposed design of testable reversible DET flip-flop, nC1 and nC2 are the controls signals of the testable negative enable D latch, while pC1 and pC2 are the control signals of the testable positive enable D latch. Depending on the values of the pC1, pC2, nC1, and nC2, the testable DET flip-flops work either in normal mode or in the testing mode.

In normal mode pC1 and pC2 are given as 0 and 1 and similarly nC1 and nC2 are given as 0 and 1. The $pC1 = 0$, $pC2 = 1$ help in copying the output of the positive enable D latch thus avoiding the Fan-out while the $nC1 = 0$ and $nC2 = 1$ help in copying the output of the negative enable D latch thus avoiding the FO. Similarly in test mode if all signals are given as 0 then it tests the circuit for stuck-at-1 fault. If all the signals are given as 1 then it tests for stuck-at-0 fault.

V.FUTURE ENHANCEMENT:

In the proposed framework we have structured successive circuits utilizing Fredkin entryway. As consecutive circuit has criticism it underpins reversible rationale and consequently we structured circuits utilizing reversible rationale entryway. So in future I would be structuring combinational circuits which are irreversible utilizing reversible rationale. And furthermore there is a progressed and a mind boggling door than Fredkin entryway which is utilized in nano innovation that is MX-QCA entryway likewise will be planned and relating circuits utilizing that entryway will be structured.

VI.RESULTS:

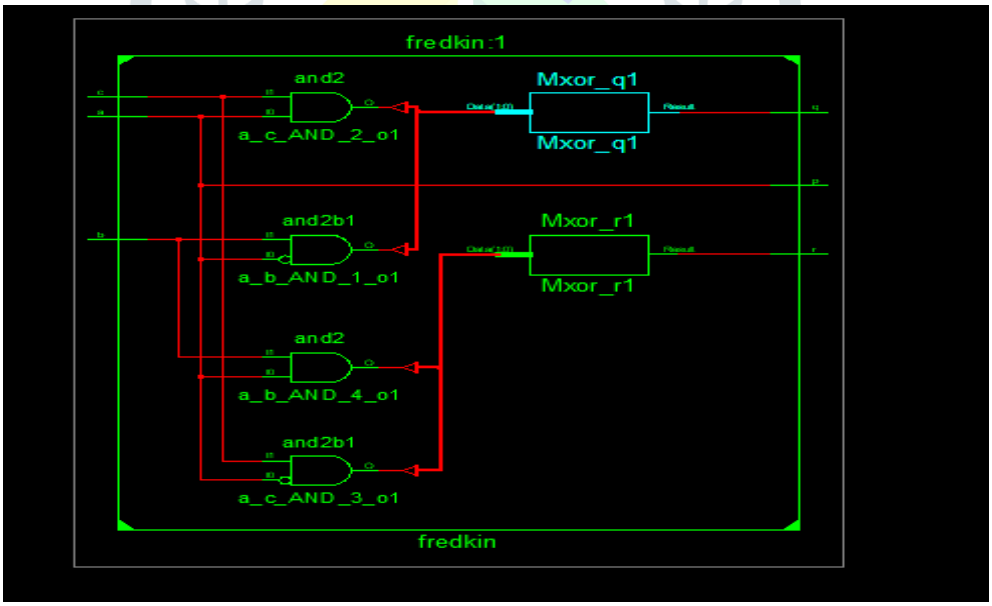

FIG 6(a):SCHEMATIC FOR FREDKIN GATE

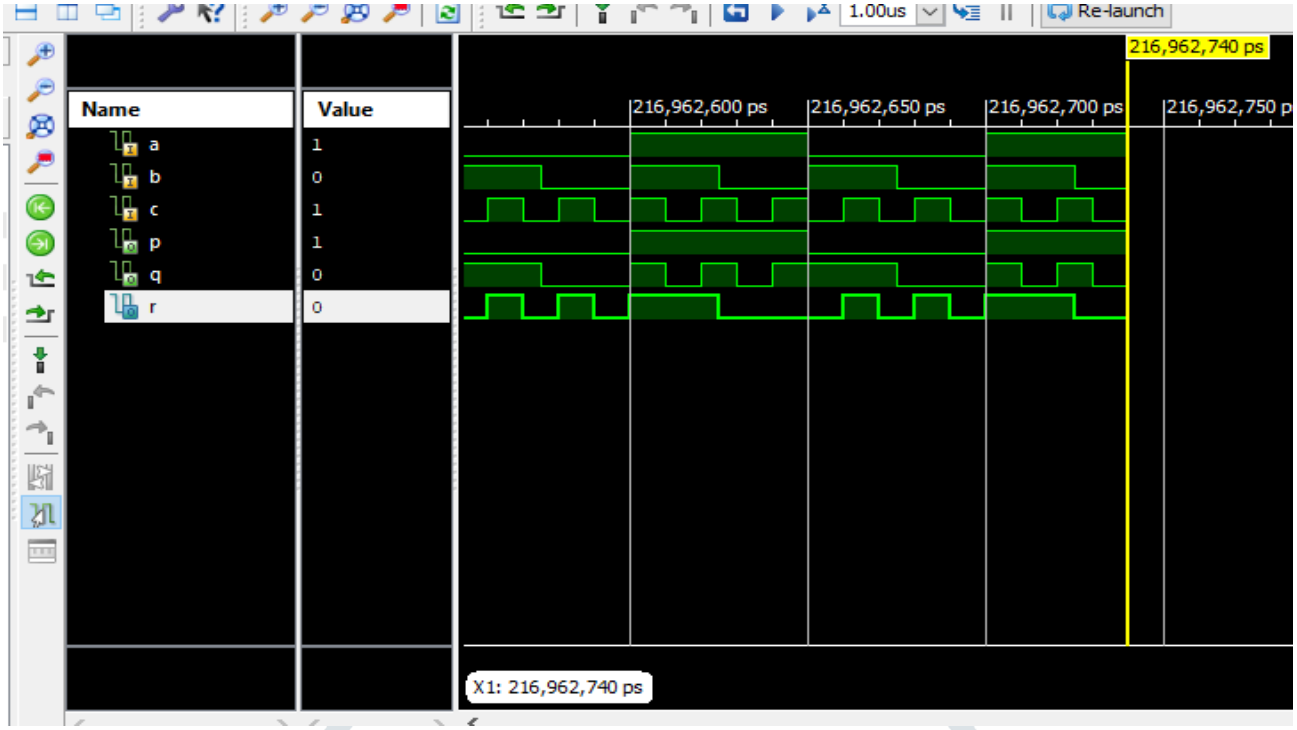

FIG 6(b): FREDKIN GATE WAVEFORMS

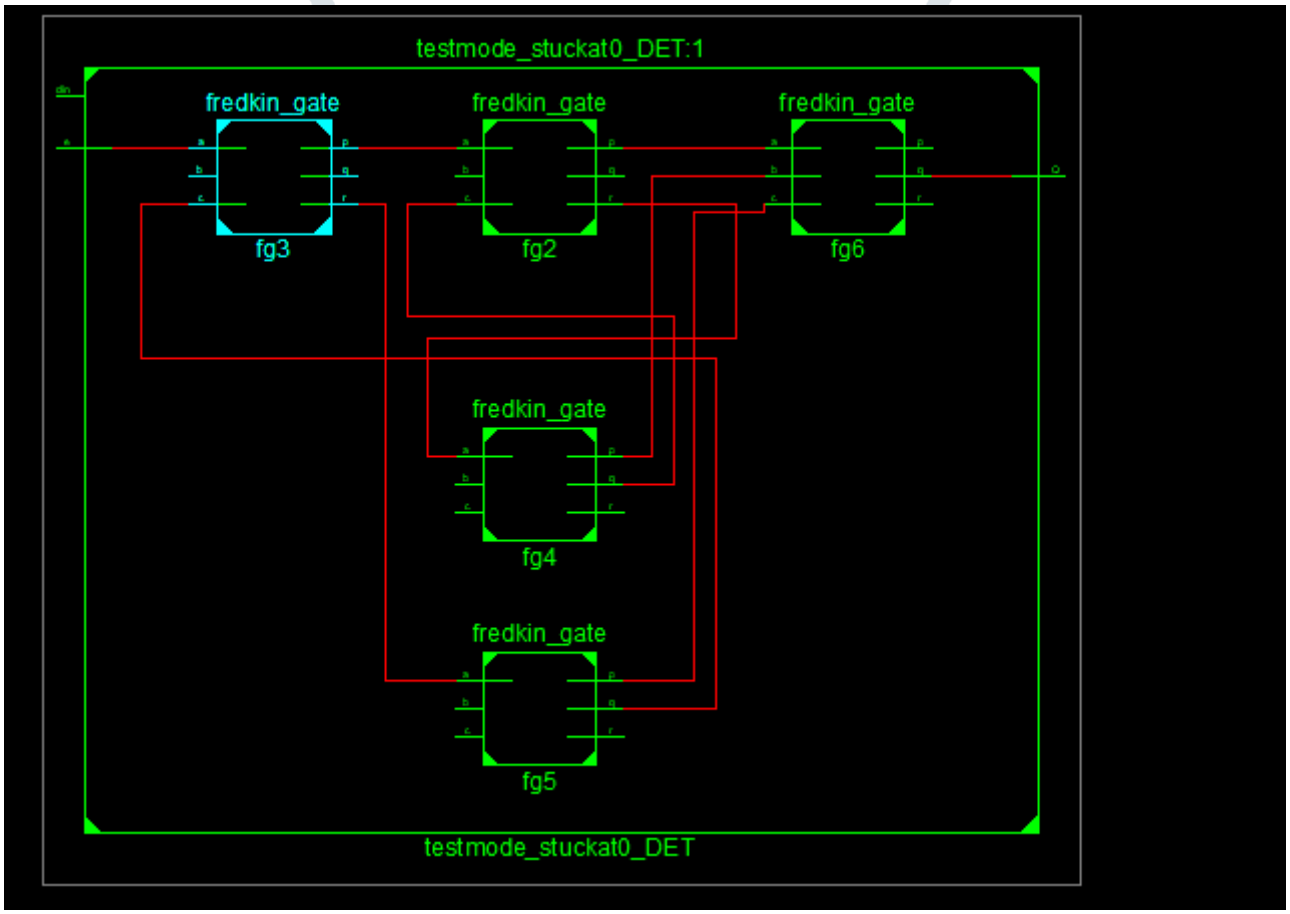

FIG 6(c):SCHMATIC FOR TEST MODE STUCK AT 0 FAULT

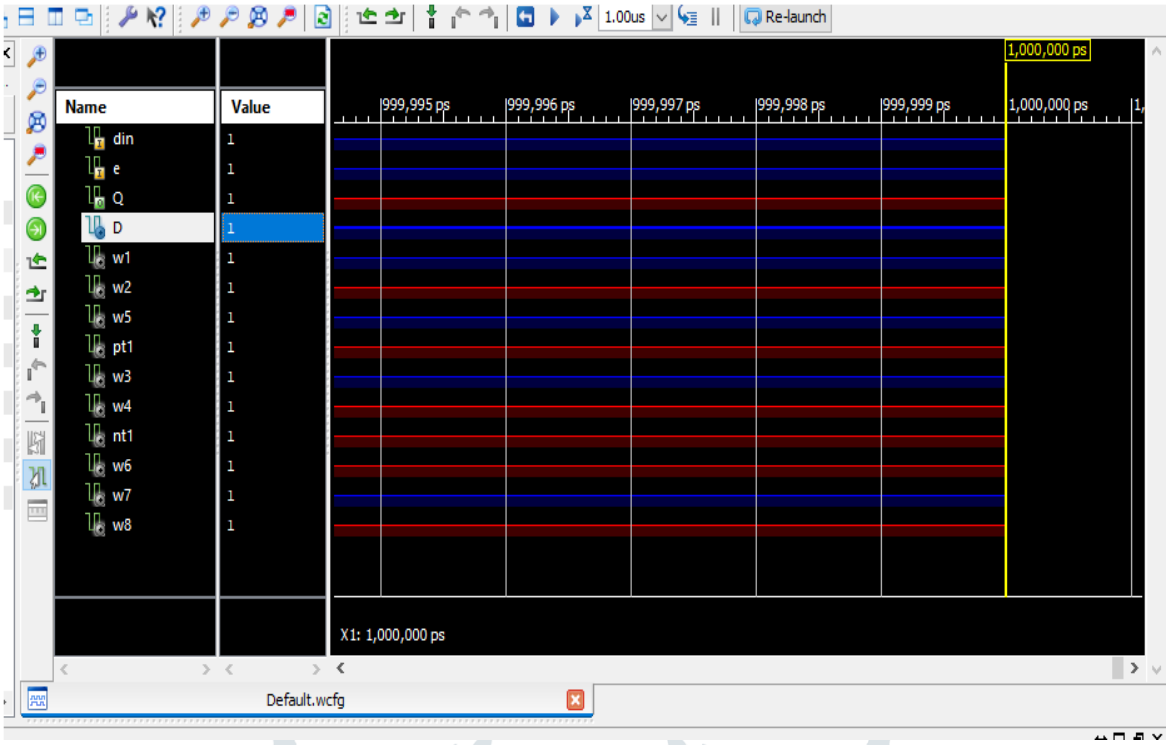

FIG 6(d):WAVE FORM FOR STUCK AT 0 FAULT

VII. CONCLUSION: Thus Reversible sequential circuits are designed using reversible and conservative logic successfully and tested for stuck-at-faults. A design of Fredkin gate, testable D latch using Fredkin gate, Master slave flip-flop using Fredkin gate, DET flip flop is designed. It is made testable only using two vectors 0 and 1 and so complexity is reduced. In future reversible and conservative logic will be designed for combinational circuits and implemented and will be tested for faults. Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit.

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