Design of High Speed Synchronous Counter Using BICMOS Logic

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Abstract: In most of the digital systems counter is a basic and essential component so it is important to design an efficient counter in terms of delay and power. In this paper BICMOS logic has been used for the implementation of 4-bit synchronous counter. BICMOS is the combination of CMOS and Bipolar transistors and the purpose of choosing this logic for designing is to combine the advantages of both Bipolar and CMOS transistor logic. Latch up problem can be completely eliminated by using BICMOS logic. Cadence Virtuoso schematic editor is used to implement the proposed circuit and Cadence Virtuoso analog design environment is used for the simulation process. The estimated power for the proposed counter circuit is 85.07 µw and delay is 18.27 ns.

Index Terms **- BICMOS, Master-Slave D flip flop, Latch up.**

I. INTRODUCTION

For digital systems, counters used as a basic building block. Counter is a sequential circuit, which is collection of flip flops with a clock signal. There are many applications of counter in electronic industry such as timing circuits, signal generator, digital memories, frequency synthesizers and analog to digital converters. Circuit design is an important factor for designing any digital circuit

BICMOS logic is used to design 4-bit Synchronous Counter and then calculate its power consumption and delay. The motive of doing this is to compare delay & power consumption of this proposed counter circuit with prior implemented research results. So, that we can get power efficient counter circuit with low delay.

Cadence EDA tool has used to design the proposed counter. The tool having Cadence Virtuoso schematic editor which gives advanced capabilities of speed and ease the design.

BICMOS is the combination of bipolar and CMOS transistors, which offers fast and low power circuits. CMOS logic have disadvantages like high propagation delay due to large interconnect capacitances and latch up condition but also has advantage of low power dissipation than BJT logic. BJT logic have advantages like high current driving capabilities and high speed than CMOS logic. BICMOS configuration which is the combination of bipolar and cmos logic can combine advantages of both the logics. By using BICMOS configuration latch up problem can be completely eliminated. [1]

In previously done research work, several digital circuits have been designed using different techniques targeting on design accents like power, delay & area. In [1], Divya Bora et.al. used BICMOS technology to design and simulate some of the digital circuits such as logic gates, half adder and full adder on Tanner EDA tool. All of these circuits have certain advantages like fast switching, high gain, large load driving capability, low output impedance and low static power because of using BICMOS logic for designing. Also latch up condition can be completely eliminated.

In [2], Himal Pokhrel et.al. used three different techniques namely CMOS technique, Sleepy transistor technique (STT) and Forced stack technique (FST) to design a proposed 4 - bit binary synchronous counter . Microwind 3.1 and DSCH 3.1 software on 65 nm technology has been used to analyse circuit design and parameters. For different supply voltages height, width, surface area and power consumption have been measured in the case of all the three techniques stated above. Power consumed by CMOS counter is higher compare to remaining two techniques. In case of sleepy transistor technique, the average power reduction is 44.9% and in the case of FST the average power reduction is 70.1% as compared to CMOS counter.

In [3], Yogita Hiremath et.al. proposed a design of synchronous 4-bit up counter using master-slave negative pulse-triggered D flip-flops. Additional synchronous clear and count enable inputs have given to the counter. The design is implemented using Cadence Virtuoso schematic editor and simulated using Cadence Virtuoso analog design environment at 180nm CMOS process technology. The estimated power and delay for this proposed counter is 97.90µW and 20.39ns respectively. In [4], Shilpa Shrigiria et.al. implemented a 16-bit binary counter with clock gating at nibble level. For implementation and simulation Mentor Graphics tool has been used. Finally compared the power consumption of this proposed circuit with normal implementation.

In [5], Gifty John B et.al. proposed a design of scalable fast parallel counter using microwind tool at 0.12µm CMOS technology. This proposed circuit has power consumption of 0.164 mw and speed in 1GHz. In [6], Tehniat Banu1et.al. proposed a design of 4-bit Reversible Asynchronous Up/Down counter using Tanner EDA tool at 250nm CMOS technology. This proposed circuit has improved performance in terms of power dissipation and delay. In [7], Suresh Kumar.R implemented a counter circuit with D Flip flop using microwind tool to reduce power consumption. In [8], Vjaya BhaskarM, implemented logic gates, adder and counter circuits using self-resetting logic at 45nm CMOS technology. These proposed circuits result in low power dissipation and high performance.

In this paper a 4-Bit Synchronous counter has been designed using BICMOS logic. Section 2 explains the circuit of proposed counter. In Section 3 Schematics of counter and its components have been implemented using Cadence Virtuoso schematic editor. Section 4 describes Simulation results and Section 5 concluded the paper.

II. PROPOSED COUNTER

Proposed counter circuit shown in figure 1, consist of 3 AND gates, 4 XOR gates and 4 master-slave D flip-flops. As same clock pulse has been applied for each flip flop so, counter counts one step up with every clock pulse. The master-slave D flip-flop

gives output at the falling edge of the clock and stores the input at rising edge of clock pulse. If enable input is zero (E=0) then counter stops counting and if enable input is one (E=1) then counting action performs with every clock pulse.

For implementation of the proposed synchronous 4-bit counter we need to design individual components of the counter separately using BICMOS logic and afterwards use all the components together to design the counter.

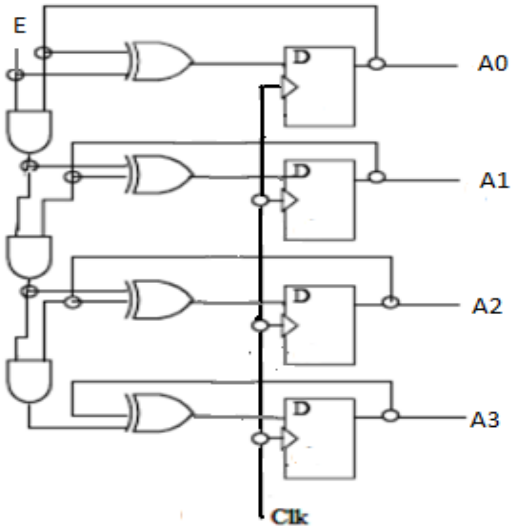

Figure 1: Circuit diagram of Synchronous 4-bit counter

Single phase clocked master-slave D flip flop is shown in figure 2. In this circuit when the inputs disable by either the clock (CK) or the inverted clock (CK) then clocked inverter is used to hold the output. For preventing the glitches at the gate node of the device PMOS MP3 used at the input. When clock is high and input goes low, there may be occurrence of glitches. This removes the requirement for clocked inverter at the input. This will reduce the area & delay. Feedback inverter is used to control the PMOS in feedback switch. Pull down section is used to control the NMOS which shunting the BJT.

Pull down network is having a regular feedback switch in series with another switch and both are controlled by the input & the clock. There is no performance degradation in this BICMOS circuit even if there is a clock skew present. However even for low supply voltages circuit will have faster output response & smaller area.

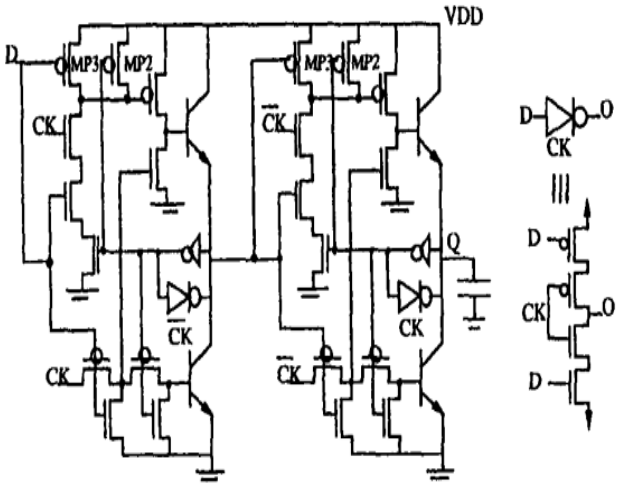

Figure 2: Implemented Master- Slave D flip flop with BICMOS logic

III. SCHEMATIC DESIGN

For implementation of counter we need to create instances of its components independently and subsequently use all the components together. Cadence tool is having Cadence Virtuoso schematic editor to design schematic for any circuit. By using this, schematic diagrams of Inverter, AND gate, XOR gate, counter have been designed and shown in following figures. Implementation of all these circuits have done using BICMOS logic with following specifications: Total Length L=180nm, Width W= 2 µm.

Schematic diagram of Inverter shown in figure 3 having one PMOS, three NMOS and two BJT. Schematic diagram of AND gate shown in figure 4 having three PMOS, five NMOS and two BJT. Schematic diagram of XOR gate shown in figure having six PMOS, eight NMOS and two BJT. Afterward instances of all these components have used to design schematic of counter.

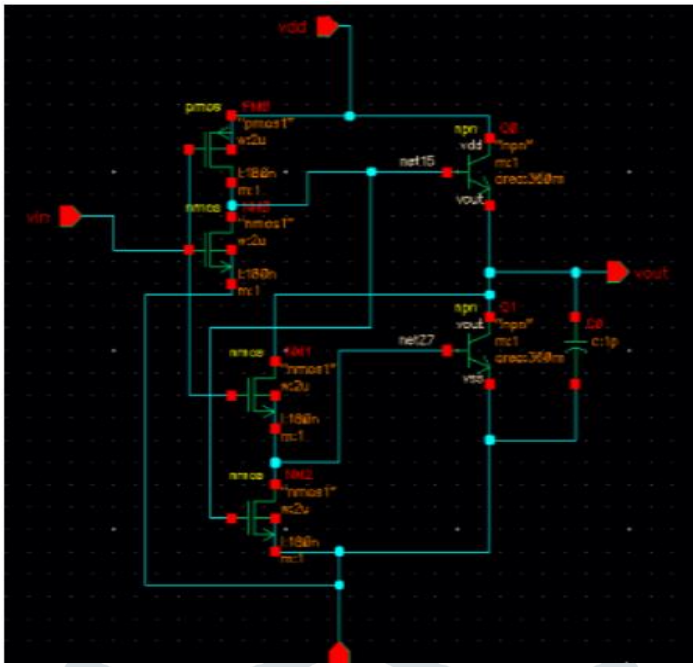

Figure 3: Implemented Design Schematic of Inverter

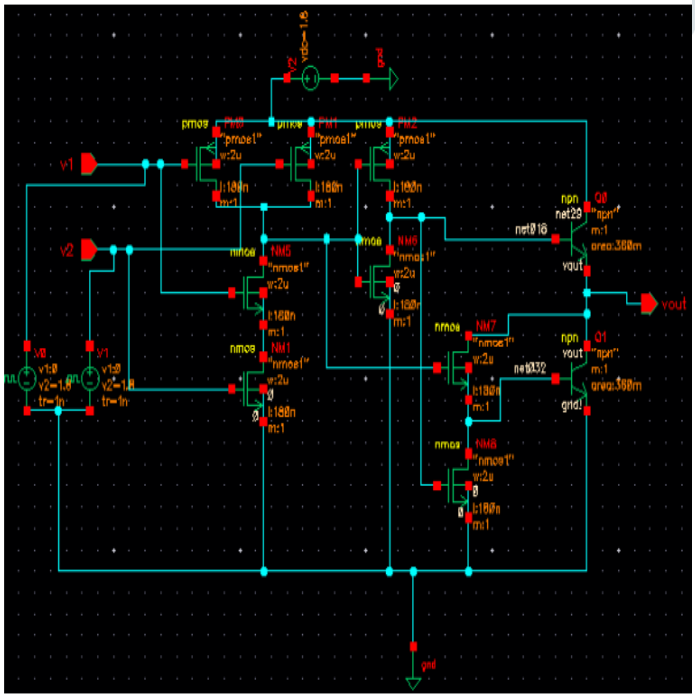

Figure 4: Implemented Design Schematic of AND gate

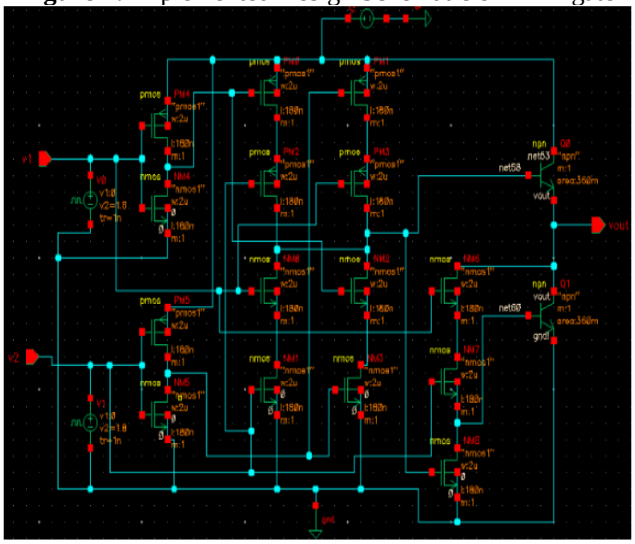

Figure 5: Implemented Design Schematic of XOR gate

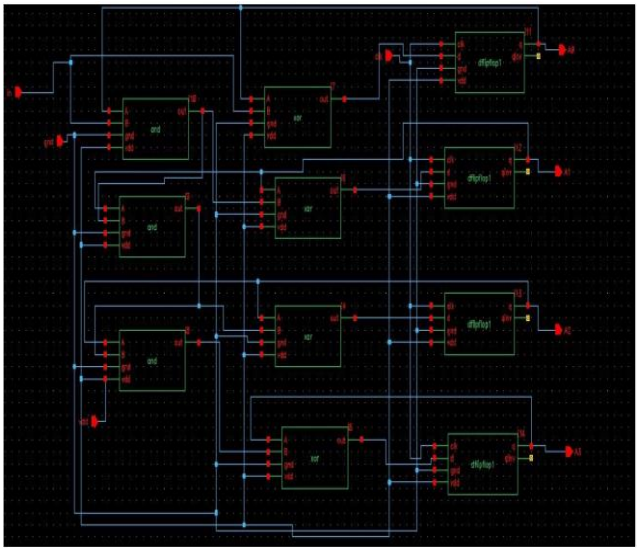

Figure 6: Implemented Design Schematic of 4-bit synchronous counter

IV. SIMULATION RESULTS

Cadence design environment has been used to simulate the schematics of synchronous counter with all its design components and for the analysis of their transient responses. Using simulation results, their logic and characteristics can be easily verified. After the analysis of simulation results, Power and delay for the proposed counter circuit has been calculated and shown in table 1.

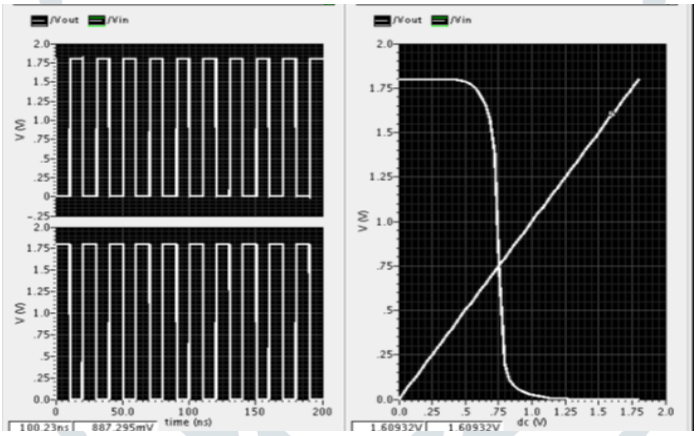

Figure 7: Simulation Waveform for implemented Inverter

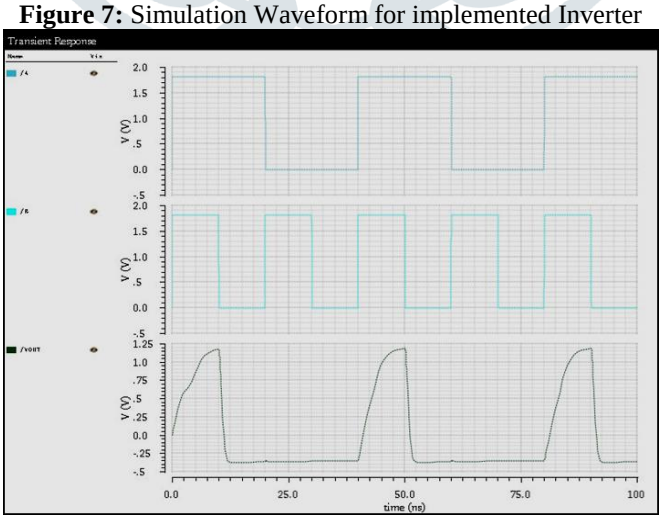

Figure 8: Simulation Waveform for implemented AND gate

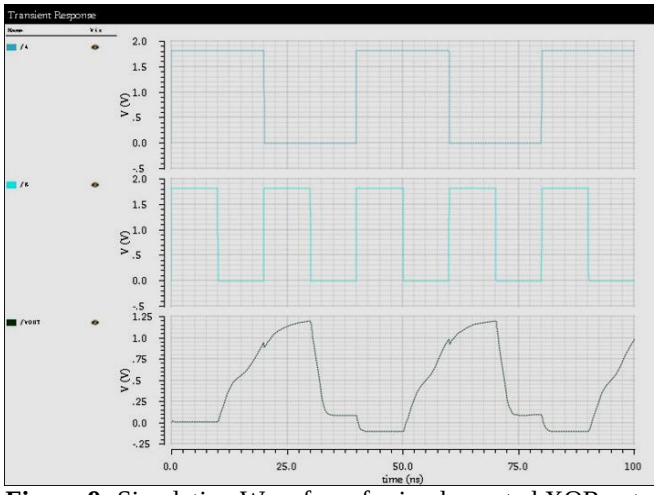

Figure 9: Simulation Waveform for implemented XOR gate

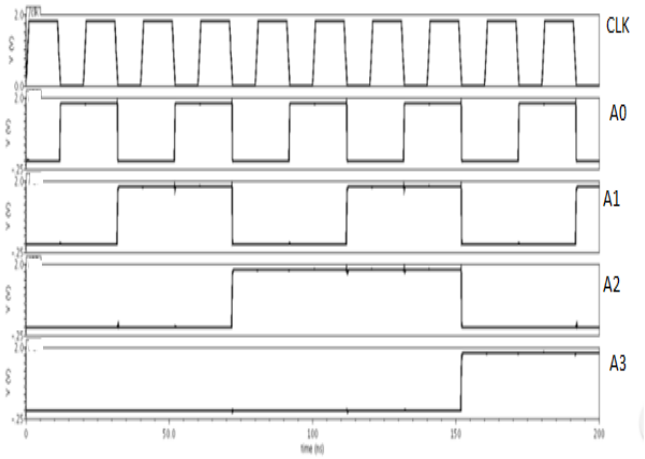

Figure 10: Simulation Waveform for implemented Counter

Table 1: Comparison Table for Delay and Power estimation of Synchronous 4-bit counter

Design Technique	**Synchronous 4-bit counter using BICMOS logic**	**Synchronous 4-bit counter using existing CMOS logic**
Power	85.07 µw	97.90 µw
Delay	18.27 ns	20.39 ns

V. CONCLUSION

In this paper, implementation of synchronous 4-bit counter has been done using BICMOS logic. The purpose of doing this is to design a power efficient counter with high speed. Cadence tool has been used to simulate and analyse the circuit on the basis of its performance parameters such as power estimation & delay. When the results of proposed counter circuit compared with previously done research results, for Synchronous 4-bit counter using CMOS logic Power consumption and delay results were 97.90 µw & 20.39 ns respectively and using BICMOS logic power consumption is 85.07 µw and delay is 18.27 ns. It can be concluded from the observations that power consumption and delay for the proposed counter circuit is better than the counter circuit implemented using CMOS logic.

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