Two stage conversion based SMPS for high Power Application

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Abstract: Designing of Switched mode power supply (SMPS) involve many challenges while developing for specific application. This study proposes two stage conversion based SMPS design with Interleaved boost as PFC stage and Phase shifted full bridge as DC-DC converter stage. The design is simulated to obtain 600W,16V output DC for universal input AC range. Stage wise power analysis is done which produces 98.48% and 93.27% efficiency for PFC and DC-DC converter stages respectively.

***Index terms*- SMPS, PFC, Interleaved boost, Phase shifted full bridge**

Nomenclature-

V'_{IN} = Rectified input voltage
V'_{OUT} = PFC stage output voltage
I'_{ripple} = Input ripple current at the PFC side
P'_{OUT} = Output power at the PFC stage
f'_s = Switching frequency in PFC stage
D' = Duty cycle of PFC stage
V_{RDSON} = Voltage drop across MOSFET
P_{OUT} = Output Power of SMPS
V_{OUT} = Output voltage of SMPS
η = Converter stage efficiency
f_{LINE} = Input line frequency
f_s = Switching frequency in converter stage
D = Duty cycle of converter stage
I_{ripple} = Output ripple current of converter stage

I. Introduction

Switched mode power supplies are most popular power supply option in most of the industrial applications. SMPS term was first used in 1976 which was patent on power supply circuit for TV receiver. During 70s most of the application started moving from conventional linear supply to SMPS. Unlike linear supply which requires large transformer to convert low frequency AC to higher or lower voltage, SMPS is operated in high frequencies which reduces their sizes an make them compact.

A basic SMPS involves a switching element (MOSFETs or IGBTs) in which the switching is controlled by a controller which generates square wave according to the duty cycle requirement. This duty cycle will depend on the output voltage requirement and the input voltage. In some of the SMPS design a high frequency transformer used which is used to step down the DC voltage according to the output voltage requirement. While designing a SMPS one can choose different topology for the DC-DC conversion. There are non-isolated topologies such as Buck, Boost and isolated topologies such as Fly back, Forward, Half bridge, Full bridge topologies are popular. Each topology has its own limitations with respect to operating voltages and Power. For high power applications (greater than 500W) Half bridge and Full bridge topologies are more preferred. A phase shifted full bridge is the improved version of the full bridge which reduces the switching power losses by Zero Voltage Switching [2].

When AC signal drawn from the source, the Voltage (V) and the Current (I) might not be in phase with each other. This might be due to any passive component involving the circuit. Which leads to the lower value of the power received than the expected one. Due to the high-power application there might exists harmonic component of the input power i.e. the components of the input power with lower magnitude at different fundamental frequencies. A PFC circuit provide solution for both these cases [3].

Different equipment needs different supply based on the rating of the design. In many cases there might not be off the shelf product available for given specification. So, one must design customized product based on the specifications such as wattage, voltage rating. This work involves designing of Switch mode power supply module that gives 600W,16V DC output. SMPS design with two stages (Power factor correction and DC-DC converter) is proposed to meet the specification.

II. Methodology

The proposed SMPS architecture consists of mainly two stages i.e. Power factor correction stage and a DC-DC converter stage as shown in the Figure 1.

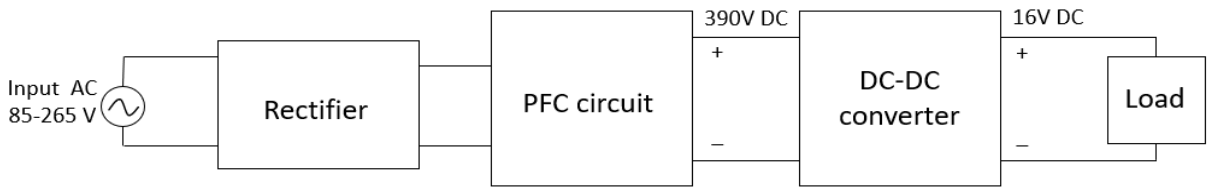

Figure 1. Two stage conversion based SMPS architecture

2.1 RECTIFICATION

Rectification is the conversion of the input AC to DC. For this one can use diode bridge. The universal input AC is converted to the DC in this stage.

2.2 POWER FACTOR CORRECTION (PFC)

Power factor correction block involves circuits that is used to maximize the real power available from the input. Due to various passive components the input voltage and current are not in phase. Also, high power input leads to the harmonic components. PFC circuits helps in reduction of harmonic losses as well as it makes sure that current and voltages are in phase. In the proposed design Interleaved boost type of PFC is chosen which gives nominal output voltage of 390V.

2.3 DC-DC CONVERTER

This is the core block of SMPS which involves conversion of high DC input to lower DC voltage which will be constant throughout the time. SMPS converter block involves switching element which will be controlled by a controller which controls duty cycle given to the switch based on feedback provided by the output end. Designing of converter block is critical. Selection of topology and components based on the operating voltage and power plays important role. The design proposes Phase shifted full bridge converter to produce 16V DC from PFC stage output.

III. DESIGN AND IMPLEMENTATION OF TWO STAGE SMPS

Based on proposed architecture 600W,16V SMPS is designed. Table 3.1 indicates the specification considered for the design. Universal AC of range 85-265V with line frequency 47-63Hz is considered as the input.

TABLE 3.1 Design specification

Parameter	Terminology	Unit	Min	Typical	Max
Input Voltage (AC)	V_{ac}	V	85		265
Line frequency	f_{LINE}	Hz	47		63
Output Power	P_{OUT}	W		600	
Output Voltage (DC)	V_{OUT}	V		16	

3.1 PFC design

PFC stage comes before DC-DC converter stage do the job of maintaining low harmonics and maximizing power factor. In this design Interleaved boost PFC is selected which best suited for the PFC specification defined before design. Table 3.2 gives the input specification considered. Figure 2 shows two cell interleaved PFC circuit used for the design.

TABLE 3.2 PFC Specification

Parameter	Terminology	Unit	Min	Typical	Max
Input Voltage (AC)	V_{ac}	V	85		265
Output Power	P'_{OUT}	W			750
Output Voltage (DC)	V'_{OUT}	V	370	390	410
Switching frequency	f'_s	kHz		200	
Efficiency	η'	%	90		
Duty cycle	D'				0.97

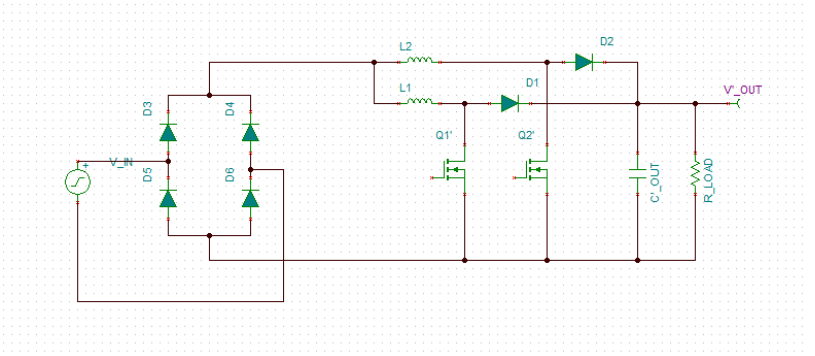

Figure 2. Circuit used for Interleaved boost PFC

3.1.1 Inductor Selection

Boost inductors L_1 and L_2 are selected based on the duty cycle value. And the operating duty cycle is calculated using Eq.1.With the calculated duty cycle inductor values are determined using Eq.2.

$$D' = 1 - \frac{V'_{IN}}{V'_{OUT}} \qquad (1)$$

$$L_1 = L_2 = \frac{V'_{OUT} \times D'(1-D')}{f'_s \times I'_{ripple}} \quad (2)$$

The input ripple current I'_{ripple} is calculated based on maximum rms current at the input.Eq.3 gives maximum rms current. And the Eq.4 indicates I'_{ripple}.

$$I_{line\_max} = \frac{P'_{OUT}}{\times V_{ac\_min}} \quad (3)$$

$$I'_{ripple} = 0.5 \times I_{line\_max} \quad (4)$$

3.1.2 Capacitor Selection

The minimum value of the output capacitor can be determined using the Eq.5.

$$C'_{OUT} \geq \frac{\frac{2 \times P'_{OUT}}{f_{LINE}}}{(V'_{OUT})^2 - (V'_{OUT} \times 0.75)^2} \quad (5)$$

3.1.3 MOSFETs Selection

In order sustain input voltage stress and the rms current condition MOSFETs Q'$_1$ and Q'$_2$ are selected with 500V drain to source voltage capacity,11A max current capacity.

3.3 DC-DC converter design

DC-DC converter is second stage of the proposed design. High DC output produced in the PFC stage is converted to the final required DC voltage. Table 3.3 gives the parameter considered for the DC-DC converter design. Phase shifted Full bridge topology is selected for the design. Figure 3 shows the topology used in the designing of the converter. The design based on synchronous rectifiers at the secondary side of the transformer as shown in the Figure 3.

TABLE 3.3 DC-DC converter Specification

Parameter	Terminology	Unit	Min	Typical	Max
Converter stage input voltage	V_{DC} (V'_{OUT})	V	85		265
Output Power	P_{OUT}	W		600	
Output Voltage (DC)	V_{OUT}	V		16	
Switching frequency	f_s	kHz		200	
Efficiency	η	%	90		
Duty cycle	D				0.7

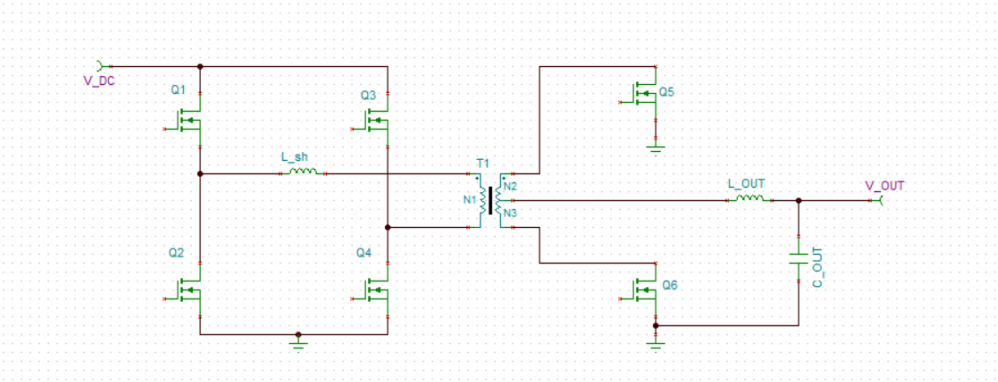

Figure 3. Circuit used for Phase shifted full bridge

3.2.1 Transformer Selection

The transformer used in the design is center tapped with one primary end two secondary coils. The turns ratio is calculated by the Eq.6.

$$a1 = \frac{(V_{INMIN} - 2 \times V_{RDSON}) \times D_{MAX}}{V_{OUT} + V_{RDSON}} \quad (6)$$

The magnetic inductance is calculated by the Eq.7. And the Eq.8 give the duty cycle of the square wave given to the switching elements. For the calculation allowed output ripple current (I_{ripple}) is assumed as ($0.2 \times I_{OUT}$).

$$L_{MAG} \geq \frac{V_{IN} \times (1 - D_{TYP})}{\frac{I_{ripple}}{a1} \times 0.5 \times f_s} \quad (7)$$

$$D_{TYP} = \frac{(V_{OUT} + V_{RDSON}) \times a1}{(V_{IN} - 2 \times V_{RDSON})} \quad (8)$$

3.2.2 Output inductor Selection

The output inductor value mainly depends on the output ripple current. Its value is calculated using Eq.9.

$$L_{OUT} = \frac{V_{OUT} \times (1 - D_{TYP})}{I_{ripple} \times f_s} \qquad (9)$$

3.2.3 Output capacitor Selection

The output capacitor is selected based on the holdup time requirement. Eq.10 gives the holdup time condition and the Eq.11 gives the minimum value of output capacitor.

$$t_{HU} = \frac{\frac{L_{OUT} \times P_{OUT} \times 0.9}{V_{OUT}}}{V_{OUT}} \qquad (10)$$

$$C_{OUT} \geq \frac{\frac{P_{OUT} \times 0.9 \times t_{HU}}{V_{OUT}}}{V_{TRAN} \times 0.1} \qquad (11)$$

3.1.4 MOSFETs Selection

In order sustain input voltage stress, considering power and efficiency parameters MOSFETs Q_1-Q_4 are selected with 650V drain to source capacity,20A max current capacity (Power MOSFETs). And MOSFETs Q5 and Q6 are selected with 75V drain to source capacity,120A max current capacity.

3.4 Controller ICs for the design

Both PFC stage and the converter stage involves two separate controller ICs to produce square wave according to output voltage. UCC28950 controller is used for Phase shifted full bridge design and UCC28070 is used for Interleaved boost PFC design.

IV. SIMULATION RESULTS

Proposed design is simulated using TINA-TI Spice simulation tool. Transient response for each stage is observed by considering input AC as 230V,50Hz. The design is verified for universal range. Figure 4 and Figure 5 shows the steady state output voltage waveforms at the PFC and converter stage respectively. The steady state output 15.89 V is obtained as shown in the Figure 5. The variation in the output voltage compare to the expected 16V is due to non-ideal characteristics of MOSFETs and the controller ICs.

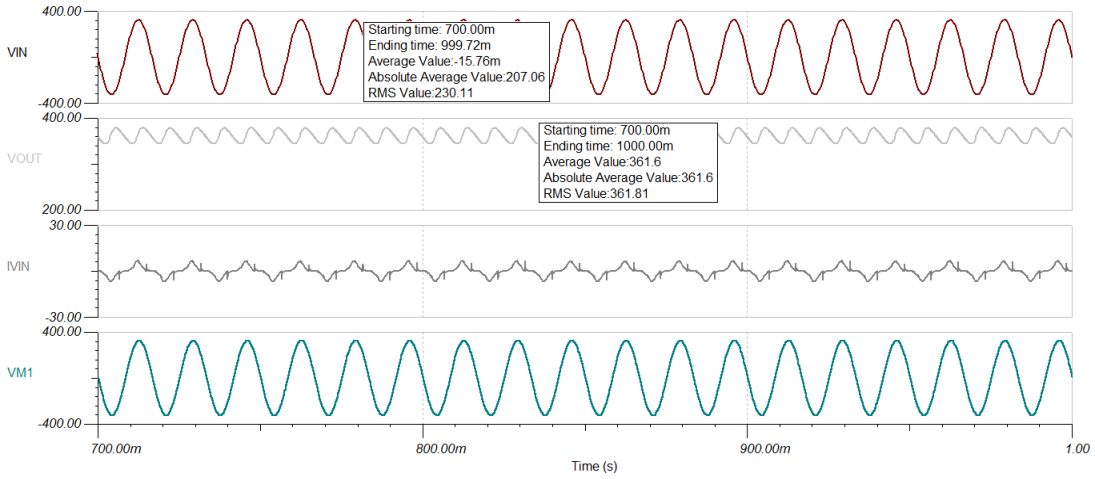

Figure 4. PFC stage steady state output

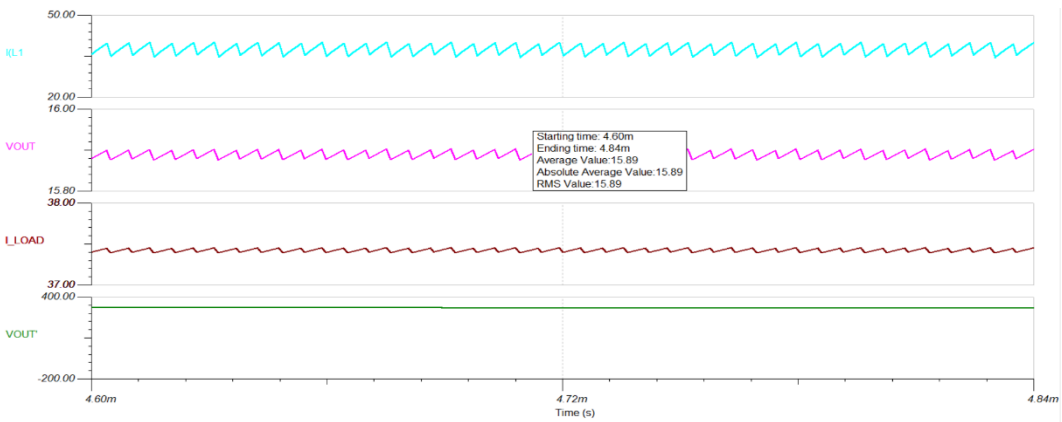

Figure 5. DC-DC converter stage steady state output

Power Analysis is done to measure the output power and efficiency of each stages. Figure 6 shows the output power waveform. At steady state 596.47W output power (P_{OUT}) is observed.

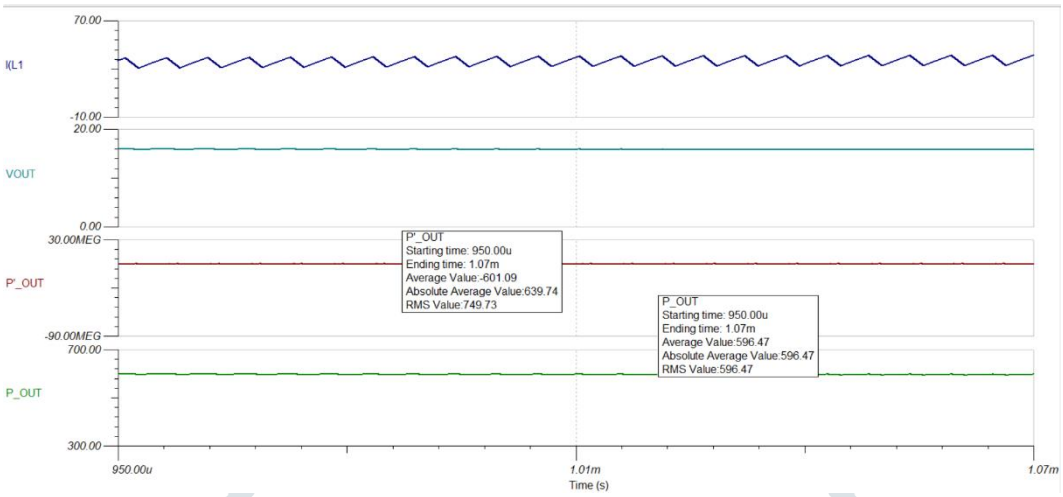

Figure 6. Output Power at steady state

Table 4.1 gives the efficiency of each stages and the line and load regulation of the design. With the design 98.48% efficiency at PFC and 93.27% efficiency at the converter stage is achieved.

TABLE 4.1 Simulation results

PFC stage Efficiency	98.48 %
Converter stage Efficiency	93.27 %
Overall Efficiency	91.85 %
Line regulation	0.05 %
Load regulation	6.92 %

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REFERENCES

[1] J. C. Maraga˜no-Schmidt and J. Renes-Pinheiro,” Comparative study of Full-Bridge and Double Half-Bridge converters,” 2015 CHILEAN Conference on Electrical, Electronics Engineering, Information and Communication Technologies (CHILECON), Santiago, 2015, pp. 453-460.

[2] Y. Sun and B. Jiao,”Design of a soft-switched phase-shift full bridge converter,” 2016 3rd International Conference on Systems and Informatics (ICSAI), Shanghai, 2016, pp. 230-234

[3] W. Su and H. Ming, “Research and simulation of active power factor correction,” 2011 International Conference on Consumer Electronics, Communications and Networks (CECNet), XianNing, 2011, pp. 5156-5158

[4] H. Xu, D. Chen, F. Xue and X. Li,”Optimal Design Method of Interleaved Boost PFC for Improving Efficiency from Switching Frequency, Boost Inductor, and Output Voltage,” in IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6088-6107, July 2019

[5] P. R. Mohanty, A. K. Panda and D. Das,”An active PFC boost converter topology for power factor correction,” 2015 Annual IEEE India Conference (INDICON), New Delhi, 2015, pp. 1-5.

[6] R. Beibei, W. Dan, M. Chengxiong, Q. Jun and Z. Jiangang, "Analysis of full bridge DC-DC converter in power system," 2011 4th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), Weihai, Shandong, 2011, pp. 1242-1245, doi: 10.1109/DRPT.2011.5994085.

[7] D.J. Shortt, W.T. Michael, R.L. Avert, and R.E. Palma, “A 600 W four stage phase-shifted parallel DC-DC converter,”, IEEE Power Electronics Specialists Conf., 1985, pp. 136-143

[8] Patil, Sandeep & Vemuru, Srinivasa & Devabhaktuni, Vijay & Al-Olimat, Khalid. (2013). Comparison of multilevel DC-DC converter topologies. IEEE International Conference on Electro Information Technology. 1-5. 10.1109/EIT.2013.6632681.

[9] Jeong-Eon Park, Jong-Woo Kim, B. Lee and G. Moon,”Design on topologies for high efficiency two-stage AC-DC converter,” Proceedings of The 7th International Power Electronics and Motion Control Conference, Harbin, 2012, pp. 257-262.

[10] Patil, Sandeep & Devabhaktuni, Vijay & Vemuru, Srinivasa. (2013). Operation and transition loss analysis in modified multilevel DC-DC converter modules. 699-704. 10.1109/ICRERA.2013.6749844.